The Flyback Converter

Lecture notes

ECEN4517

- Derivation of the flyback converter: a transformer-isolated version of the buck-boost converter
- Typical waveforms, and derivation of $M(D) = V/V_g$
- Flyback transformer design considerations
- Voltage clamp snubber

Derivation of the flyback converter

The flyback converter is based on the buck-boost converter. Its derivation is illustrated in Fig. 1. Figure 1(a) depicts the basic buck-boost converter, with the switch realized using a MOSFET and diode. In Fig. 1(b), the inductor winding is constructed using two wires, with a 1:1 turns ratio. The basic function of the inductor is unchanged, and the parallel windings are equivalent to a single winding constructed of larger wire. In Fig. 1(c), the connections between the two windings are broken. One winding is used while the transistor Q_1 conducts, while the other winding is used when diode D_1 conducts. The total current in the two windings is unchanged from the circuit of Fig. 1(b); however, the

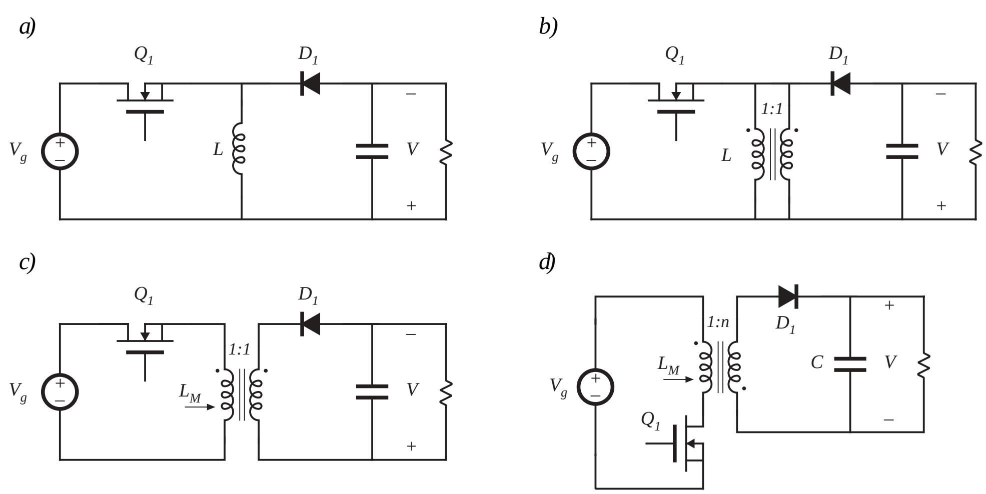


Fig. 1. Derivation of the flyback converter: (a) buck-boost converter, (b) inductor L is wound with two parallel wires, (c) inductor windings are isolated, leading to the flyback converter, (d) with a 1:n turns ratio and positive output.

current is now distributed between the windings differently. The magnetic fields inside the inductor in both cases are identical. Although the two-winding magnetic device is represented using the same symbol as the transformer, a more descriptive name is “two-winding inductor”. This device is sometimes also called a “flyback transformer”. Unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer. Figure 1(d) illustrates the usual configuration of the flyback converter. The MOSFET source is connected to the primary-side ground, simplifying the gate drive circuit. The transformer polarity marks are reversed, to obtain a positive output voltage. A 1:*n* turns ratio is introduced; this allows better converter optimization.

Analysis of the flyback converter

The behavior of most transformer-isolated converters can be adequately understood by modeling the physical transformer with a simple equivalent circuit consisting of an ideal transformer in parallel with the magnetizing inductance. The magnetizing inductance must then follow all of the usual rules for inductors; in particular, volt-second balance must hold when the circuit operates in steady-state. This implies that the average voltage applied across every winding of the transformer must be zero.

Let us replace the transformer of Fig. 1(d) with the equivalent circuit described above. The circuit of Fig. 2(a) is then obtained. The magnetizing inductance L_M functions in the same manner as inductor L of the original buck-boost converter of Fig. 1(a). When transistor Q_1 conducts, energy from the dc source V_g is stored in L_M. When diode D_1 conducts, this stored energy is transferred to the load, with the inductor voltage and current scaled according to the 1:*n* turns ratio.

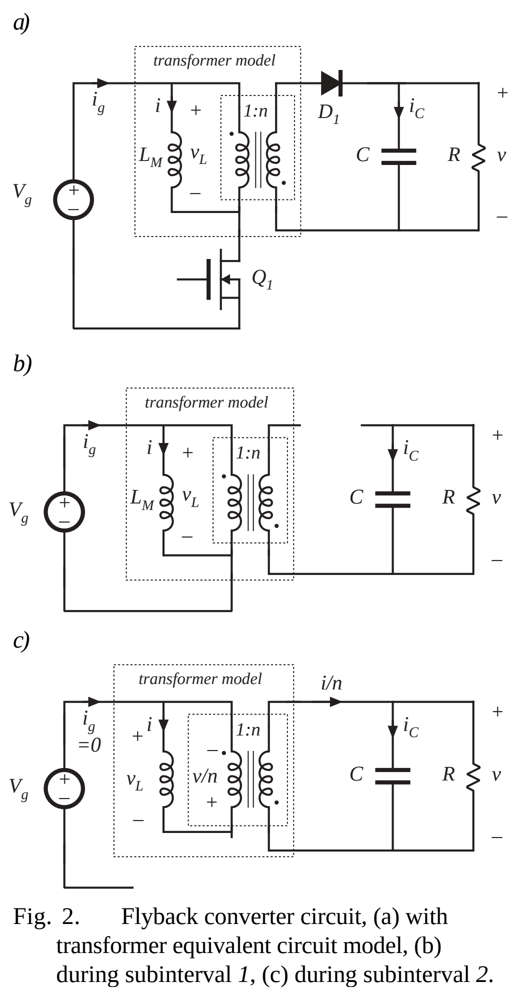


Fig. 2. Flyback converter circuit, (a) with transformer equivalent circuit model, (b) during subinterval *1*, (c) during subinterval *2*.

During subinterval *1*, while transistor Q_1 conducts, the converter circuit model reduces to Fig. 2(b). The inductor voltage v_L, capacitor current i_C, and dc source current i_g, are given by

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{v}{R} \\ i_g &= i \end{aligned} \qquad (1)$$

With the assumption that the converter operates with small inductor current ripple and small capacitor voltage ripple, the magnetizing current i and output capacitor voltage v can be approximated by their dc components, I and V, respectively. Equation (1) then becomes

$$\begin{aligned} v_L &= V_g \\ i_C &= -\frac{V}{R} \\ i_g &= I \end{aligned} \qquad (2)$$

During the second subinterval, the transistor is in the off-state, and the diode conducts. The equivalent circuit of Fig. 2(c) is obtained. The primary-side magnetizing inductance voltage v_L, the capacitor current i_C, and the dc source current i_g, for this subinterval are:

$$\begin{aligned} v_L &= -\frac{v}{n} \\ i_C &= \frac{i}{n} - \frac{v}{R} \\ i_g &= 0 \end{aligned} \qquad (3)$$

It is important to consistently define $v_L(t)$ on the same side of the transformer for all subintervals. Upon making the small-ripple approximation, one obtains

$$\begin{aligned} v_L &= -\frac{V}{n} \\ i_C &= \frac{I}{n} - \frac{V}{R} \\ i_g &= 0 \end{aligned} \qquad (4)$$

The $v_L(t)$, $i_C(t)$, and $i_g(t)$ waveforms are sketched in Fig. 3.

Application of the principle of volt-second balance to the primary-side magnetizing inductance yields

$$\langle v_L \rangle = D\,(V_g) + D'\,(-\frac{V}{n}) = 0 \qquad (5)$$

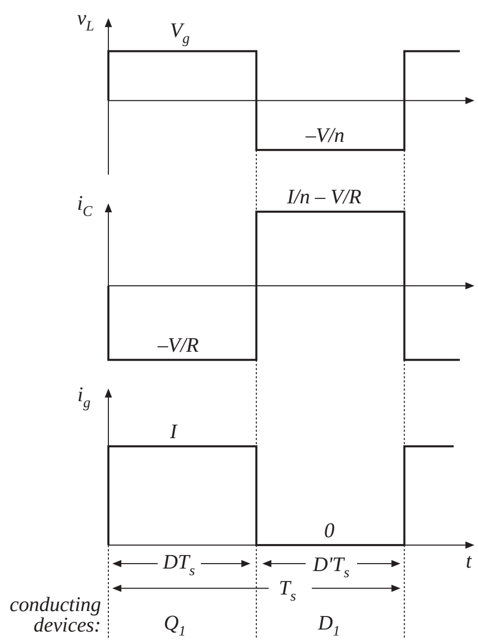


Fig. 3. Flyback converter waveforms, continuous conduction mode.

Solution for the conversion ratio then leads to

$$M(D) = \frac{V}{V_g} = n\,\frac{D}{D'} \tag{6}$$

So the conversion ratio of the flyback converter is similar to that of the buck-boost converter, but contains an added factor of n.

Application of the principle of charge balance to the output capacitor C leads to

$$\left\langle i_C \right\rangle = D\,(-\frac{V}{R}) + D'\,(\frac{I}{n} - \frac{V}{R}) = 0 \tag{7}$$

Solution for I yields

$$I = \frac{nV}{D'R} \tag{8}$$

This is the dc component of the magnetizing current, referred to the primary. The dc component of the source current i_g is

$$I_g = \left\langle i_g \right\rangle = D\,(I) + D'\,(0) \tag{9}$$

An equivalent circuit which models the dc components of the flyback converter waveforms can be constructed. The resulting dc equivalent circuit of the flyback converter is given in Fig. 4. It contains a 1:D buck-type conversion ratio, followed by a (1 – D):1 boost-type conversion ratio, and an added factor of 1:n, arising from the flyback transformer turns ratio.

The flyback converter is commonly used at the 50-100W power range, as well as in high-voltage power supplies for televisions and computer monitors. It has the advantage of very low parts count. Multiple outputs can be obtained using a minimum number of parts: each additional output requires only an additional winding, diode, and capacitor. The peak transistor voltage is equal to the dc input voltage V_g plus the reflected load voltage V/n; in practice, additional voltage is observed due to ringing associated with the transformer leakage inductance. A *snubber circuit* may be required to clamp the magnitude of this ringing voltage to a safe level that is within the peak voltage rating of the transistor.

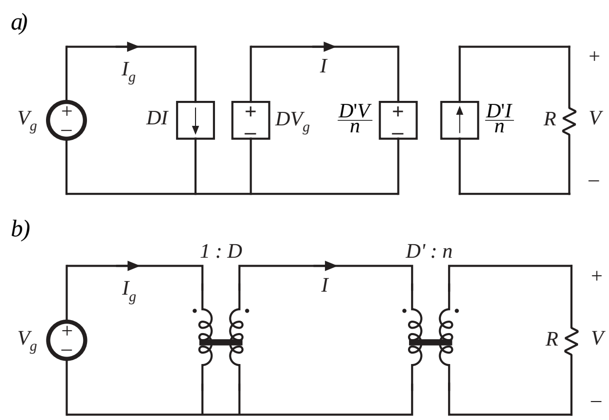


Fig. 4. Flyback converter equivalent circuit model: (a) circuits corresponding to Eqs. (5), (7), and (9); (b) equivalent circuit containing ideal dc transformers.

Flyback transformer design

For this lab, you are given the following flyback transformer design tasks:

- select L_M such that $\Delta i = 50\%$ of I
- use turns ratio $n = \frac{n_2}{n_1} = 1.5$
- use a PQ 32/20 core $\Rightarrow A_c, W_A, MLT, l_m$ are given
- select turns n_1 such that total loss is minimized:

$$\text{minimize} \quad P_{tot} = \underbrace{P_{fe}}_{\substack{\text{core} \\ \text{loss}}} + \underbrace{P_{cu}}_{\substack{\text{loss in resistances} \\ \text{of primary and secondary} \\ \text{windings}}}$$

- determine air gap length l_g
- determine primary and secondary wire gauges
- use fill factor $K_u = 0.4$
- check to make sure that the peak B does not cause the core to saturate.

Choosing n_1 to minimize P_{tot}

We can relate B_{ac} to n_1 and Δi using the basic formula $\lambda = Li$:

$$\lambda_{ac} = n_1 A_c B_{ac} = L_M \Delta i$$

so $$B_{ac} = \frac{L_M \Delta i}{n_1 A_c}$$

Once we have solved the converter circuit to find the desired values of L_M and Δi, then L_M, Δi, and A_c are known. Hence this equation relates B_{ac} to n_1.

Increasing n_1 decreases B_{ac}, which decreases the core loss P_{fe}.

Computing core loss

Core loss P_{fe} depends on the peak value of the ac component of flux density B_{ac}. Manufacturers published data sheets contain plots of P_{fe}, that follow functions of the form

$$P_{fe} = K_{fe} \, B_{ac}^{\beta} \, A_c \ell_m$$

see TDK H7C1 ferrite data – course website links to data sheets

K_{fe} is a constant of proportionality that depends on switching frequency and core material

β is an exponent that depends on core material

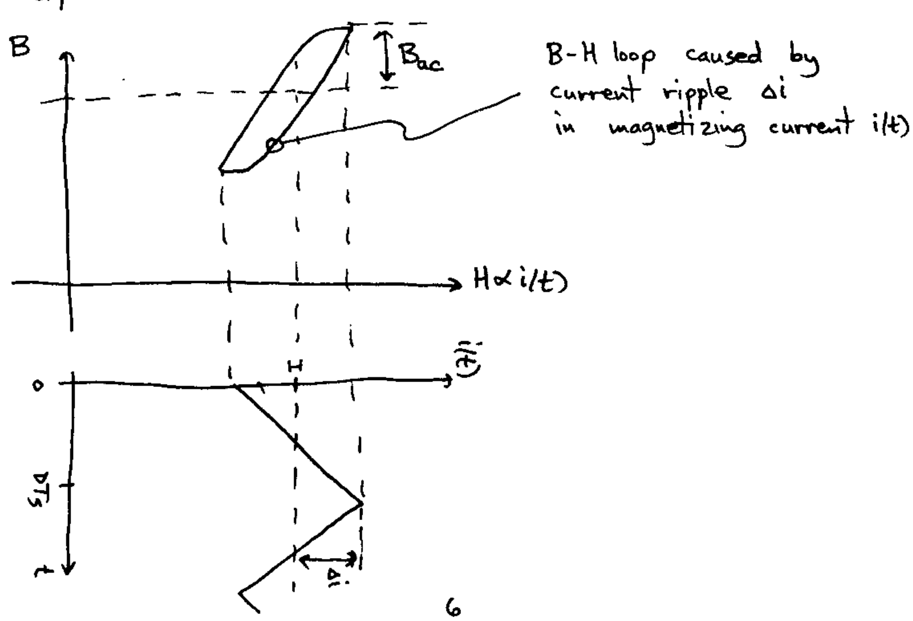
$A_c \ell_m$ is the volume of the core

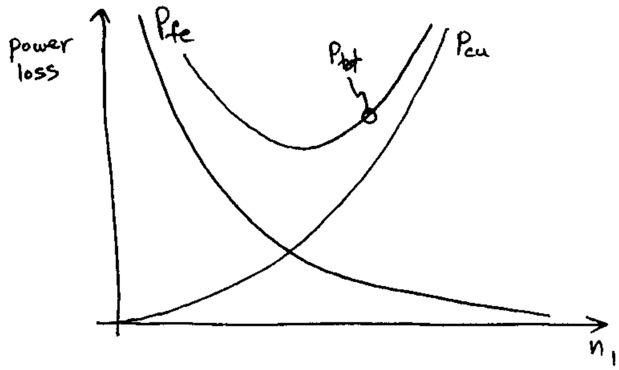
For H7C1 material:

$$\beta = 2.6$$

$$K_{fe} = \begin{cases} 16 & \text{at } 50 \text{ kHz} \\ 40 & \text{at } 100 \text{ kHz} \end{cases} \quad \text{at } 60^\circ\text{C}$$

with $A_c \ell_m$ expressed in cm^3
B_{ac} expressed in Tesla
P_{fe} expressed in watts



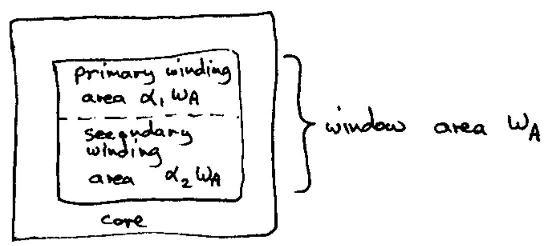


so use lots of turns to decrease core loss.

Problem: increasing n_1 increases resistances of windings
$\Rightarrow$ copper loss increases

need more turns of smaller wire for windings

Resistance of windings



$\alpha_1 + \alpha_2 = 1$

α_1 = fraction of W_A allocated to primary

α_2 = fraction of W_A allocated to secondary

Wire areas

Primary wire area $A_{w1} = \dfrac{\alpha_1 K_u W_A}{n_1}$

Secondary wire area $A_{w2} = \dfrac{\alpha_2 K_u W_A}{n_2}$

note turns ratio $n = \frac{n_2}{n_1}$ is given

Winding resistances

Primary winding resistance $R_1 = \rho \dfrac{n_1 (MLT)}{A_{w1}}$

Secondary winding resistance $R_2 = \rho \dfrac{n_2 (MLT)}{A_{w2}}$

Copper loss

primary winding copper loss $P_{cu1} = I_{1,rms}^2 R_1$

Secondary winding copper loss $P_{cu2} = I_{2,rms}^2 R_2$

total copper loss $P_{cu} = P_{cu1} + P_{cu2}$

Note: carefully sketch the winding current waveforms $i_1(t)$ and $i_2(t)$, then compute their RMS values!

Copper loss vs. n_1:

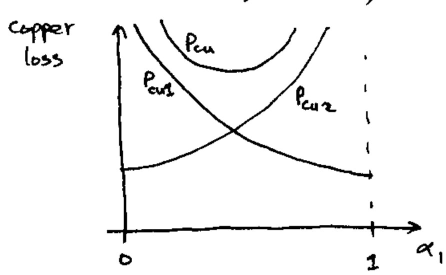
$$P_{cu} = P_{cu1} + P_{cu2} = I_{1,rms}^2 R_1 + I_{2,rms}^2 R_2$$

$$= I_{1,rms}^2 \rho \frac{n_1^2 (MLT)}{\alpha_1 K_u W_A} + I_{2,rms}^2 \rho \frac{(n n_1)^2 (MLT)}{\alpha_2 K_u W_A}$$

$$= \rho \frac{n_1^2 (MLT)}{K_u W_A} \left(\frac{I_{1,rms}^2}{\alpha_1} + \frac{n^2 I_{2,rms}^2}{\alpha_2} \right) \qquad \text{with } \alpha_2 = 1 - \alpha_1$$

- increasing n_1 increases copper loss
- there is a value of n_1 that minimizes total loss
- Minimum copper loss occurs when window area is allocated as follows:

$$\alpha_1 = \frac{I_{1,rms}}{I_{1,rms} + n I_{2,rms}}, \qquad \alpha_2 = \frac{n I_{2,rms}}{I_{1,rms} + n I_{2,rms}}$$

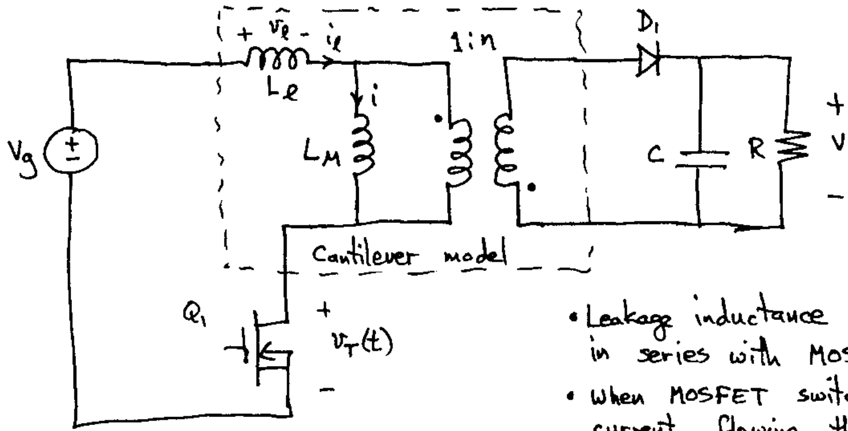


A spreadsheet design approach

- Choose α_1 and α_2 as above
- For a trial value of n_1, compute P_{fe}, P_{cu1}, P_{cu2}, and P_{tot} using above formulas
- Try different values of n_1 until P_{tot} is minimized
- Then compute wire sizes, gap length, etc.

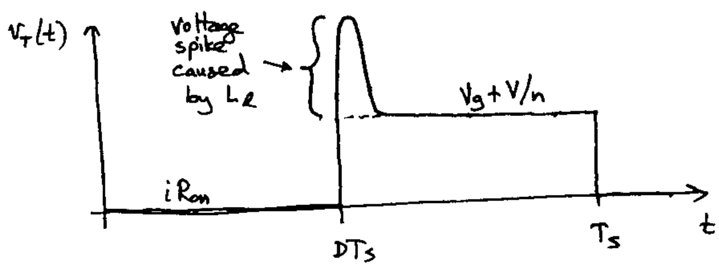
Effect of transformer leakage inductance

Voltage clamp snubber



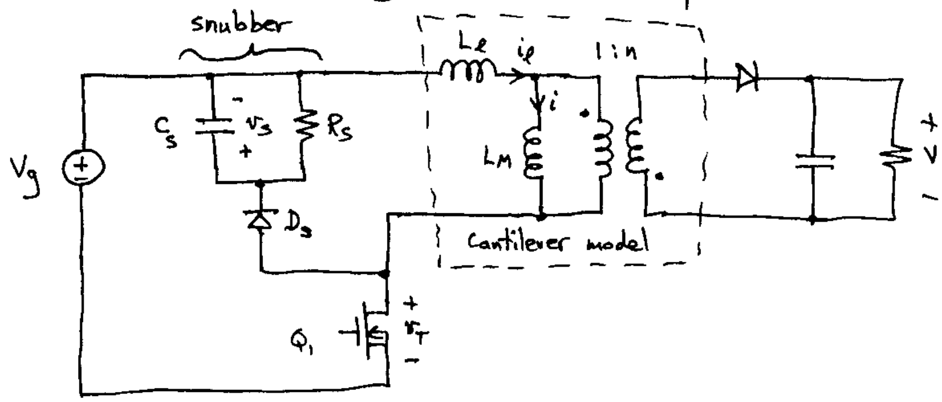
- Leakage inductance L_ℓ is effectively in series with MOSFET Q_1
- When MOSFET switches off, it interrupts current flowing through L_ℓ
- L_ℓ induces voltage spike according to $v_\ell(t) = L_\ell \frac{di_\ell(t)}{dt}$

transistor voltage waveform:

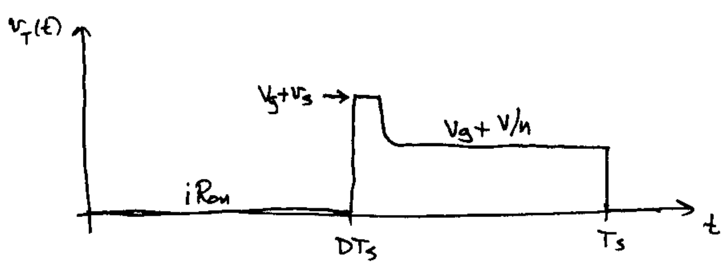


If the peak magnitude of the voltage spike exceeds the voltage rating of the MOSFET, then Q_1 will fail.

Protection of Q_1 using a voltage clamp snubber



- snubber provides a path for i_ℓ to flow after Q_1 has turned off
- energy stored in $L_\ell = \frac{1}{2} L_\ell i_\ell^2 = \frac{1}{2} L_\ell I^2$ is transferred to C_s and then is dissipated by R_s. Average power $= \frac{1}{2} L_\ell I^2 f_s$
- peak transistor voltage is clamped to $V_g + v_s > V_g + \frac{V}{n}$



<u>An approach to select R_s and C_s:</u>

- use large C_s, so that $v_s(t)$ has negligible ripple:

$$C_s \gg \frac{T_s}{R_s} \qquad \Rightarrow v_s(t) \approx V_s$$

- Voltage V_s rises until power dissipated by R_s is equal to average power transferred from L_ℓ:

$$\frac{V_s^2}{R_s} = \frac{1}{2} L_\ell I^2 f_s$$

$\Rightarrow$ choose R_s such that V_s is acceptably low

- Note that L_ℓ depends on winding geometry, and is not known until transformer is wound.

$\Rightarrow$ measure L_ℓ via short circuit test, or guess its value

<u>Example</u> – a first-pass selection of R_s and C_s

Given $V_g = 150\,V$, $V = 15\,V$, $n = 0.2$

$f_s = 100\,kHz$, $L_M = 1\,mH$ $I = 1.5\,A$

MOSFET peak voltage rating = 400V

It is desired to limit peak v_T to 325V

Estimate L_ℓ: in a good, carefully wound transformer, it may be possible to achieve $L_\ell = 3\%$ of $L_M = 30\,\mu H$

Energy stored in L_ℓ during $0 < t < DT_s$:

$$W_\ell = \frac{1}{2} L_\ell I^2 = \left(\frac{1}{2}\right)(30\,\mu H)(1.5\,A)^2 = 33.75\,\mu J$$

Average power transferred from L_ℓ to snubber:

$$P_\ell = W_\ell f_s = (33.75\,\mu J)(100\,kHz) = 3.375\,W$$

To limit peak v_T to 325V, we need

$$V_s = (\text{peak } v_T) - V_g = 325 - 150 = 175\,V$$

So choose

$$R_s = \frac{V_s^2}{P_\ell} = \frac{(175)^2}{(3.375\,W)} = 9074\,\Omega$$

we might use a $10\,k\Omega$, 5W resistor. Then

$$C_s \gg \frac{T_s}{R_s} = \frac{(10\,\mu s)}{(10\,k\Omega)} = 1\,nF$$

A good choice might be $C_s = 47\,nF$, 250V.

The above calculations are based on the estimate $L_\ell = 3\%$ of L_M, and should be considered first-pass estimates.