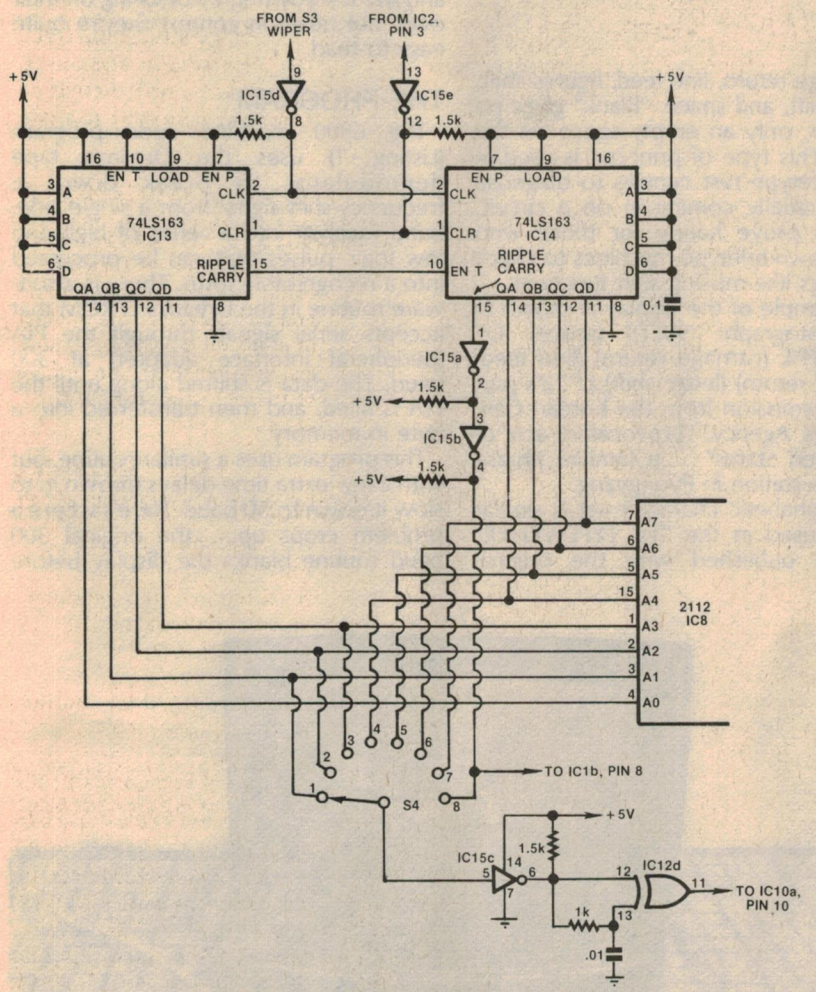
Digital Storage CRO Adapter: Addenda

A shortcoming in the design for the Digital Storage CRO Adapter described in the November issue has been brought to our attention. Due to propagation delays in the 4040 ripple counter, there could be addressing errors in the memory when used at high clocking rates. To alleviate this problem, we have produced an alternative circuit.

The changes involve replacement of the 4040 with two four-bit synchronous counters, IC13 and IC14, and an open collector inverter package, IC15. The two counters are connected to count synchronously by connecting the ripple carry output from IC13 to the "T enable" of IC14. The ripple carry output from IC14 gives the "end of memory" signal. The double inversion of this signal with IC15a and IC15b provides drive for the CMOS input, pin 8 of IC1b.



Similarly a buffer is required for the input to IC12d, connected between the wiper of S4 and pin 12 of IC12d. Note that the address outputs to S4 have been changed from the original circuit to comply with the front panel artwork of the Digital Storage CRO Adapter. The change involves moving all the switch contacts to one address bit higher with respect to the address counter. The least significant bit, A0, is now not connected to the switch and the most significant bit to the switch is now the ripple carry output signal from IC14, via the inverters, indicating the start and finish of memory.

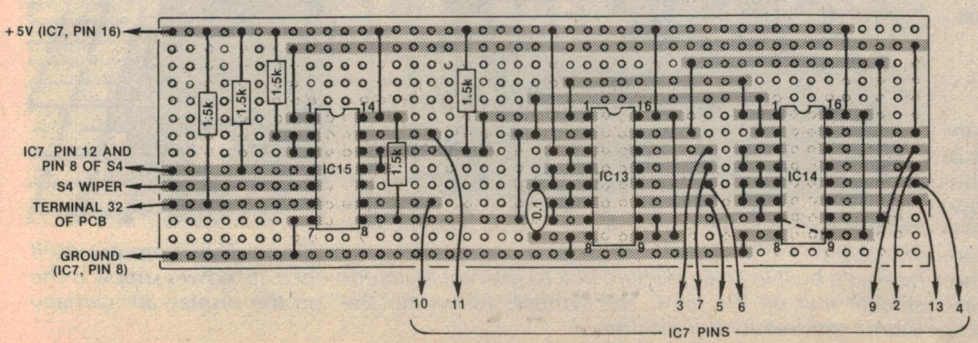
Two alternatives are available to enable the conversion. Firstly a Veroboard lashup containing IC13, IC14 and IC15 can be wired to the IC pads where IC7 is located. Alternatively, a new PC board coded 81dc2b having identical dimensions to the 80dc10 board originally used will be available, and more details on this PC board will be published in a coming issue.

The Veroboard version has dimensions 115 x 40mm. Follow the overlay provided to aid you in the layout of components. Links of non-insulated wire make the interconnections that the veroboard tracks cannot provide. Breaks in the veroboard tracks can be achieved with a small sharp drill and twisted by hand at the positions indicated.

To wire the Veroboard to the PC board, it will be necessary to refer to the article of the November 1980 issue, in particular the PC board overlay and circuit diagram.

Most of the wiring from the Veroboard goes to the IC7 pads on the PC board with the exception of IC15c which is inserted between the wiper of S4 and pad number 32 of the PC board. Remove the wire from pad 32 on the PC board going to the wiper of S4. The wiper of S4 goes to IC15c pin 5 and pin 6 to pad 32 of the PC board.

Wires to pads 33 to 40 on the PC board should be removed and rewired such that wire 40 on S4 goes to pad 39 on the PC board; wire 39 to pad 38; 38 to 37; 37 to 36; 36 to 35; 35 to 34; 34 to 33; and wire 33 on S4 to IC15b pin 4.



Above left is the revised memory address counter while at left is the suggested Veroboard layout which can be wired to the existing PC board.