distance between the control head and video heads is different for the two machines, the playback signals will not be synchronized, even though the servo is locked to the CTL signal. This condition can be corrected by physically moving the control/audio head stack in relation to the scanner. (That is one of the recommended service adjustment procedures for some VCRs.) However, it is far more practical for the user to operate a front-panel tracking control.

1-8.9 Typical Overall Functions of Beta VCR System Control Circuits

The system control circuits are not identical for all Beta VCRs. In fact, this is an area where one model of VCR can be quite different from other models. However, most system control circuits have some basic functions in common.

First, the system control circuits coordinate operation of all other VCR circuits during the various operating modes. For example, the system control circuits provide the necessary voltages and signals to keep both the tape and scanner moving during normal record and playback operations, but stop tape movement when the pause operating mode is selected. Since all VCRs do not have the same operating modes, it is not practical to generalize on the functions of the system control circuits.

Another major function of the system control circuits is to provide a fail-safe function that stops operation of the VCR in case of failure, as well as at both ends of the cassette tape. Typical failures that stop operation of the VCR include slack tape, excessive moisture on the tape, prolonged operation in the pause mode, and failure of the drum to rotate.

Most system control circuits also provide the control signals for muting audio and video circuits during fast-forward and fast-rewind operating modes. In Beta VCRs, muting also occurs when there is no CTL signal during playback. This produces a blank picture instead of snow when a blank cassette is played back or at the end of a recording. In Chapter 3 we describe operation for the system control circuits of Beta VCRs in much greater detail.

1-9 INTRODUCTION TO THE VHS SYSTEM

Now that we have reviewed Beta VCRs, let us go into similar detail on the VHS system. There are many similarities between the two systems. In this section we concentrate on the differences between the two. Again, note that the circuit descriptions here are general in nature. We go into much more detailed VHS functions in Chapter 4.

The VHS system also uses high-density recording to get the maximum amount of program information on a given amount of tape. This involves *zero guard band recording* and results in the crosstalk problem described in Sec. 1-8.3. The VHS system also uses *azimuth recording* and *phase inversion* to

minimize the effects of crosstalk. The azimuth recording used for VHS is similar to that for Beta. However, VHS uses a ±6° azimuth difference (resulting in a 12° difference between head A and head B) rather than the ±7° for Beta. Also, VHS records the chroma or color information at 629 kHz rather than the 688 kHz for Beta. The 629 kHz is obtained by mixing the incoming 3.58-MHz chroma signal with a 4.2-MHz reference signal, which is phase-inverted and locked to the incoming H-sync signal. Note that 629 kHz is 40 times the H-sync frequency of 15,750 Hz (actually 15,734.26 Hz during a color broadcast).

The phase-inversion system used in VHS is entirely different from that in Beta. In the simplest of terms, the phase of the 629-kHz color signal being recorded on head A is advanced in phase in increments of 90° at each successive horizontal line. At the end of four lines, the 629-kHz signal is back to original phase. For example, lines 1, 2, 3, and 4 are shifted 0°, +90°, +180°, and +270° in succession. When head B is recording, the 629-kHz color signal is shifted in phase (retarded) in the opposite direction (0°, 270°, 180°, 90°). This results in the following pattern:

Line	1	2	3	4	5	6
Head A	0°	90°	180°	270°	0°	90°
Head B	0°	270°	180°	90°	0°	270°

Thus, recorded phase shifts for odd-number lines (1, 3, 5) are the same, but are opposite for even-number lines (2, 4, 6).

When the 629-kHz color signal is played back, the 4.2-MHz signal is again phase inverted, and mixed with the 629-kHz signal to restore the 3.58-MHz chroma signal. When both the playback 629-kHz and reference 4.2-kHz signals are phase shifted in the same direction, the effect in the mixer is to restore the 3.58-MHz signal to its normal phase. When the playback 629 kHz and reference 4.2 MHz are phase shifted in opposite directions, the phase of the 3.58-MHz chroma signal is reversed from normal. Thus, the phase of the restored 3.58-MHz signal is shifted on every other line. As discussed in Sec. 1-8.3, when such a signal is passed through a 1H delay line (Fig. 1-29), the crosstalk component is canceled out, and the normal chroma signal component is double in amplitude.

1-9.1 Typical Luminance Circuit Operation of a VHS VCR during Record

Figure 1-41 is a block diagram showing luminance (Y) signal flow in a VHS system during record. This illustration is also referenced in Chapter 4.

The video signal from the VIDEO IN terminal is fed to LPF (low-pass filter) 2F4, where the 3.58-MHz color signal is attenuated and the video fed to the AGC circuit Q201 and Q202. The AGC circuit serves to keep the output level constant at all times regardless of input-level variations. The video signal subject

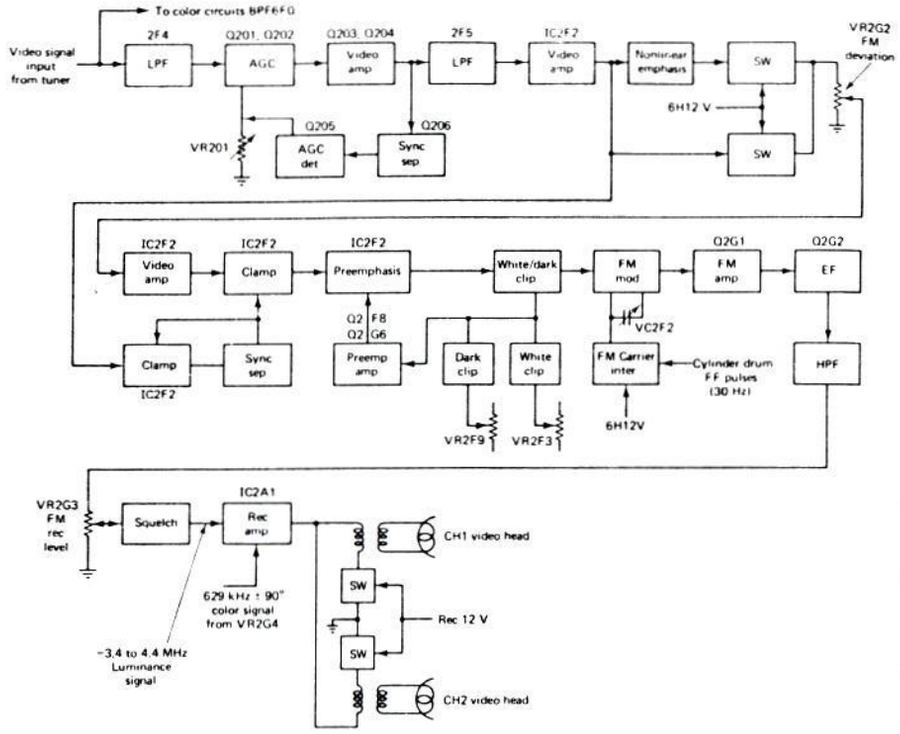


FIGURE 1-41. Luminance (Y) signal flow in a VHS system during record.

to AGC is amplified by the video amplifier Q203 and Q204, and fed to LPF2F5. Low-pass filter 2F5 serves as a 3.58-MHz trap which removes the color signal completely. A pure video signal is amplified by video amplifier IC2F2 and is fed to the nonlinear emphasis circuit. This circuit (Q2H1–Q2H5 and D2F6–D2F7) emphasizes the luminance signal frequencies by different amounts, depending on playing time (2 hours or 6 hours). The selection of frequency emphasis is made by a pulse 6H12V from Q402 applied to the switches.

The output of the nonlinear emphasis circuit is applied through VR2G2, which sets the level of FM modulation. Note that the nonlinear emphasis network is completely bypassed on the 2-hour playing mode. In any mode, the signal from the nonlinear emphasis circuit is amplified by the video amplifier (part of IC2F2) and is fed to a clamp circuit where the d-c voltage of the video sync tip remains constant regardless of the fluction in the video signal. This keeps the sync tip at 3.4 MHz (as shown in Fig. 1-24 and described in Sec. 1-7).

The clamped signal is fed to the preemphasis network, where the high-frequency spectrum is emphasized to improve the signal-to-noise ratio in FM modulation. This preemphasis of high frequencies is necessary to reduce noise.

In FM, the higher the modulated frequency, the more liable it is to be influenced by noise.

The preemphasized video signal causes a sharp overshoot at the rise and fall of the video signal. If such a signal were fed directly to the FM modulator, the frequency deviation would be excessive at the rise and fall, and overmodulation would result. Overmodulation could cause a *reverse phenomenon* (or *negative picture),* and will cause a poor S/N ratio. The white and dark clip circuits are included to prevent overshoot above a specified level.

The white and dark clip circuits are set to the correct level by VR2F3 and VR2F9, respectively. Output from the white and dark clip circuits is applied to the FM modulator, which is designed to operate at 3.4 MHz for the sync tips and 4.4 MHz for the white peaks. The FM modulator also receives 30-Hz pulses from the FM carrier interleaving circuits. These circuits are similar to the $\frac{1}{2}$fH carrier shift circuits described for the Beta system in Sec. 1-8.6. As discussed, there is a possibility of hetrodyning due to crosstalk between adjacent tracks during playback. The carrier interleaving circuits advance the video signal phase by $\frac{1}{2}$fH for the channel 2 track. (Note that in some VCR service literature, the heads and tracks are referred to as A and B, whereas the terms "channel 1" and "channel 2" are used to identify the heads and tracks in other literature.)

The FM luminance signal is amplified by the FM amplifier and passed through an emitter follower and high-pass filter. The HPF attenuates the lower end of the FM signal so as not to interfere with the 629-kHz chroma signal that is added later in the signal path. The output of the HPF is applied to squelch circuit through VR2G3, which sets the level of FM modulation.

The squelch circuit serves to prevent the signal from being fed to the record amplifier for about 1.5 s after completion of cassette loading. This prevents the recorded signal from being erased if the tape runs near the drum in a transient tape running condition (in the middle of loading). The signal passing through the squelch circuit is amplified by the record amplifier to the optimum recording level and is supplied to the video heads through a rotary transformer, to be recorded on the tape. Note that the record amplifier also receives the 629-kHz chroma signal from the color recording system, as described in Sec. 1-9.3.

1-9.2 *Typical Luminance Circuit Operation of a VHS VCR during Playback*

Figure 1-42 is a block diagram showing luminance (Y) signal flow in a VHS system during playback. This illustration is also referenced in Chapter 4.

The reproduced signal from the video heads for channel 1 and channel 2 is supplied to the preamplifier IC2A0 separated for each channel through the rotary transformer. Switch circuit IC2A0 processes the signals from the two channels and removes any overlap to provide a composite signal output. This signal is amplified by mixer amplifier IC2A0 and applied to video amplifier cir-

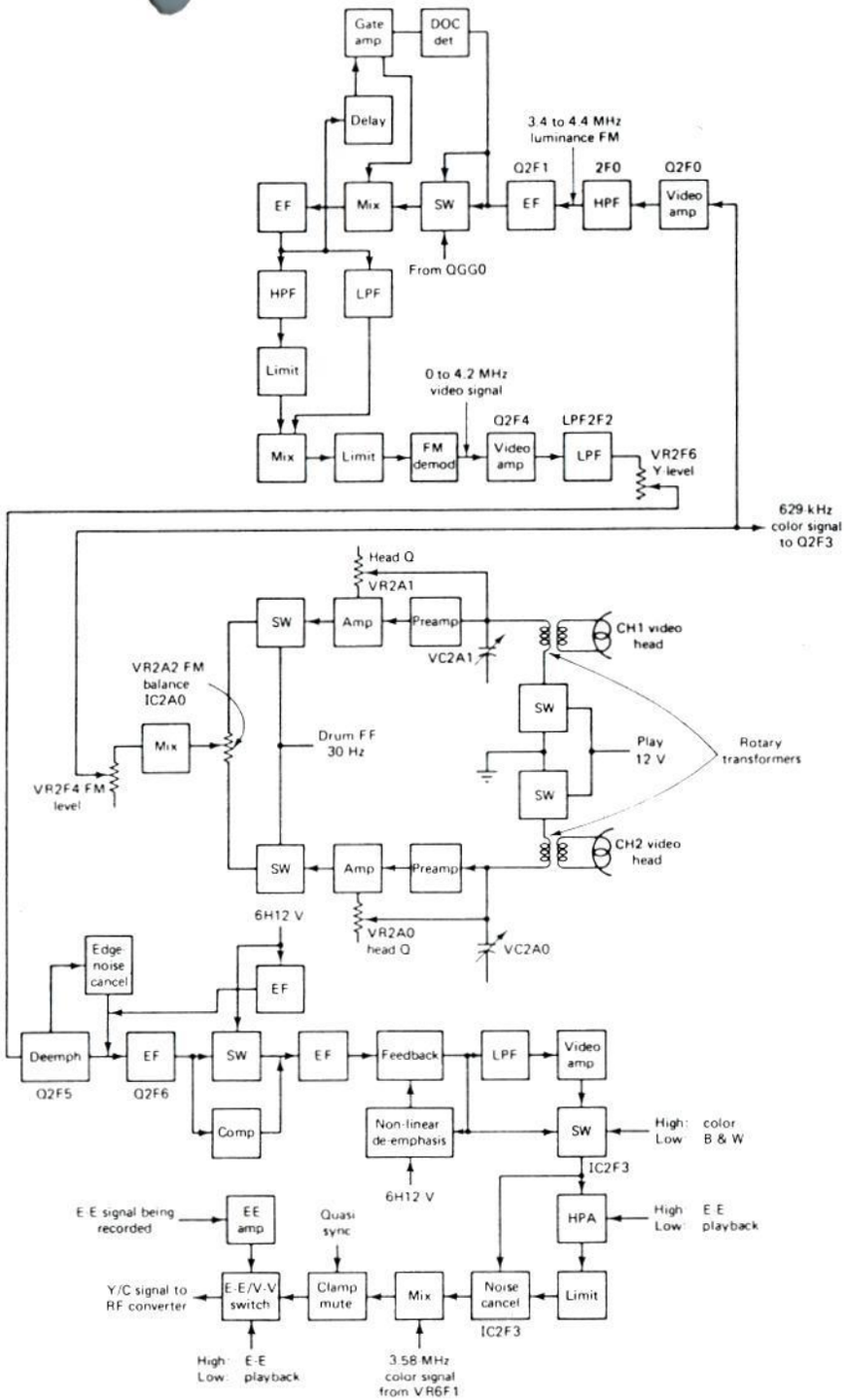


FIGURE 1-42. Luminance (Y) signal flow in a VHS system during playback.

cuit Q2F0 through the FM level adjust VR2F4. The reproduced signal is also made available to the color circuits (Sec. 1-9.4) from VR2F4. After being amplified, the signal is passed through HPF2F0 to extract only the luminance (Y) FM signal and applied to a dropout compensation circuit consisting of a mixer amplifier, 1H delay line, a gate amplifier, a DOC, and a detector. This circuit prevents deterioration of picture quality by supplying a 1H preceding signal through the 1H delay line if the FM signal is partially missed (drop out) due to a flaw in the magnetic tape, excessive dirt, and so on. The dropout circuit also provides a pulse to the AFC circuits (Sec. 1-9.6).

The FM signal is then fed to a double limiter circuit consisting of a high-pass filter, first limiter, low-pass filter, mixer amplifier, and second limiter. This circuit removes the AM components in the FM signal. The signal is then fed to the FM demodulation circuit, which uses a delay-line type of phase detection. The demodulated signal is amplified and impedance matched by video amplifier Q2F4, and only the video signal is derived from the low-pass filter LPF2F2. The video signal is compensated in frequency response (reverse to the response of preemphasis at recording as described in Sec. 1-9.1) by deemphasis circuit Q2F5. An edge-noise canceler then removes noise from the signal. The video signal is then applied to a compensator circuit through emitter follower Q2F6.

During the 6-hour playing mode, the compensator together with the nonlinear deemphasis and feedback amplifier return the nonlinear emphasis which was supplied during record by the nonlinear emphasis circuit (Sec. 1-9.1). The output of the feedback amplifier is applied to a video amplifier through a low-pass filter (during a color broadcast). For black and white, the low-pass filter is bypassed by action of the color/black and white switch in IC2F3. The low-pass filter is used to remove noise which may arise where the video signal overlaps the demodulated chroma signal.

The signal transmitted through the color/black and white switch circuit is sent to the noise cancel circuit of IC2F3. The noise cancel circuit suppresses pulse noise contained in the video signal. The luminance (Y) and chroma (C) signals are combined in the Y/C mixer circuit, and then applied to E-E/V-V switch circuit through the clamp mute circuit. The output of the E-E/V-V switch is applied to the RF unit, where the NTSC signal is converted to a television broadcast frequency signal (channel 3 or 4). The E-E amplifier and E-E/V-V switch combination permits a signal being recorded to be monitored on a TV set if desired (as discussed in Sec. 1-8.6).

1-9.3 *Typical Color Circuit Operation of a VHS VCR during Record*

Figure 1-43 is a block diagram showing chroma (C) signal flow in a VHS system during record. This illustration is also referenced in Chapter 4.

The video signal from the VIDEO IN terminal is passed through bandpass filter Q6F0 to remove only the chroma signal (3.58 MHz ± 500 Hz), which is

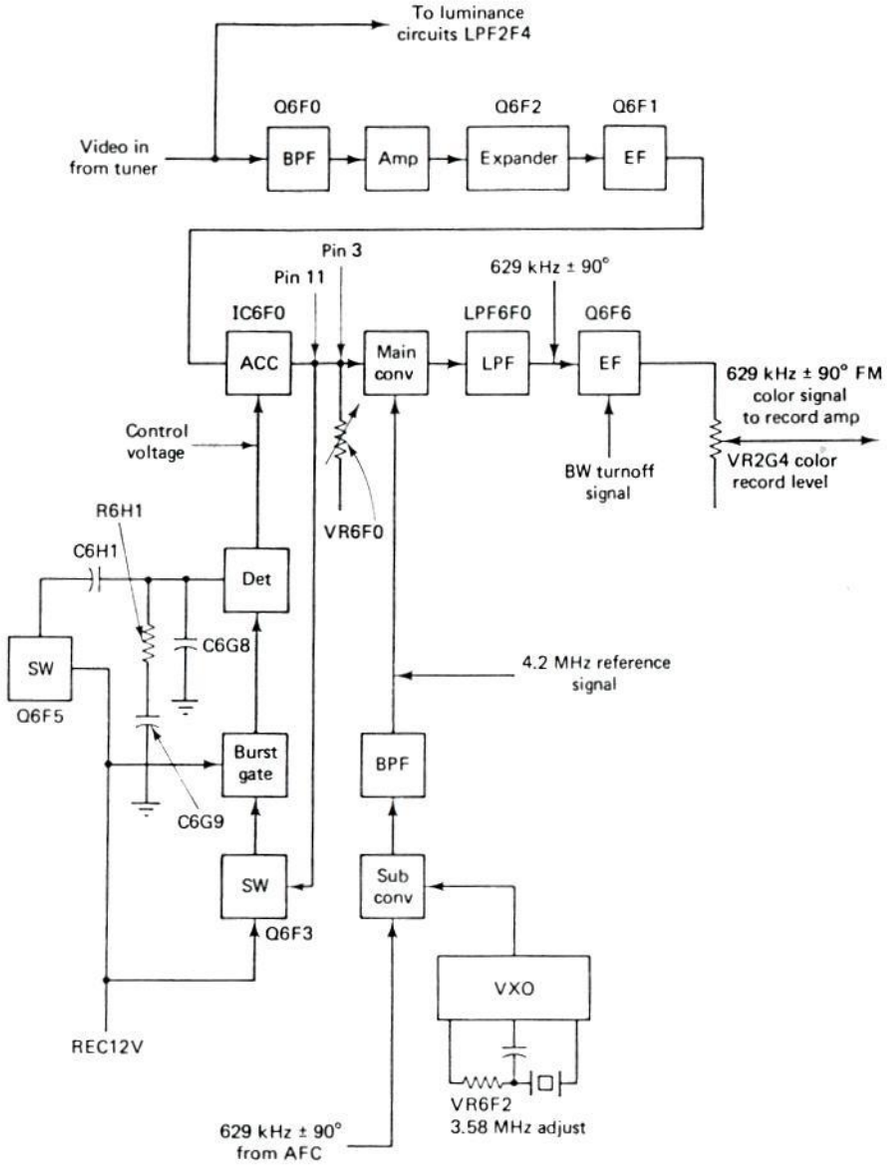


FIGURE 1-43. Chroma (C) signal flow in a VHS system during record.

amplified by Q6F0. The color signal is then fed to the expander Q6F2 to boost the burst signal by 6 dB. The burst is fed to the automatic color control (ACC) circuit through impedance-matching emitter follower Q6F1.

The signal at pin 11 of IC6F0 is applied to the color control detector circuit through switch Q6F3 and a burst gate circuit. The peak of the color signal is

detected in the detector circuit and produces a control voltage which is applied to the ACC circuit. This detected voltage controls the ACC so as to maintain the color signal at a certain voltage level. The color signal is then applied to the main converter where it is mixed with a reference signal to produce the desired 629 kHz for recording on tape (together with the luminance signal as described in Sec. 1-9.1).

The reference signal applied to the main converter is developed by mixing a 3.58-MHz signal from the VXO (variable crystal oscillator) and a 629-kHz ± 90° signal from the AFC circuit (described in Sec. 1-9.6). Note that the term "± 90°" applied to a signal means that the signal has been rotated or shifted in phase every 1H period as described in the introduction to Sec. 1-9. The 3.58-MHz VXO signal and 629-kHz signals are combined in the subconverter to produce a 4.2-MHz signal. This 4.2-MHz signal is passed through a bandpass filter to the main converter, where the signal is combined with the 3.58-MHz chroma signal to produce a 629-kHz ± 90° signal. The resultant signal is then fed to the record amplifier (together with the luminance signal, Sec. 1-9.1) through a low-pass filter, emitter follower, and color record level control VR2G4.

1-9.4 *Typical Color Circuit Operation of a VHS VCR during Playback*

Figure 1-44 is a block diagram showing chroma (C) signal flow in a VHS system during playback. This illustration is also referenced in Chapter 4.

The reproduced signal from IC2F0, applied through the FM level adjust VR2F4 (Sec. 1-9.2), is amplified by Q2F3. At this point, the signal contains both luminance and chroma. Only the 629-kHz ± 90° chroma signal is passed by low-pass filter LPF2F0. This chroma signal is amplified by Q6F0 and applied to the ACC circuit through impedance-matching emitter follower Q6F1.

The chroma signal is maintained at a constant level by the ACC circuit, and is mixed with a 4.2-MHz ± 90° signal from the APC circuit (Sec. 1-9.5) in the main converter. The resultant 3.58-MHz signal is amplified by Q6F7 after being passed by the bandpass filter BPF6F1.

The compressor circuit operates whenever there is a burst gate pulse to reduce gain in amplifier Q6F7. This is necessary to restore the burst signal to a normal level at playback. As discussed in Sec. 1-9.3, the burst signal is increased in amplitude by about 6 dB during record.

The restored chroma signal is passed through a 1H delay line to remove crosstalk from the neighboring video track, as discussed in the introduction to Sec. 1-9. The 1H delay line output is amplified by IC6F1 and is fed to the killer amplifier of IC6F0. This killer amplifier is a switch circuit which allows the signal to pass only when there is a color signal carrier present in the video signal. When the playback is black and white (no color carrier), the color killer prevents a color signal from being applied to color out control VR6F1. This function eliminates noise components from the chroma circuit being applied during a black-and-

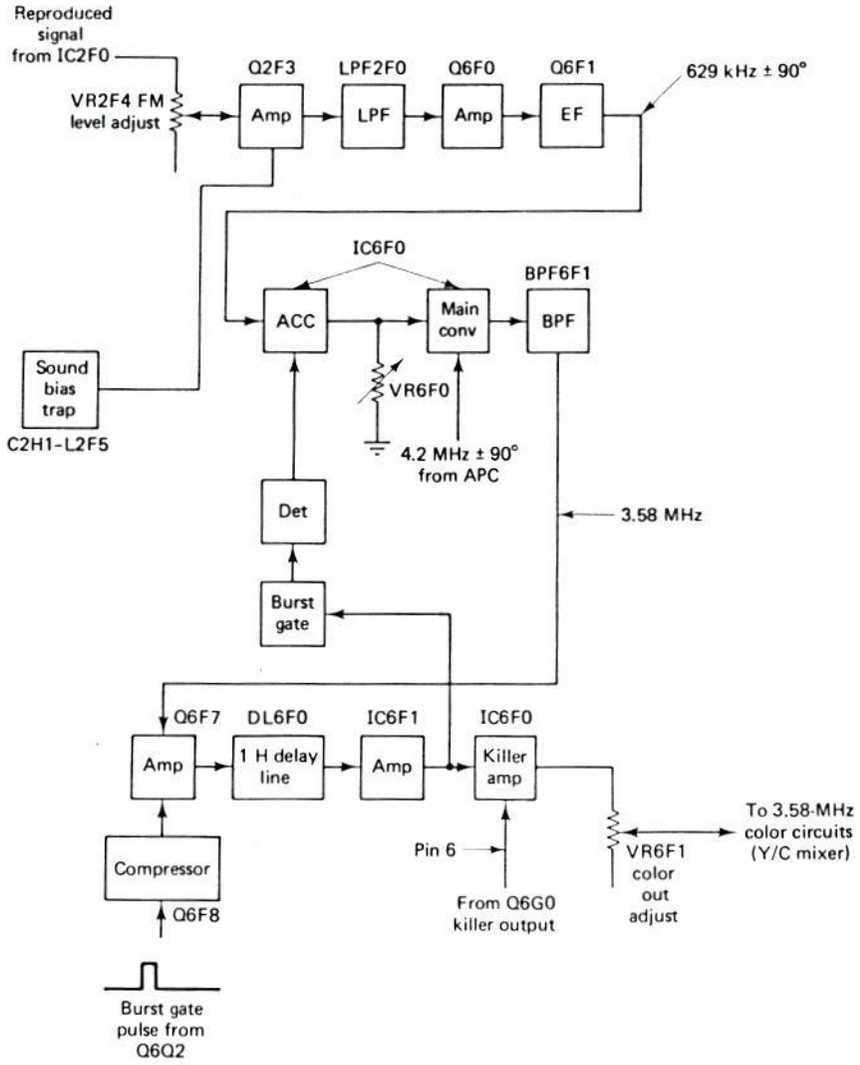


FIGURE 1-44. Chroma (C) signal flow in a VHS system during playback.

white playback. The color killer circuit is operated by signals from Q6G0. When pin 6 of IC6F0 is high, the color signal passes through VR6F1 and is superimposed on the luminance (Y) signal (as discussed in Sec. 1-9.2).

1-9.5 Typical APC Circuit Operation of a VHS VCR

Figure 1-45 is a block diagram showing operation of the APC (automatic phase control) circuit during record and playback. This illustration is also referenced in Chapter 4.

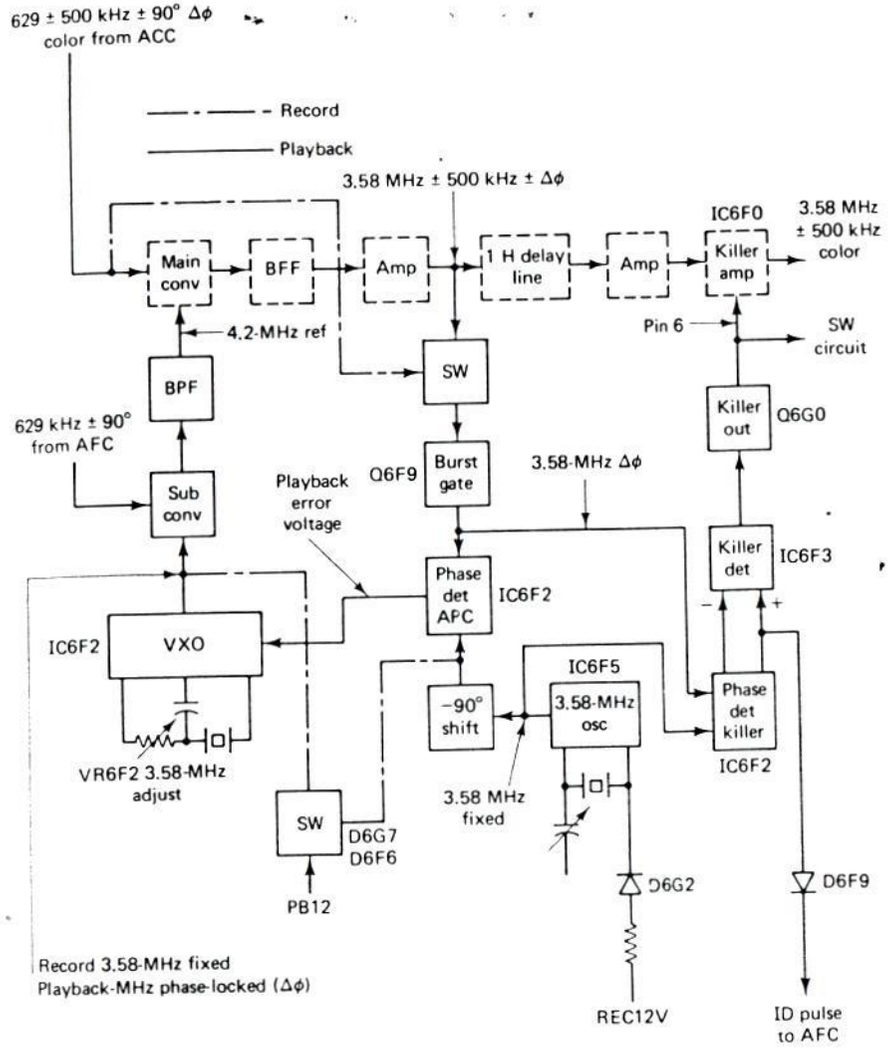


FIGURE 1-45. Typical APC circuit operation.

During record, the VXO IC6F2 operates as a fixed 3.58-MHz oscillator. The output of the VXO is mixed with the 629-kHz ± 90° signal from the AFC circuit (Sec. 1-9.6) in the subconverter to form a 4.2-MHz reference voltage, as discussed in Sec. 1-9.3. The VXO output is also applied to the phase detector killer IC6F2 through diode switches D6G6 and D6G7.

During playback, the VXO operates as a phase-locked 3.58-MHz oscillator. The phase of the VXO is controlled by an error voltage from the phase detector APC IC6F2. This phase detector receives and compares two 3.58-MHz inputs. One input is the playback color burst (which includes any phase shifts due to jitter), while the other input is from a fixed 3.58-MHz oscillator IC6F5. If

there are any phase differences between the two signals, the error voltage produced by the phase detector shifts the phase of the VXO to correct the condition. Since the phase of the playback color burst is controlled by the VXO, any phase shift in the playback 3.58-MHz color signal is eliminated.

Note that the term "$\Delta\phi$" or "delta phi" applied to a signal means that the signal has been shifted in phase or is of differing phase. In the case of the 3.58-MHz signal applied to the phase detector, the term means that the signal contains any possible jitter effect which could shift the phase.

The killer circuits shown in Fig. 1-45 have two functions. First, they prevent a color signal from being passed when the signal is black and white only (to eliminate color circuit noise from being mixed with the black-and-white signal). Second, the killer circuits provide an identification pulse (ID) which is used by the AFC circuit to prevent 180° out-of-phase lockup. This is similar to the burst ID pulse used for Beta as described in Sec. 1-8.4.

During color operation, the 3.58-MHz color burst signal is passed through the burst gating circuit Q6F9 to the phase detector killer IC6F2, which also receives a 3.58-MHz signal from either the 3.58-MHz oscillator IC5F5 (during playback) or the VXO (during record). The two signals are compared in phase by the phase detector killer. If both signals are of the same phase, the output of the killer detector IC6F3 becomes low, and the output of the killer output circuit Q6G0 becomes high. This high output is applied to pin 6 of killer amplifier IC6F0. As discussed in Sec. 1-9.4, with a high signal at pin 6 of IC6F0, the color signal is passed.

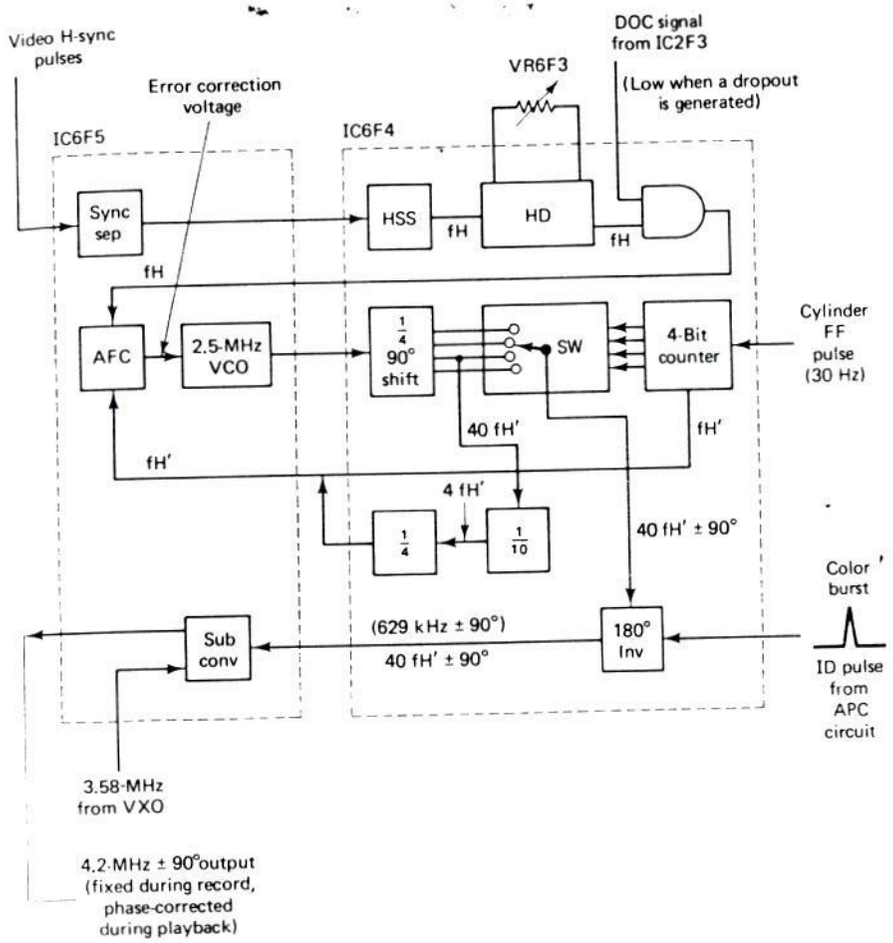
During black-and-white operation, there is no 3.58-MHz color burst signal. Therefore, the phase detector killer IC6F2 sees only one signal. The output of the killer detector IC6F3 then becomes high, and the output of the killer output circuit Q6G0 goes low. This low output at pin 6 of IC6F0 cuts off the killer amplifier and prevents passage of color signals (or color noise).

Also during color operation, if the 3.58-MHz color burst is exactly 180° out of phase with the IC6F5 3.58-MHz oscillator (locked in phase, but 180° out), the phase detector killer IC6F2 develops a burst identification pulse. This pulse is applied through D6F9 to the AFC circuits (Sec. 1-9.6).

1-9.6 Typical AFC Circuit Operation of a VHS VCR

Figure 1-46 is a block diagram showing operation of the AFC (automatic frequency control) circuit. Note that the AFC system operates in much the same way for both record and playback. However, during record, the AFC uses H-sync pulses contained in the video signal from the tuner. During playback, the AFC uses the H-sync signals recorded on tape.

The AFC system has five inputs and one output. The five inputs include the video H-sync pulses, a dropout pulse from the dropout detection circuit (Sec. 1-9.2), a 30-Hz cylinder flip-flop from the servo (Sec. 1-9.7), a color burst ID pulse from the APC circuits (Sec. 1-9.5), and a 3.58-MHz fixed or phase-



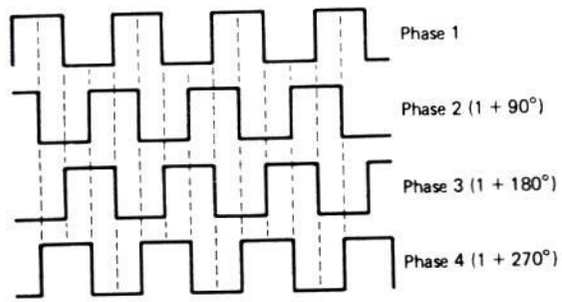


FIGURE 1-46. Operation of AFC circuit.

corrected signal from the VXO in the APC circuits. The output of the AFC circuit is a 4.2-MHz ± 90° signal (fixed reference during record, or phase corrected during playback).

The video signal (from tuner or playback) is applied to a sync separator where only the vertical and horizontal sync signals are passed. The resultant signal is then applied to the HSS (H-sync separator) where only the H-sync signal is passed. The H-sync signals (or fH as they are referred to in most VCR literature) are shaped into a 2-μsec pulse by a HD (horizontal drive) circuit. The output from the HD circuit is adjusted to exactly 2 μsec by VR6F3 and is applied to an AND gate. The other input to the AND gate is normally high so that the 2-μsec fH pulses can pass. However, if there is a dropout (Sec. 1-9.2) the other AND gate input goes low, preventing the fH pulses from passing.

The output of the AND gate is applied to an AFC circuit within IC6F5. This AFC circuit also receives a fH′ (fH prime) signal developed by a 2.5-MHz VCO (voltage-controlled oscillator). Note that the actual frequency of the 2.5-MHz oscillator is 160 times the H-sync frequency of 15,750 Hz (for black and white), or 160 times 15,734.26 Hz (for color). Note that the term "prime" applied to the signal here means that the signal has been locked in frequency to some other signal (to the H-sync signals in this case).

The 160fH′ from the VCO is divided by four into 40fH′ through operation of a $\frac{1}{4}$ 90° shift and switch circuit which is operated by a 4-bit counter. The 40fH′ output of this circuit is further divided by 10 to produce 4fH′, and by one-fourth to produce 1fH′ (or simply fH′). This fH′ is fed back to the AFC circuit. If there is any difference in frequency between the fH signal coming from the AND gate, and the fH′ signal originating at the VCO, the VCO is shifted in frequency by an error correction voltage developed in the AFC circuit. Thus, the VCO is precisely locked onto the H-sync frequency.

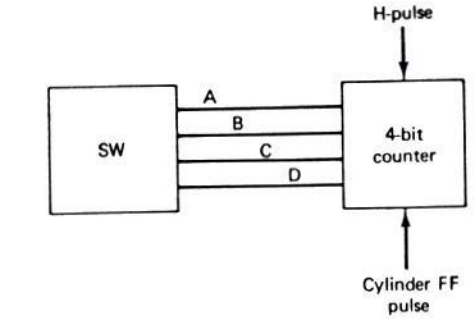
The 4-bit counter (operated by the fH′ and cylinder pulses) produces switch signals which select each of four signals from the $\frac{1}{4}$ 90° shift circuit, in sequence. Each of the four signals is shifted by 90° from the previous signal as shown. In effect, the switch can be thought of as a rotary switch where the rotational direction and speed of the rotor are determined by the 4-bit counter. The counter supplies the pulses to the switch each time an H-sync pulse is applied. As shown in Fig. 1-47, the channel 1 signals are advanced in phase by 90°, whereas the channel 2 signals are retarded or delayed in phase by 90°. These signals (40 fH′ ± 90°) are applied through the 180° inverter circuit to be mixed in the sub-converter with the 3.58-MHz signal from the VXO, and result in a 4.2-MHz ± 90° that is precisely locked to the VCO.

The 180° inverter is operated by the burst identification (ID) pulse from the APC circuit. As discussed in Sec. 1-9.5, the ID pulse occurs only when the 3.58-MHz color burst is 180° out of phase with the 3.58-MHz oscillator (locked in phase, but 180° out). The inverter normally passes the 40fH′ ± 90° signal without change. However, if the burst ID pulse is present (indicating an undesired 180° lockup) the inverter reverses the phase of the 40fH′ ± 90° signal to correct the condition.

1-9.7 Typical Overall Functions of a VHS Servo System

Figure 1-48 is the block diagram of a typical VHS servo system. The following is a brief explanation of overall operation. In Chapter 4 we describe operation for the circuit of a similar VHS VCR in much greater detail. As in the case of Beta, a VHS servo must keep the speed of the video heads constant relative to the input signal to properly record the video signal on tape. Both the *speed* and *phase* of direct-drive (DD) motors of the cylinder (containing the video heads) and the capstan (that moves the tape) must be servo controlled.

One major purpose of the servo control during record operation is to rotate



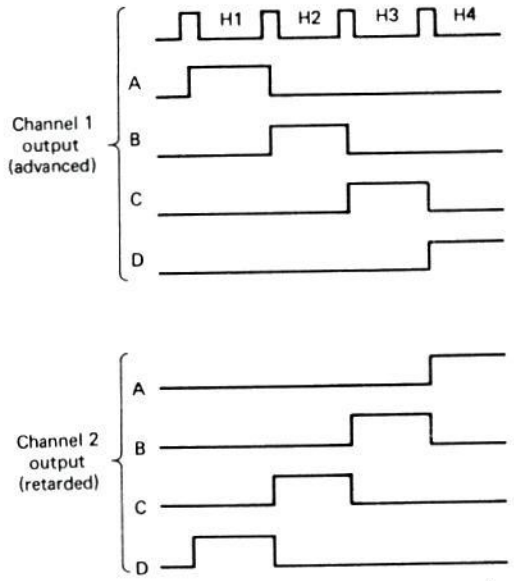
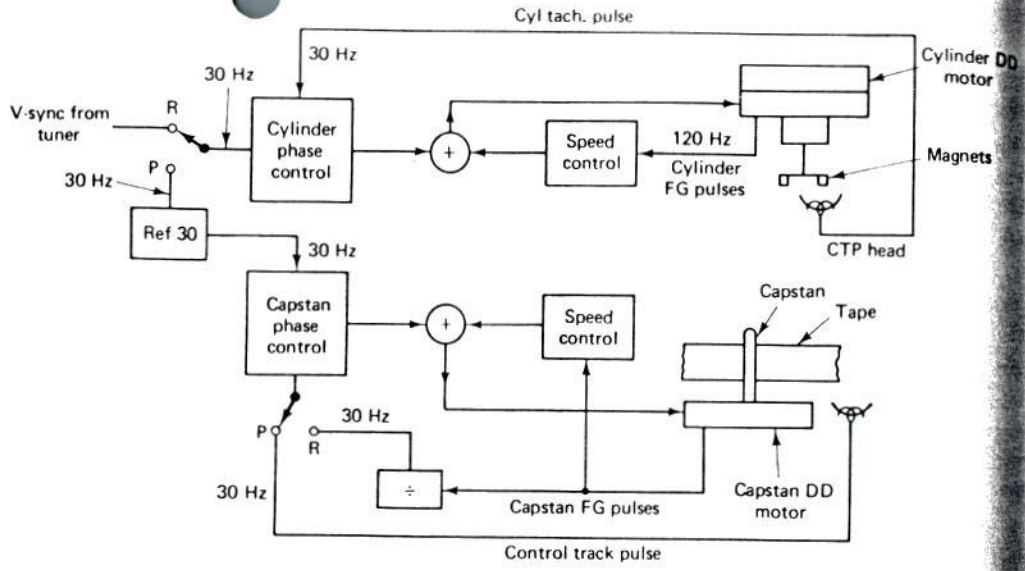


FIGURE 1-47. Operation of a 4-bit counter to advance and retard signals by 90°.



Pulse	Ferquency (Hz)	
Cylinder FG	120	
Capstan FG	SP (2 hour)	720
	LP (4 hour)	360
	EP (6 hour)	240
	Slow (slow motion)	120
	Quick (fast motion)	720
	Search	2160
Cylinder tach	30	
REF 30	30	
Control track	30	

System		Mode	Reference signal	Waveform	Comparison signal	Waveform
Phase	Cylinder	REC	$\frac{1}{2}$ V-sync	Sample pulse	Cylinder tach pulse	Trapezoid
		PB	REF 30			
	Capstan	REC	REF 30	Trapezoid	1/24 Capstan FG	Sample pulse
		PB	REF 30		Control track pulse	
Speed	Cylinder	PB/REC	Cylinder FG	Sample pulse	Cylinder FG	Sawtooth
	Capstan		Capstan FG		Capstan FG	

FIGURE 1-48. Typical VHS servo system.

the cylinder at precisely 30 Hz, which is one-half the vertical sync frequency (60 Hz) of the input video signal. With this speed, the vertical blanking period can be recorded at any desired point on each video track. In television, the vertical blanking occurs at the bottom of the screen, where it will not interfere with the picture. For this reason, the vertical sync signal is recorded at the bottom (or start) of each video track. This is shown in Fig. 1-49, which is the typical magnetic tape pattern used in VHS.

As in the case of Beta, there are two heads (channel 1 and channel 2) and each head traces one track for each field. Two adjacent tracks or fields make up one complete frame. To ensure that there are no nonimage or blanks in the picture, the information recorded on tape overlaps at the changeover point (from one head to another). This changeover point must also occur at the bottom of the screen, where it will not interfere with the picture. For that reason the vertical sync signal is recorded precisely in the position 6.5H from the changeover time of the channel 1 and channel 2 tracks.

This precise timing requires that the speed and phase of both the cylinder motor and capstan motor be controlled (since the cylinder motor determines the position of the heads at any given instant, while the capstan motor determines the position of the tape). In the servo system of Fig. 1-48, five separate signals are used to achieve the precise timing. The following paragraphs describe each of these signals and how (in general terms) they are used. The tables of Fig. 1-48 summarize the signal functions.

Cylinder FG Pulses. As shown in Fig. 1-48, the cylinder FG pulses are developed by a generator in the video head cylinder. The generator consists of an eight-pole magnet installed in the cylinder rotor, and a detection coil in the stator. When the cylinder rotates at 30 rps, the stator coil detects the moving magnetic fields and produces the cylinder FG pulses at a frequency of 120 Hz.

Capstan FG Pulses. The capstan FG pulses are developed by a generator in the tape capstan and are applied to the capstan speed control circuits, as well as the capstan phase control circuits (through a divider) during record. The

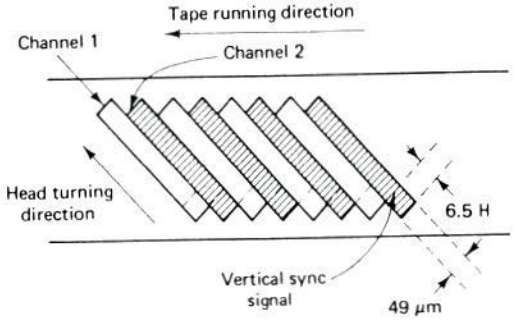


FIGURE 1-49. Typical magnetic tape pattern used in VHS.

generator consists of a 240-pole magnet installed in the lower part of the capstan shaft, and a detection coil in the stator. When the capstan rotates, the stator coil detects the moving magnetic fields and produces the capstan FG pulses. The frequency of the capstan FG pulses depends on the speed of the capstan (which also controls tape speed). The tables of Fig. 1-48 show some typical capstan FG pulse frequencies for various playing times and tape speeds. Note that not all VHS machines are capable of the six play modes or tape speeds shown in Fig. 1-48.

Cylinder Tach Pulse. The cylinder tach pulses (CTP) are developed by another generator in the cylinder and are applied to the cylinder phase control circuits. The generator consists of a pair of magnets installed symmetrically in a disk in the lower part of the cylinder shaft, and a stationary pickup head. When the cylinder rotates, the CTP pickup head detects the moving magnetic fields. The pulse frequency is a constant 30 Hz. In effect, the tach pulse indicates video head channel switching, and is used as a comparison signal in the cylinder phase control circuits during both record and playback.

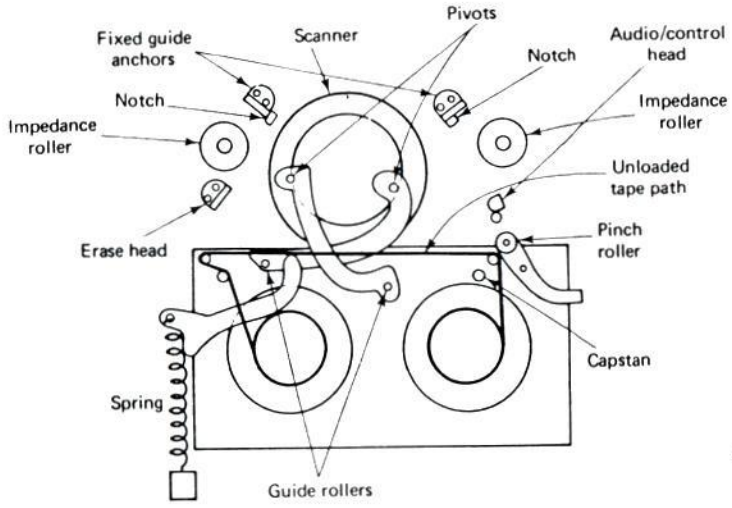
REF 30 Pulse. The reference signal for the phase control system of both the capstan motor and the cylinder motor is obtained from a crystal oscillator with a frequency of 32.765 kHz. A frequency of 30 Hz is obtained when the crystal oscillator signal is divided. The REF 30 pulse is used for the cylinder phase control circuit only during playback. During record, the cylinder phase control circuit receives broadcast V-sync pulses from the tuner.

Control Track Pulse. The 30-Hz control track pulses are the broadcast V-sync pulses recorded on tape during record. At playback, the pulses are picked up by the control head (as described for Beta, Sec. 1-8.8) and applied to the capstan phase control circuit.

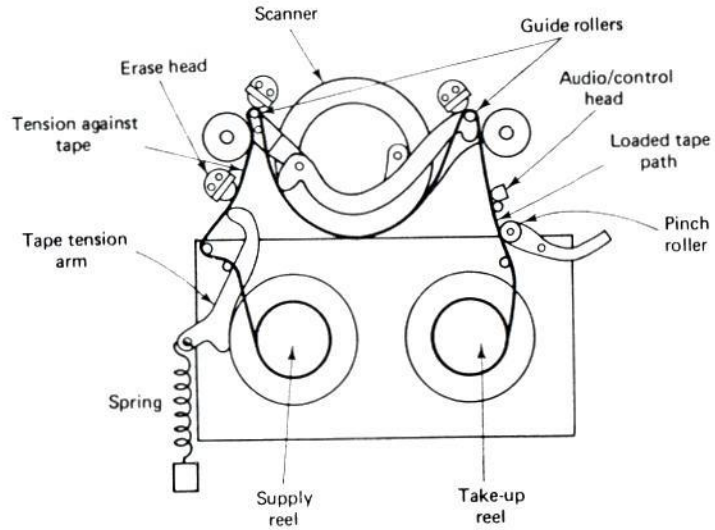
1-9.8 Tape Loading for the VHS System

The VHS tape loading system is entirely different from that used for Beta (Sec. 1-8.5). Unlike Beta, the VHS tape is not loaded automatically when the cassette compartment lid is closed. Instead, VHS loading starts when the PLAY button is pressed. Basic operation of a typical VHS tape loading system is illustrated in Fig. 1-50. As shown, the VHS system uses a so-called M loading or threading system, since the tape appears to form the letter M when fully threaded. When the cassette is dropped into place, two guide rollers, a tape tension arm, and the capstan are positioned behind the tape (between the tape and the reels). The capstan is stationary, and the two guide rollers are attached to movable arms which are pivoted below the video head scanner. The tape tension arm is spring loaded and pivots near the supply reel.

As shown in Fig. 1-50a, when the PLAY button is pressed, the two guide rollers are moved by the arms to pull the tape against the capstan and the various



(a)



(b)

FIGURE 1-50. Typical VHS tape loading system.

heads (video, audio/control, erase). The pinch roller is also pulled against the tape. Usually, the arms and pinch rollers are operated by a gear train driven by the capstan motor. The movable arms have guide pins which press into notches on fixed guide anchors when fully extended. These anchors are positioned with considerable accuracy since the guide pins and rollers form entrance and exit tape guides for the scanner.

When tape threading is complete (usually in less than 1 second), the tape tension arm is released to apply spring-loaded tension against the tape. With the tension arm in place, the tape begins to move, the arms are locked in place, and the arm gear train is disengaged from the capstan motor.

Unthreading of a VHS is initiated when the stop button is pressed. The STOP button interrupts both PLAY or RECORD functions. When the STOP mode has been selected, the arms, pinch roller, and tape tension are returned to the position shown in Fig. 1-50a. With the tape back in the cassette, FAST FORWARD and REWIND functions can be performed by pressing the appropriate buttons.

1-10 BASIC VCR OPERATING PROCEDURES AND RECORD LOCKOUT PROVISIONS

The operating procedures for VCRs are not standard. Each VCR has its own set of controls and procedures, so we will make no attempt to describe the operating procedure for any particular VCR. However, there are two operating functions in common for most VCRs. The procedures involve inserting and removing the cassette, and a *record lockout* or *malerase* provision for both Beta and VHS.

1-10.1 Inserting and Removing a Video Cassette

As shown in Fig. 1-2, both Beta and VHS cassettes are installed in the VCR from the top. To insert a cassette in a typical Beta VCR such as shown in Fig. 1-51, you must apply power to the VCR and set the POWER switch to ON. You then press the EJECT button, which automatically opens and raises the cassette compartment lid. You then install the cassette in the compartment (usually within a holder) and press down on the compartment lid. The VCR is then ready (in about 3 seconds) to perform any of the normal operations, such as RECORD, PLAYBACK, STOP, REWIND, FAST FORWARD, and so on.

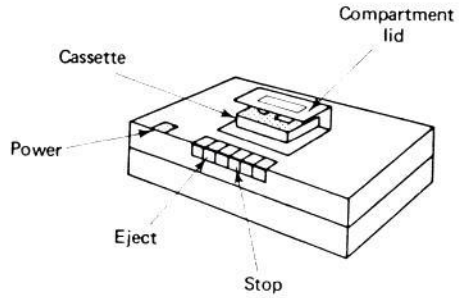


FIGURE 1-51. Inserting and removing a video cassette.

When the cassette compartment lid is pressed down, the supply and takeup reels within the cassette engage the drive mechanisms of the *supply* and *takeup drives* within the VCR. These drives are capable of operating in both directions to accommodate both playback/record and rewind functions. The supply and takeup motors are usually capable of operating at various speeds. Typically, the supply and takeup reel motors receive a low voltage during record and playback modes. This low voltage keeps tension on the tape, but the actual tape drive is provided by the capstan and pinch roller. During fast forward and rewind, the supply and takeup motors receive a higher voltage and provide the tape drive. In the case of VHS, the tape is unloaded and returned back inside the cassette when fast forward and rewind are in operation.

For Beta machines, when the lid is closed, the tape is automatically loaded as described in Sec. 1-8.5. For VHS, tape loading occurs after the lid is closed and the PLAY button is pressed as described in Sec. 1-9.8. Operation of the tape, drive motors and loading/unloading circuits is discussed further in Chapters 3, 4, and 5.

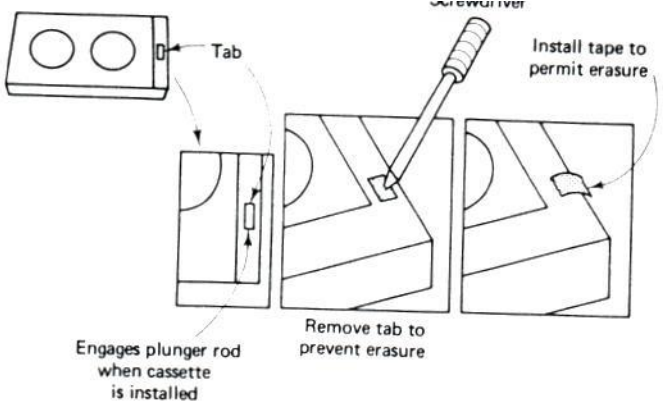
To remove a Beta cassette, make sure that the power is turned on and that the VCR is in the STOP mode. On some VCRs, the EJECT button cannot be pressed except in the STOP mode. In other VCRs, the EJECT button can be pressed but will not actuate the circuit unless the VCR is in STOP. Press EJECT, remove the cassette, and close the compartment lid. When a Beta compartment lid is raised by pressing the EJECT button, the tape is automatically unloaded as described in Sec. 1-8.5, and the cassette supply and takeup reels disengage from the tape drive motors.

For VHS, when the STOP button is depressed, the tape is unloaded. The cassette can then be removed by pressing the EJECT button to release the cassette holder.

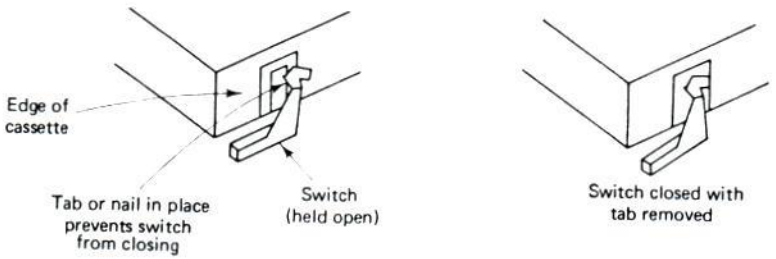
1-10.2 Record Lockout or Malerase Functions

Both Beta and VHS cassettes can be reused to record new program material many times. The erase head automatically erases all recorded material on the tape before the tape reaches the rotating video heads (Fig. 1-19). Both Beta and VHS cassettes have provisions for preventing accidental erasure of recorded material when you want to retain a particular program. These provisions are called "record lockout" or "malerase" or similar term. In a Beta VCR, the record lockout takes the form of a tab located on the bottom of the cassette, as shown in Fig. 1-52a. In VHS, a similar tab or nail is located on the edge of the cassette, as shown in Fig. 1-52b.

With either system, the tabs engage a plunger rod or switch when the



(a) Beta



(b) VHS

FIGURE 1-52. Typical record lockout or malerase function.

cassette is inserted and the compartment lid is closed. In the case of most Beta systems, the RECORD button cannot be pressed unless the rod is pushed down by the tab. In most VHS systems, the tab prevents a switch from closing (closing of the switch disables record operation). If you want to keep a recorded program from being accidentally erased, you break off the tab or nail with a screwdriver. In this way, the plunger is not pushed down (Beta) or the switch is closed (VHS), and the RECORD function is disabled.

If you wish to record on a cassette with the tab or nail removed, cover the hole with a piece of cellophane or vinyl tape. The tape will actuate the plunger rod or hold the switch open, and the RECORD function will be normal. During service, it is sometimes necessary to operate the VCR without a cassette installed (say to observe rotation of the tape drive motor). In this case you can use vinyl tape to hold the plunger rod or switch in place, just as though it was actuated by the tab or nail.

4

Typical VHS VCR Circuits

This chapter describes the theory of operation for a number of VHS VCR circuits. (Similar coverage for a cross section of Beta circuits is provided in Chapter 3.) The VHS circuits described here include video signal processing, servo, and system control. Note that the RF unit and tuner circuits are not covered. As discussed in Chapter 3, this is typical for most VCR service literature. In the case of the RF unit (and in many cases the tuner), if the unit fails, it must be replaced as a unit, preferably at a factory service facility. Since the RF unit is essentially a miniature TV broadcast station or transmitter, any improper adjustment can produce interference with normal television broadcasting.

By studying the circuits found in this chapter, you should have no difficulty in understanding the schematic and block diagrams of similar VHS VCRs. This understanding is essential for logical troubleshooting and service, no matter what type of electronic equipment is involved. No attempt has been made to duplicate the full schematics for all circuits. Such schematics are found in the service literature for the particular VCR. Instead of a full schematic, the circuit descriptions are supplemented with partial schematics and block diagrams that show such important areas as signal flow paths, input/output, adjustment controls, test points, and power source connections. These are the areas most important in service and troubleshooting. By reducing the schematics to these areas, you will find the circuit easier to understand, and you will be able to relate circuit operation to the corresponding circuit of the VCR you are servicing.

Note that, as shown in the illustrations of this chapter, many circuit parts are contained within integrated circuits which carry the reference designation of

IC. Individual transistors outside the ICs carry the designation Q. Both the ICs and transistors are mounted on printed circuit boards, carrying the reference designations PCB.

The majority of the video circuits described in this chapter are part of the Mitsubishi HS-300U. This VCR uses the conventional VHS color-under recording system described in Sec. 1-7 and the VHS high-density PI (phase inversion) described in Sec. 1-9. Note that the overall block diagrams showing video luminance and color (chroma) operation in both record and playback are given in Chapter 1 and are not duplicated here. However, the following paragraphs (which describe circuit details) make direct reference to these block diagrams in Chapter 1.

4-1 VHS LUMINANCE SIGNAL CIRCUITS DURING RECORD

Figure 1-41 is the overall block diagram of the luminance circuits used during record. Overall functions of these circuits are described in Sec. 1-9.1. The following paragraphs describe details and characteristics for some of the circuits.

4-1.1 Low-Pass Filter and AGC Circuits

The video signal coming from the VIDEO IN terminal, during a color broadcast, is first fed to the low-pass filter LPF2F4 to remove the burst signal inserted in the back porch of the horizontal sync signal. The filter characteristics are shown in Fig. 4-1. The filter impedance is 1 kΩ and the filter delay is about 0.35 μsec.

The signal passing through LPF2F4 is added to the AGC circuit, which uses a peak AGC system. The video signal from LPF2F4 passes through the AGC (Q201, Q202), and video amplifier (Q203, Q204) to LPF2F5. The video signal of the video amplifier is passed through the sync separator Q206 to extract only the signal at the AGC detector (which controls the AGC function). The peak

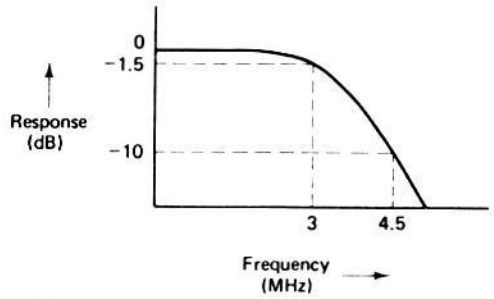


FIGURE 4-1. LPF2F4 characteristics.

AGC system uses the peak level of the sync signal to keep the amplitude of the video signal constant.

4-1.2 Low-Pass Filter and Video Amplifier Circuits

The video signal from the AGC circuit is amplified by Q203 and Q204, and applied to LPF2F5 where the 3.58-MHz color subcarrier is reduced in amplitude to prevent beat interference due to mixing of the 3.58-MHz subcarrier and the FM modulation frequency. The characteristics of LPF2F5 are shown in Fig. 4-2. The filter impedance is 1 kΩ, and the filter delay is about 0.35 μs. The signal passing through LPF2F5 is amplified by the video amplifier (of IC2F2) and applied to the nonlinear emphasis circuit.

4-1.3 Nonlinear Emphasis Circuit

Since the FM signal usually deteriorates in signal-to-noise (S/N) ratio at the high frequencies, the signal is preemphasized during record to compensate for this deterioration. However, in this case, the narrower the video track thickness, the worse the S/N ratio becomes if the signal level decreases. To correct this condition, the high-frequency component of the input signal is recorded with nonlinear emphasis (more emphasis on low-level signals than on high-level signals). On playback, the signal is passed through a circuit with the reverse characteristics. This overall process improves the S/N ratio by about 3 dB.

Figure 4-3 shows the nonlinear emphasis circuit. On a 2-hour (standard) recording, the base of Q2H5 goes low, turning Q2H5 off, and Q2H1 on. The video signal from pin 22 of IC2F2 is supplied to pin 19 of IC2F2 through Q2H1, R244, R245, VR2G2, and C2N5, resulting in no emphasis. VR2G2 sets the level of FM deviation during record. On 6-hour (extended) recording, a high is applied to the base of Q2H5, turning Q2H5 on and Q2H1 off. Q2H4 turns on because of the high applied to the base. The video signal from pin 22 of IC2F2 is amplified by Q2H2 and Q2H3 and is taken from the emitter of Q2H3. Under these condi-

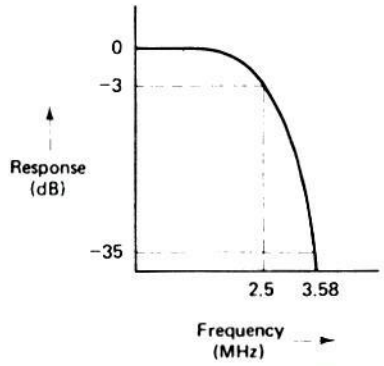


FIGURE 4-2. LPF2F5 characteristics.

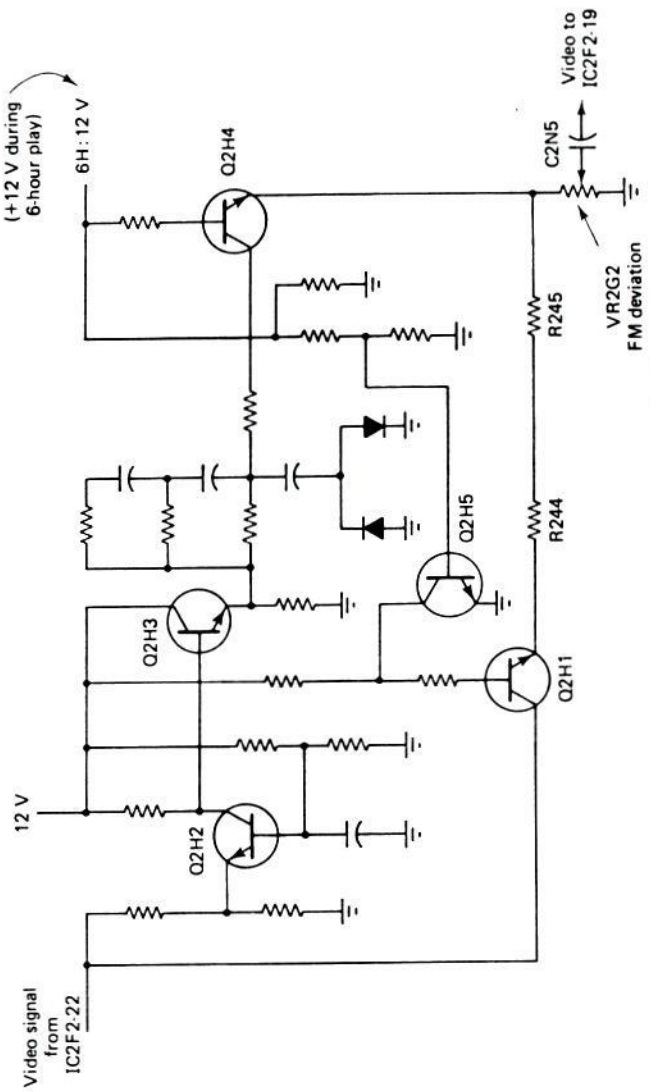


FIGURE 4-3. Nonlinear emphasis circuit.

tions, the video signal supplied to pin 19 of IC2F2 passes through the nonlinear emphasis circuit of Q2H4, VR2G2, and C2N5. As a result, though the rate of preemphasis is the same as a conventional circuit when signal level is high, the high-frequency region is further increased by about 8 dB when the signal level is small. The rate of preemphasis varies in this low-signal-level region.

4-1.4 *Clamp, Preemphasis, White and Dark Clip Circuits*

The video signal from the nonlinear emphasis circuit (set to the correct level for proper FM deviation by VR2G2) is amplified by the video amplifiers of IC2F2 and applied to the clamp. The signal amplified by the video amplifier is applied to the clamp through pin 16 to keep the sync tip accurately at a constant potential so that the sync tip remains at 3.4 MHz during FM modulation.

The video signal is then applied to preemphasis, where the high-frequency spectrum is emphasis to improve the S/N ratio at demodulation. Generally, the FM signal is subject not only to a change in amplitude by noise, but also to phase modulation. The higher the frequency, the more the FM signal is influenced by noise. In some literature, such noise is called "triangle noise" because of the characteristics as plotted in Fig. 4-4, which shows the noise at FM signal demodulation. Preemphasis is determined by the frequency response of the feedback loop from the collector of Q2F8 to pin 16. Figure 4-5 shows the typical preemphasis characteristic.

The video signal passing through the preemphasis circuit is applied to the white clip and dark clip circuits. Since a sharp overshoot and undershoot are caused at the rise and fall of the signal by preemphasis and can cause overmodulation when FM modulation is applied, the white level exceeding a specified level is clipped by the white clip. Similarly, the dark clip circuit clips the black level that goes below a specified point. VR2F3 controls white level, while VR2F9 controls the black level. The signal thus processed is applied to the FM modulator.

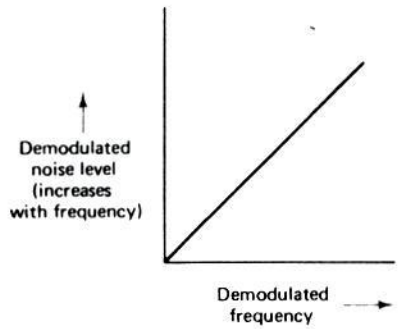


FIGURE 4-4. Noise at FM signal demodulation.

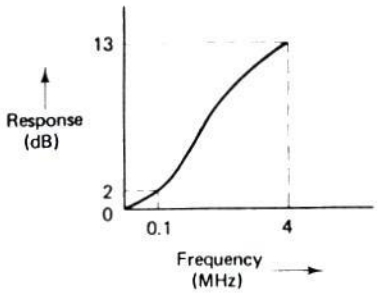


FIGURE 4-5. Typical preemphasis characteristics.

4-1.5 *FM Modulator, Carrier Interleave, Amplifier, and High-Pass Filter*

The video signal supplied from the white and dark clip circuits is fed to the FM modulator, which is adjusted by VC2F2. The FM modulator uses an emitter-coupled unstable multivibrator which is designed to operate from 3.4 MHz (at sync tip) to 4.4 MHz (at white peak). The FM-modulated signal, after being amplified by Q2G1 and converted into a lower impedance by emitter-follower Q2G2, is applied to the high-pass filter.

As shown in Fig. 4-6, during a color broadcast, the chroma signal is down-converted (heterodyned) to 629 ± 500 kHz to be superimposed on the FM signal. There is a part of the lower sideband of the FM signal which can overlap the color signal. This lower sideband is attenuated by the high-pass filter (HPF).

A 30-Hz pulse is applied to the FM modulator from the FM carrier interleave circuit to advance the phase of the channel 2 (head B) track by $\frac{1}{2}$ fH. Figure 4-7 shows the carrier interleave circuit. On 6-hour play, a high is fed from the collector of Q408 in the 2H/6H discriminator circuit to the cathode of D2G4. This turns D2G4 off and permits the 30-Hz pulses from the drum or cylinder servo to be applied at the base of Q2H0 through R2S5, D2F8, and D2F9. The drum pulse is inverted at the collector of Q2H0. During record, the magnitude of the video signal to be recorded is adjusted by VR2G6 and is fed to the FM modulator circuit. Since the drum pulse changes from high to low with each field, the carrier interleaving circuit interleaves the FM carrier by $\frac{1}{2}$ fH for each

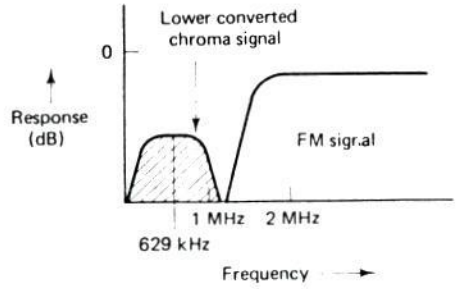


FIGURE 4-6. Relationship of chroma signal and FM signal during record.

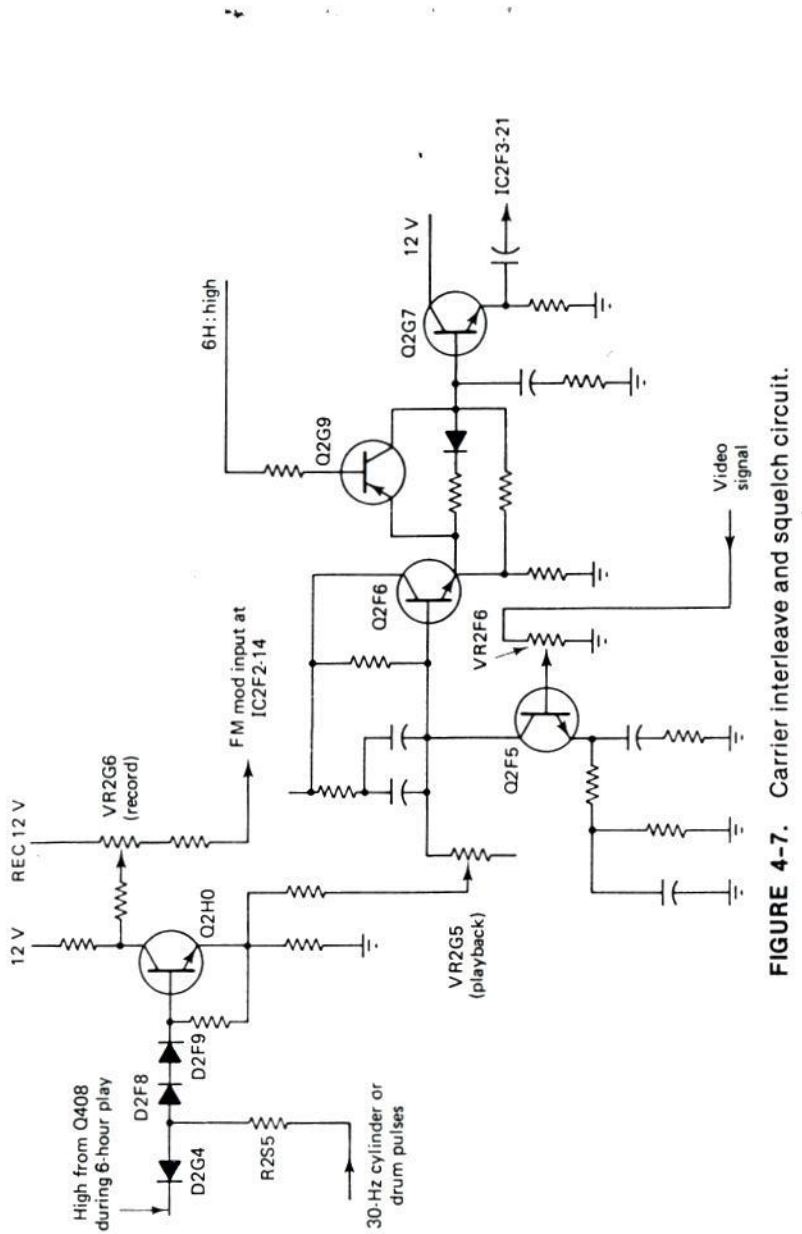


FIGURE 4-7. Carrier interleave and squelch circuit.

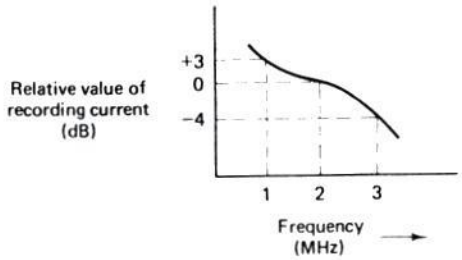


FIGURE 4-8. General characteristics of optimum recording current.

video track. This makes noise invisible on the picture (due to the integrating effect of the human eye). Note that the video signal is applied to the base of Q2F5 through VR2F6, which sets the level of the video signal.

4-1.6 *Squelch and Record Amplifier Circuit*

The signal from emitter of Q2H0 is supplied to the squelch circuit through VR2G5, as shown in Fig. 4–7. The squelch circuit functions to prevent signals from being fed to the record amplifier for about 1.5 seconds after completion of loading. This prevents the recorded signal from being erased if the tape runs near the drum during the loading process (if the tape is incorrectly threaded).

The signal passing through the squelch circuit is applied to the record amplifier IC2A1, which produces the optimum recording current for each signal frequency to be recorded. Figure 4–8 shows the general characteristics of optimum recording current. The record amplifier uses a complementary SEPP [single-ended (push-pull) circuit] which minimizes crossover and switching distortion while still providing a low load resistance.

4-2 VHS LUMINANCE SIGNAL CIRCUITS DURING PLAYBACK

Figure 1-42 is the overall block diagram of the luminance circuits used during playback. Overall functions of these circuits are described in Sec. 1-9.2. The following paragraphs describe details and characteristics for some of the circuits.

4-2.1 *Preamplifier, Switch and Mixer Amplifier*

Since the playback signal from the video head is in the order of a few millivolts, the playback signal is amplified in the first, second, and third preamplifiers to a level of about 0.3 V (peak to peak). The preamplifier circuits are provided with adjustment controls to produce an overall flat response as shown in Fig. 4–9. This is done by adjusting both the resonance frequency and the Q of the video

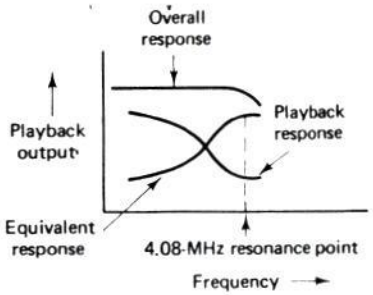


FIGURE 4-9. Reproduction characteristics to produce overall flat response during playback.

heads. VC2A1 and VC2A0 are adjusted to set the resonance of the heads at about 4.08 MHz. VR2A1 and VR2A0 are adjusted to set the video head Q so that the overall response characteristics of Fig. 4–9 are obtained at playback.

The signals amplified by the preamplifiers are mixed by the switching circuit and mixer amplifier to produce a continuous noise-free signal as shown in Fig. 4–10. Note that the overlap of the channel 1 and channel 2 signals at the heads is eliminated by the drum FF pulses, which switch the channel 1 and channel 2 output so that channel 1 is off at the instant channel 2 is on (and vice versa). The continuous signal obtained from the switching circuit is adjusted for proper balance between the channels by VR2A2. This signal is amplified by the mixer

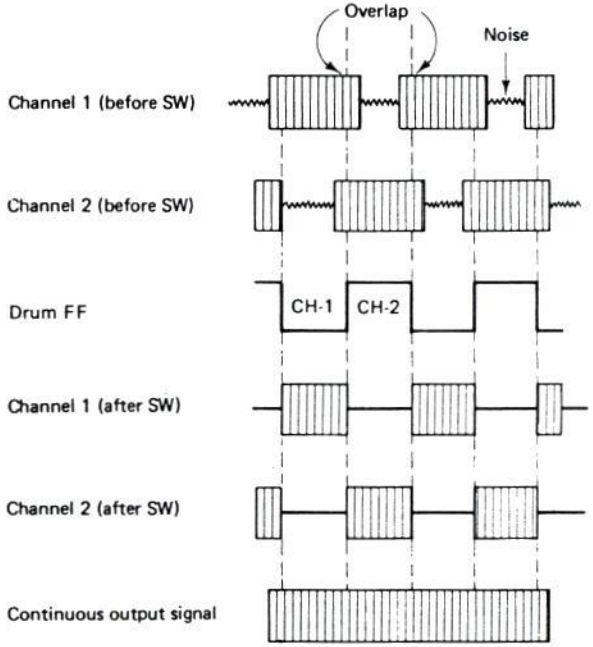


FIGURE 4-10. Switching and mixing process to produce a continuous signal from the video heads.

amplifier, adjusted to the correct FM level by VR2F4, and applied to the video amplifier circuit.

4-2.2 Video Amplifier and High-Pass Filter

The signal from VR2F4 is amplified by Q2F0 and passed through high-pass filter HPF2F0 to Q2F1. The high-pass filter removes the 629-kHz color signal. Emitter follower Q2F1 converts the output to a low impedance.

4-2.3 Dropout Compensation Circuit

Figure 4–11 shows the dropout compensation (DOC) circuit in block form. The DOC circuit is disabled during black-and-white operation by a color killer voltage applied to the changeover switch. During black-and-white operation, the switch connects the mixer to the FM input through pin 9, so that the FM signal passes to pin 10 and is not affected by the DOC circuit. During a color broadcast, the changeover switch connects the FM input from pin 7 to the mixer, and then to the circuit output at pin 10. This same output is applied through the 1H delay line and amplifier to the gate circuit. The gate remains closed when there is no dropout. The FM input at pin 7 is amplified by the DOC amplifier and applied to the DOC detector. If dropout is present, the detector produces a pulse that is shaped by the Schmitt trigger and applied to the gate. The pulse opens the gate

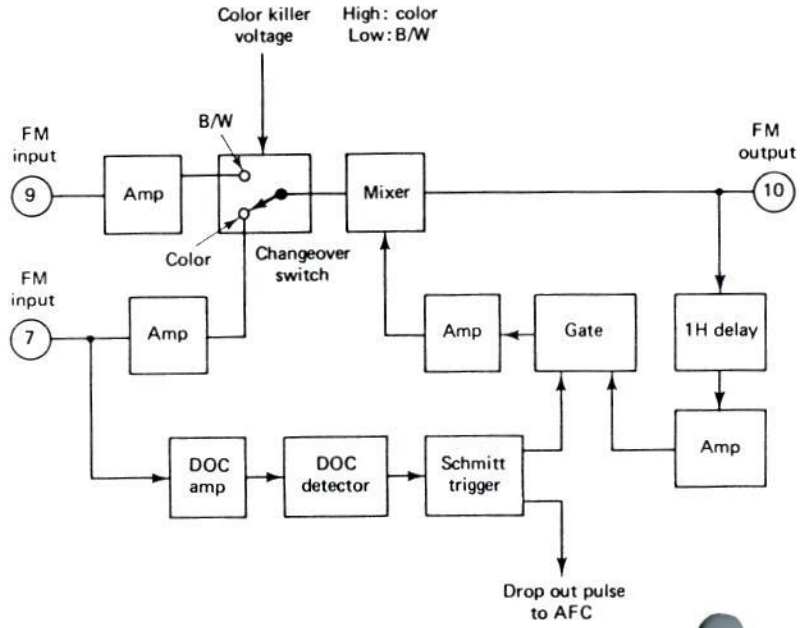


FIGURE 4–11. Basic dropout compensation circuit

and permits signal passing through the 1H delay line to be amplified and mixed with the signal from pin 7, thus eliminating dropout. As discussed in Sec. 1-9.6, the dropout pulse is also applied to the AFC circuit.

4-2.4 Double Limiter Circuit

Figure 4–12 shows the double limiter circuit in block form. A double limiter is used to offset the effects of preemphasis of the signal at various stages. Such preemphasis can result in sharp overshoot, as shown in Fig. 4–12. If a signal with ex-

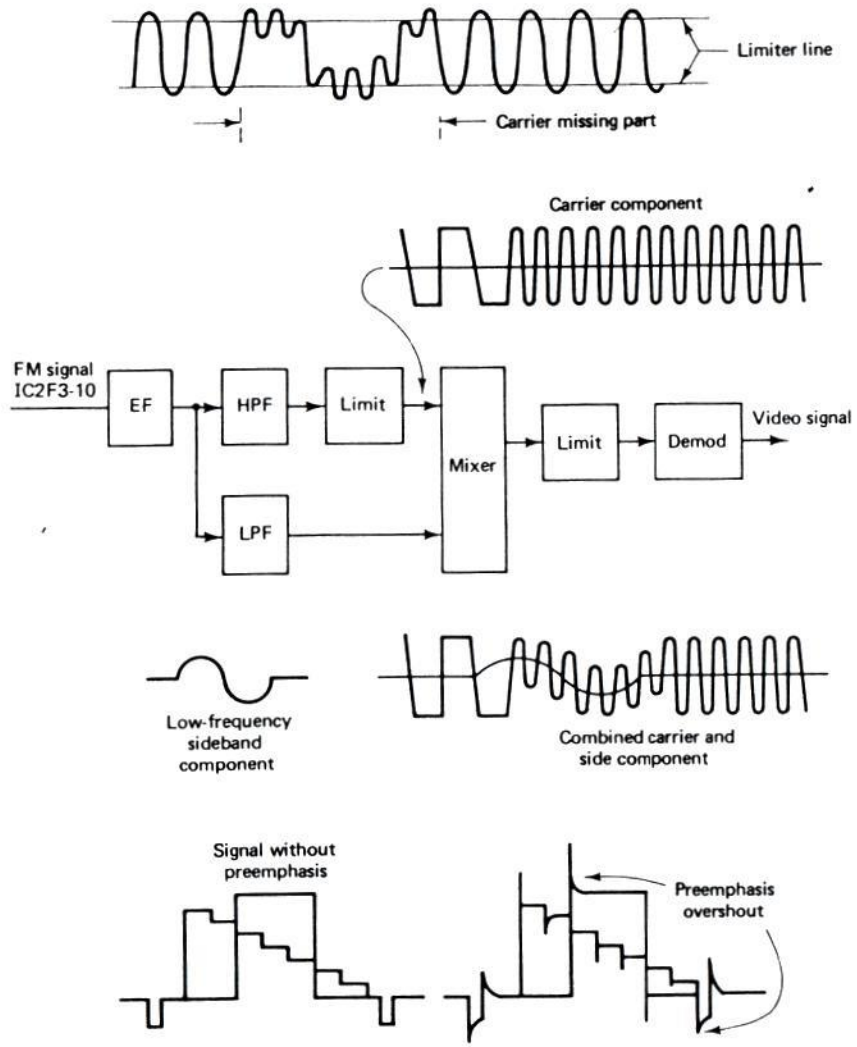


FIGURE 4–12. Double limiter circuit.

cessive overshoot is FM modulated, overmodulation occurs and the low-frequency sidebands can be increased in amplitude. This results in possible AM modulation and can cause picture reversal or negative picture (white parts turn black, and vice versa). The signal-to-noise ratio also deteriorates. Although the white and dark clip circuits serve to reduce overshoot, any AM modulation must be eliminated by limiting (as in the case of any FM system). However, conventional limiting can result in loss of low-frequency sidebands (which, in turn, results in loss of high-frequency signals after demodulation, and picture deterioration).

In the double limiter of Fig. 4–12, the FM signal is passed through a high-pass filter and a low-pass filter to separate the signal into a carrier component and a low-frequency sideband component. The carrier is further limited and mixed with the sidebands. The combined signal is again limited and demodulated. This double limiter system compensates for the ratio of the carrier and sidebands, without amplifying noise, and thus ensures no loss of carrier.

4-2.5 FM Demodulator Circuit

Figure 4–13 shows the FM demodulator circuit and the associated waveforms. The FM signal entering pin 14 of IC2F6 is limited by the limiter circuit and is fed to the mixing circuit through an internal IC2F6 circuit and through an external circuit. This external circuit is adjusted to provide the proper time constants and balance by VR2G8 and VR2G9 (limiter and carrier balance, respectively). The time period $T_0 = 1/FC$ of the FM waveform coming from pin 6 of IC2F6 is delayed by $1/4\ T_d$. The resultant signal is then mixed, detected, and rectified into waveform D of Fig. 4–13. The video portion of this signal is applied to the deemphasis and feedback circuits through an emitter follower Q2F4 and a low-pass filter LPF2F2.

4-2.6 Deemphasis and Feedback Circuits

The deemphasis circuit is provided to reduce high-frequency noise during playback by attenuating the high-frequency components using a characteristic almost exactly opposite that of the preemphasis circuits during record. The level of the playback luminance signal entering the deemphasis circuit is set by VR2F6. The deemphasized signal is supplied to the edge noise canceler.

4-2.7 Edge-Noise Canceler Circuit

Figure 4–14 shows the edge noise canceler circuit and the associated waveforms. The video signal from the emitter of Q2F5 is differentiated by C2Q6, R248, and R247 and is fed to the base of Q2H7. The signal is amplified and inverted by Q2H7. After the noise component is eliminated by D2G2 and D2G3, the signal is applied to the base of Q2H8, where the signal is amplified and superimposed on the video signal at the collector of Q2F5 to cancel noise.

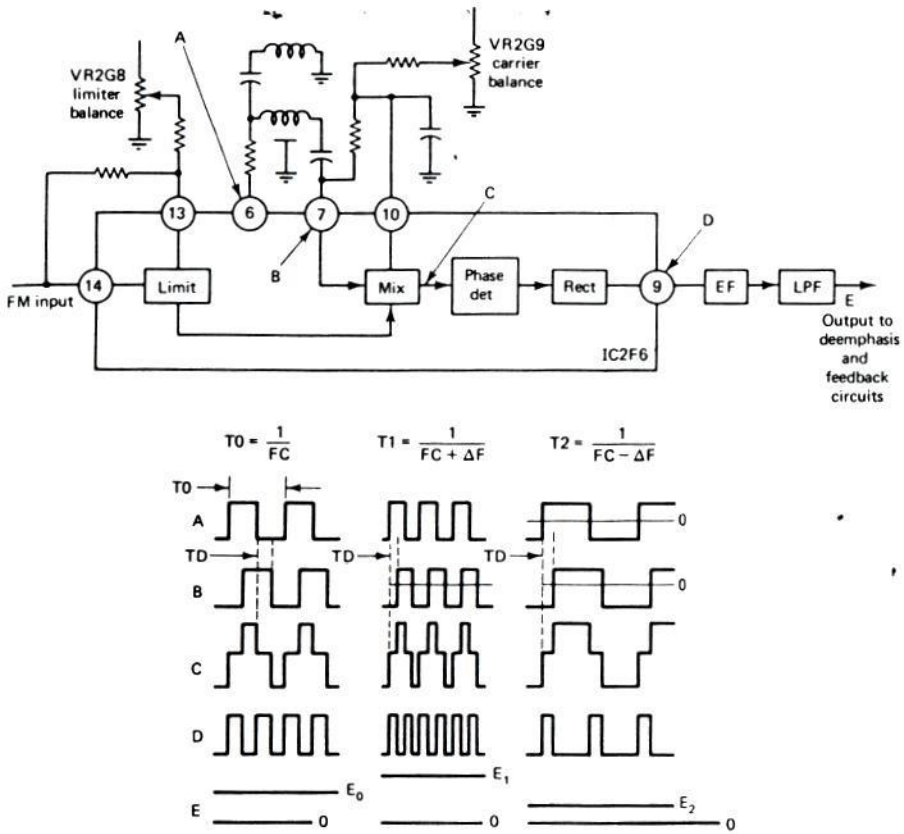


FIGURE 4–13. FM demodulator and associated waveforms.

Since, at recording, the channel 2 signal is advanced by $\frac{1}{2}$fH by the carrier interleave circuit (Sec. 4–1.5 and Fig. 4–7), a small variation in the d-c level occurs during playback. Therefore, the 30–Hz pulse derived from the emitter of Q2H0 is fed to the base of Q2F6 through VR2G5 to compensate for the d-c variation.

4-2.8 Nonlinear Deemphasis Circuit

Figure 4–15 shows details of the nonlinear deemphasis circuit used during playback. During 2-hour (standard) playback, the base of Q2G9 goes low to turn on Q2G9 and short circuit the filter network (R2S1, R2D3, D2G6). Similarly, the base of Q2G8 goes low, turning Q2G8 off and disabling the filter network (R2D4, C2R0, D2F5). During 6-hour playback [called expanded playback (EP)] a high is supplied to the base of Q2G9. This turns Q2G9 off and connects the filter (R2S1, R2D3, D2G6) into the circuit. A high is also supplied to the base of Q2G8. This turns Q2G8 on and connects the filter (R2D4, C2R0, D2F5) into the circuit.

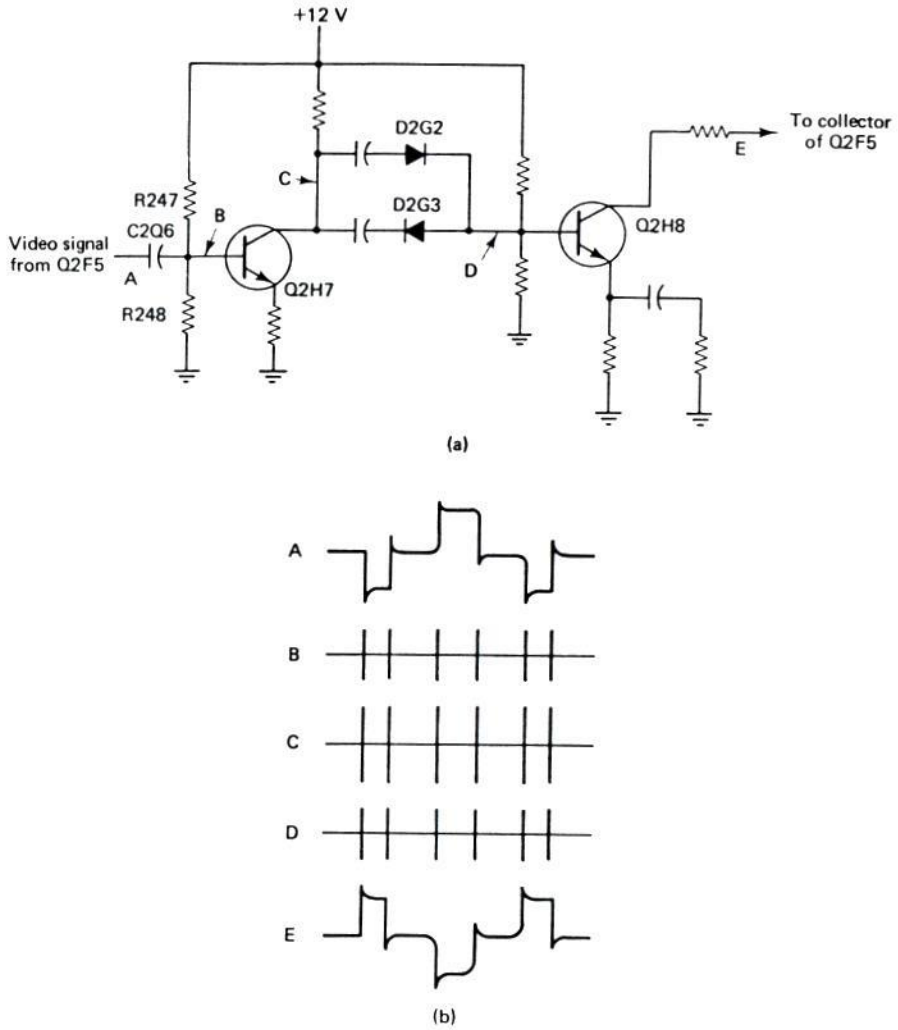


FIGURE 4-14. Edge noise canceler and associated waveforms.

When processing normal signals during playback, the high-frequency component of the video signal at the emitter of Q2F6 is attenuated by the filter of R2S1, C2R1, and R2G2. In the case of a signal where the black level changes rapidly into a white level, undershoot and noise occur. During 6-hour play, D2G6 is inserted and turned on by the undershoot. The turn-on of D2G6 connects R2S1 and R2D3 in parallel, reducing the combined resistance and increasing the filter effect to reduce the undershoot.

If the high-frequency component of the video signal becomes larger (during 6-hour play), D2F4 and D2F5 are turned on, attenuating the signal at the base

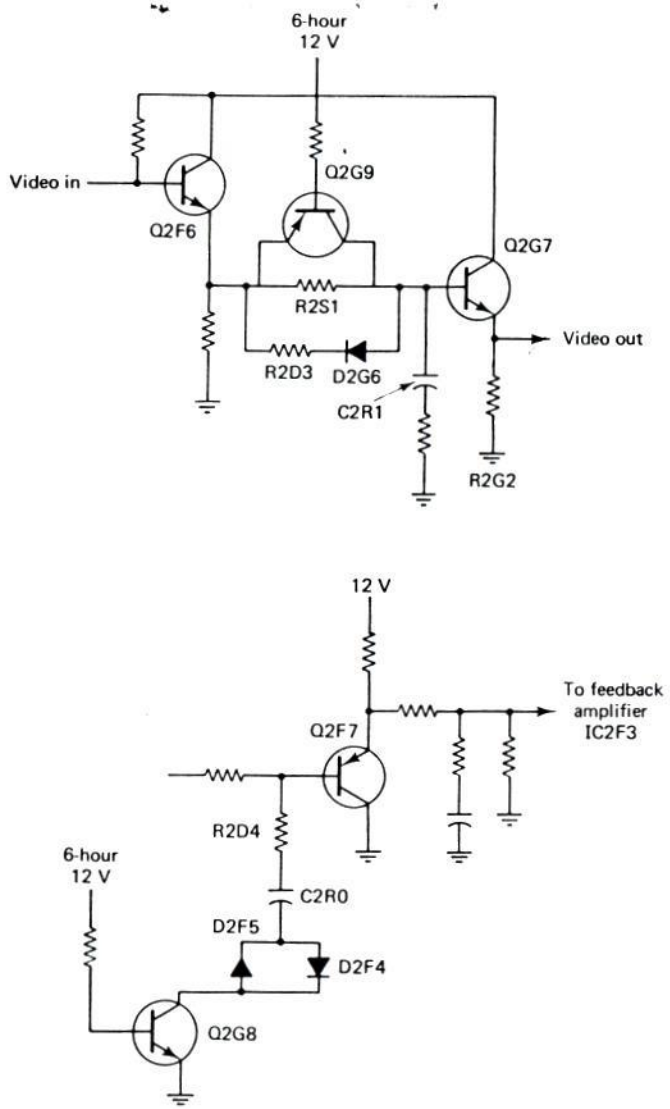


FIGURE 4-15. Playback nonlinear deemphasis circuit.

of Q2F7 (through R2D4, C2R0, D2F4, D2F5, and Q2G8). The larger the high-frequency component, the more the Q2F7 base level is attenuated. The output of Q2F7 is applied to feedback amplifier IC2F3, where the high-frequency component of the video signal is boosted. In this case, the larger the signal, the more the high-frequency component is boosted.

To summarize, the nonlinear deemphasis circuit is designed so that the high-frequency component can be attenuated by the filter, and boosted by the feedback amplifier, to correct for the nonlinear emphasis at recording.

4-2.9 Color/BW Switch

Figure 4–16 shows details of the color/BW switch network. The switch is operated by a color killer voltage and connects the low-pass filter LPF2F3 and video amplifier into the signal path when the color killer voltage is high. LPF2F3 ensures that the point where the video signal overlaps the demodulated chroma signal is free of noise, and the video amplifier compensates for any attenuation by LPF2F3. During a black-and-white playback, the color killer voltage goes low, and the switch operates to bypass both LPF2F3 and the video amplifier. This is necessary because black-and-white picture resolution can deteriorate if the signal is passed through the low-pass filter.

4-2.10 Noise Canceler, Clamp, Mute, EE/VV Switch

As shown in Fig. 1–42, the signal from the color/BW switch is processed in the high-pass amplifier (HPA) to extract only the high-frequency component to be amplified. The signal is then limited and applied to the noise canceler. The direct signal from the color/B&W switch is also added to the noise canceler so that only the high-frequency component is canceled. This type of noise canceler circuit, using a low-frequency boost circuit, improves picture quality.

The color signal is superimposed on the video signal in the Y/C mixer and is fed to the clamp/mute circuit, which receives a quasi-sync signal at pin 26. This quasi-sync signal is added to the video signal to replace or supplement the normal sync during the still, frame transfer, speed search, or slow playback modes (which may be disturbed by noise during these modes). The E-E/V-V switch is provided to automatically switch video playback and monitor (E-E) signals. Both the playback video signal from the clamp/mute circuit and the monitor (E-E) signals from the E-E amplifier are applied to the E-E/V-V switch. During record, the E-E signals are passed through the E-E/V-V switch to the RF unit so that the program being recorded can be viewed on the TV set. During playback, the E-E/V-V switch disconnects the E-E input and connects the playback video from the clamp/mute circuit to the RF unit.

4-2.11 Quasi-Sync Signal Generator

Figure 4–17 shows the quasi-sync signal generator and the associated waveforms. The drum FF pulse is applied to pin 8 of IC501, and a high from the speed search discriminator is applied to pin 9 during still, frame transfer, speed search, or slow playback. During normal playback, pin 9 goes low and pin 10 remains high, even though the drum FF pulse is being applied to pin 8. As a result, no quasi-sync signal is produced.

When a high is applied to pin 9, the drum FF pulse passes and appears at pin 10 (in inverted form). The pulse is then applied to another NAND gate (at pins 12, 13) and appears at pin 11 (again inverted). The drum FF pulse at pin 10 is differentiated by C502 and R506 and is applied to pin 1. Similarly, the pulse at pin 11 is differentiated by C503 and R501 and is applied to pin 2. This results in a 60-Hz pulse at pin 3. The 60-Hz pulse is differentiated by C504 and R502 and is applied to pins 5 and 6. The output at pin 4, a positive 60-Hz pulse of about 0.3-ms width, is inverted by Q501 and fed to the clamp/mute circuit as the quasi-sync signal.

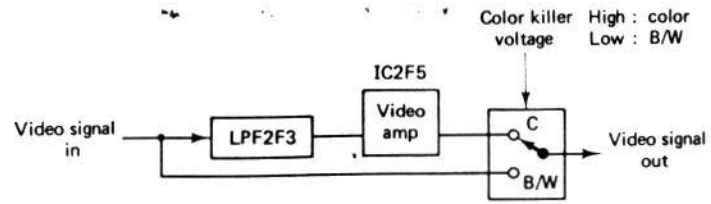


FIGURE 4–16. Color/BW switch network.

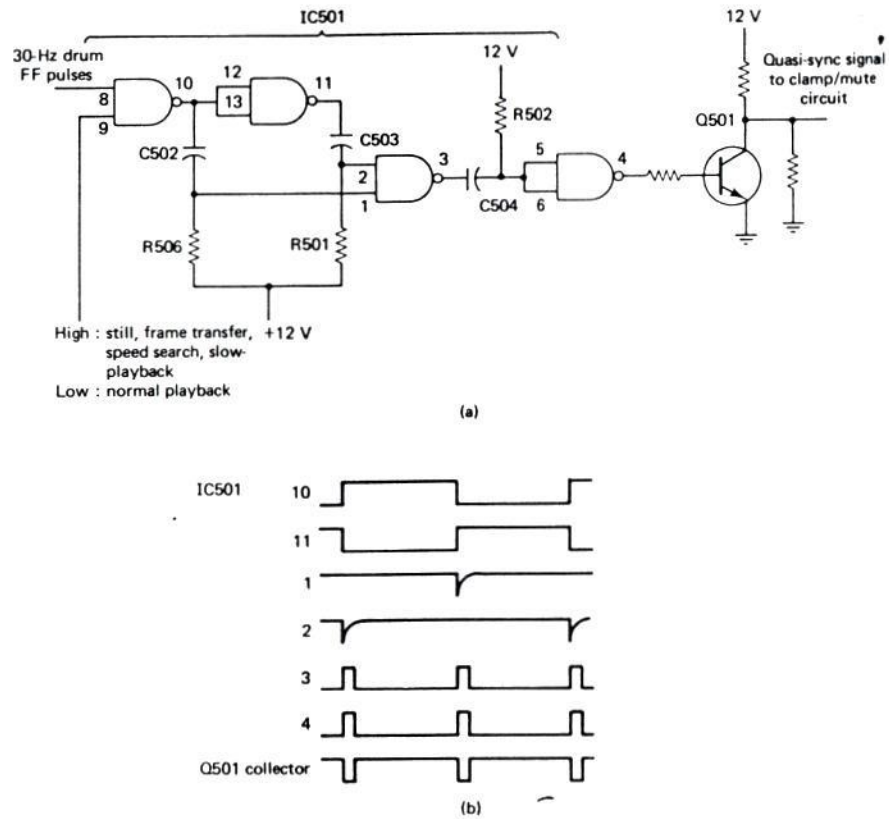


FIGURE 4–17. Quasi-sync signal generator and associated waveforms.

4-3 VHS COLOR SIGNAL CIRCUITS DURING RECORD

Figure 1-43 is the overall block diagram of the color circuits used during record. Overall functions of these circuits are described in Sec. 1-9.3. The following paragraphs decribe details and characteristics for some of the circuits.

4-3.1 *Bandpass Filter, Amplifier, Expander, and Emitter Follower*

As shown in Fig. 4-18, the video signal from the tuner is applied to BPF6F0, where only the 3.58-MHz color burst signal is passed. The response of BPF6F0 is also shown in Fig. 4-18. The signal passing through BPF6F0 is supplied to the emitter of Q6F0, which is connected in a grounded-base configuration. The amplified signal is applied through emitter follower Q6F1 to the ACC circuit. The horizontal pulse from pin 15 of IC6F4 is passed through a low-pass filter

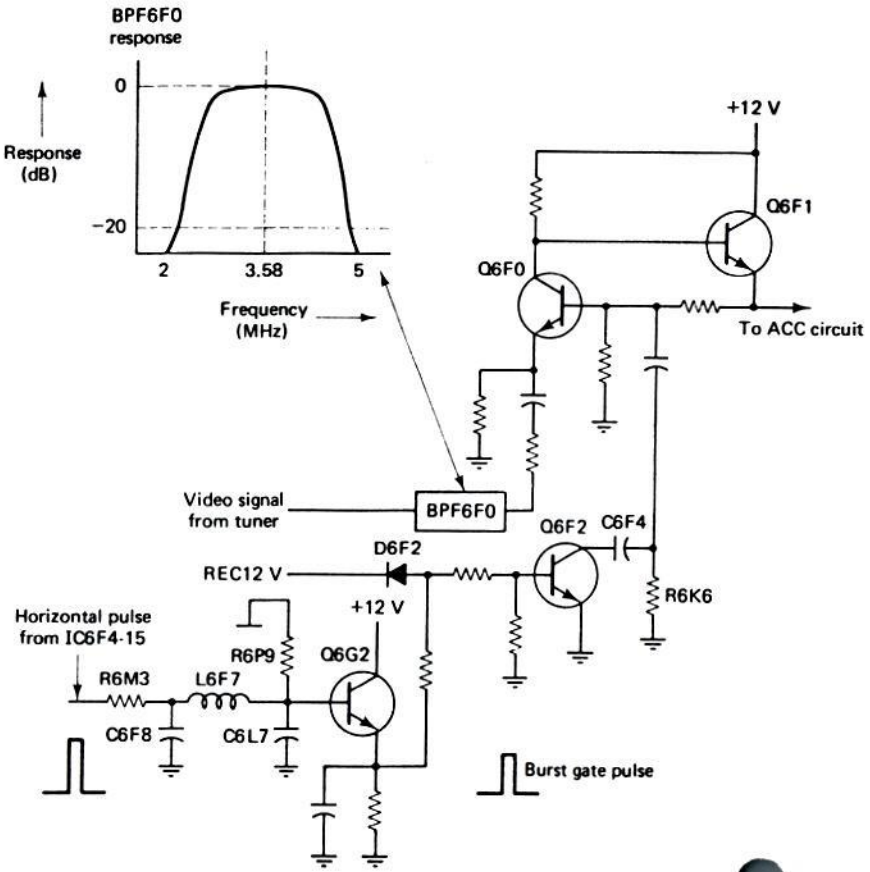


FIGURE 4-18. Bandpass filter, amplifier, expander, a emitter-follower circuits.

(R6M3, C6F8, L6F7, C6L7, R6P9), and an emitter follower Q6G2 to the base of Q6F2. This turns Q6F2 on and connects C6F4 in parallel with R6K6 to increase the gain of Q6F0 by about 6 dB during the horizontal pulse. Thus, the 3.58-MHz color signal is passed to the ACC circuit during the horizontal pulse. The low-pass filter delays the horizontal pulse so that the pulse output from the emitter of Q6G2 corresponds to the color burst portion. During playback, D6F2 is turned on so that Q6F2 remains turned off and keeps the gain of Q6F0 low during playback. This prevents tuner noise from passing to the ACC circuit during playback.

4-3.2 *ACC and Detector Circuit*

As shown in Fig. 1-43, the output of the ACC (automatic color control) at pin 11 is passed to the main converter and through the Q6F3 switch (which is turned on by the REC12V voltage) to the IC6F0 burst gate. The REC12V voltage is also applied to the burst gate and to a switch Q6F5, turning on both stages. During record, Q6F5 connects C6H1 in parallel with C6G8, R6H1, and C6G9 to change the time constants as necessary to alter the detector output. Within the detector, the peak value of the 3.58-MHz color signal is converted to a d-c voltage used as a bias or control voltage by the ACC (at pin 5). This control voltage keeps the 3.58-MHz color signal constant during record, and keeps the 629-kHz color signal constant during playback. VR6F0 sets the ACC output level during both record and playback.

4-3.3 *Main Converter, Low-Pass Filter, and Emitter Follower*

As shown in Fig. 1-43, the 3.58-MHz output from the ACC is applied to the main converter IC6F0 at pin 3. IC6F0 also receives a 4.2-MHz signal from the APC circuit (Sec. 4-5) at pin 5. This produces both sum and difference frequencies at the main converter output (pin 7). As described in Secs. 1-9.5 and 1-9.6, the 4.2-MHz signal is rotated in phase by +90° each 1H period for channel 1 and −90° for channel 2. As a result, the difference frequency at pin 7 is also rotated in phase by ±90°. This difference frequency of 629 kHz ± 90° is passed by LPF6F0, where the sum frequency is rejected. The difference-frequency signal is passed through Q6F6 and VR2G4 to the record amplifier. VR2G4 sets the level of the color signal during record. During black-and-white programs, Q6F6 is turned off to prevent noise in the color circuits from being recorded.

4-4 VHS COLOR SIGNAL CIRCUITS DURING PLAYBACK

Figure 1-44 is the overall block diagram of the color circuits used during playback. Overall functions of these circuits are described in Sec. 1-9.4. The following paragraphs describe details and characteristics for some of the circuits.

4-4.1 Amplifiers, Low-Pass Filter, and Emitter Follower

As shown in Fig. 1-44, the playback signal (video FM signal plus 629-kHz color signal) from pin 10 of IC2F0 is applied through the FM level adjustment VR2F4 to be amplified by Q2F3. A trap (C2H1-L2F5) is inserted at the base of Q2F3 to attenuate the high-frequency sound bias recorded on the tape. The amplified signal from Q2F3 is applied through LPF2F0, where the 629-kHz color signal is passed. The color signal is then amplified by Q6F0 and applied through emitter follower Q6F1 to the ACC circuit of IC6F0.

4-4.2 ACC Circuit

As shown in Fig. 1-44, the output from Q6F1 is applied through the ACC circuits of IC6F0 to the main converter of IC6F0, where the 629-kHz signal is mixed with the 4.2-MHz signal to restore the 3.58-MHz color signal. The 3.58-MHz signal is applied through BPF6F1, Q6F7, DL6F0, and IC6F1 to the burst gate IC6F0. The gate opens only during the burst period, and supplies only the burst signal to the detector. Within the detector, the peak value of the 3.58-MHz color signal is converted to a d-c voltage used as a bias or control voltage by the ACC. This control voltage keeps the 629-kHz color signal passing through the ACC constant during playback. VR6F0 sets the ACC output level during both playback and record.

4-4.3 Compressor Circuit

As shown in Fig. 4-19, the 3.58-MHz signal from BPF6F1 is passed through Q6F7, which is controlled by compressor Q6F8. During record, the burst signal is increased by the expander circuit (Sec. 4-3.1, Fig. 4-18). During playback, the

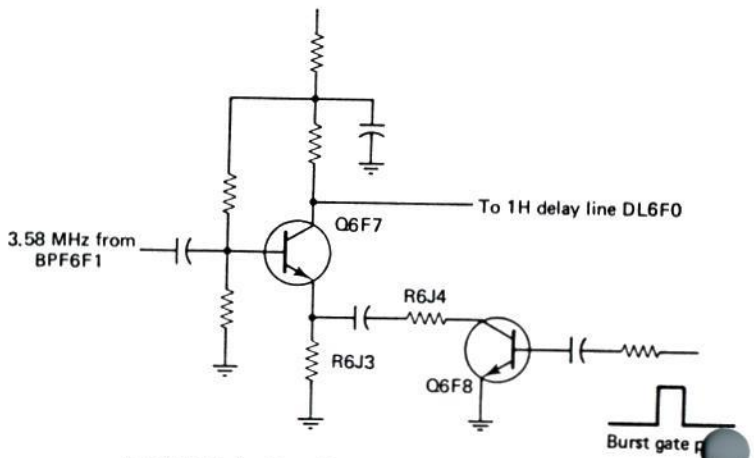


FIGURE 4-19. Burst compressor circuit.

compressor circuit of Fig. 4-19 reduces the burst signal by 6 dB. When there is no burst gate pulse, Q6F8 is turned on, placing R6J4 in parallel with R6J3, reducing the emitter resistance and increasing the gain of Q6F7. When the burst gate pulse is applied, Q6F8 is turned off, leaving only R6J3 in the emitter of Q6F7. This increases the emitter resistance and decreases the gain of Q6F7 (by about 6 dB).

4-4.4 1H Delay

As shown in Fig. 1-44, the amplified signal from Q6F7 is passed through 1H delay line DL6F0 to amplifier IC6F1. Figure 4-20a shows the equivalent circuit of DL6F0, which is designed to pass only the 3.58-MHz signal. As discussed in Sec. 1-9, with the VHS color recording system, the channel 1 track is advanced by 90°, while the channel 2 track is delayed by 90° for each 1H period. This produces a recording pattern similar to that of Fig. 4-20b. Figure 4-20c shows what can occur if the channel 1 head traces slightly on the channel 2 track during playback (producing crosstalk).

When both the major signal and crosstalk are passed through a 1H delay line, the major signal becomes equivalent to the component vector (about double), and the crosstalk is canceled. The 1H delay line circuit improves the signal-to-noise ratio by about 3 dB.

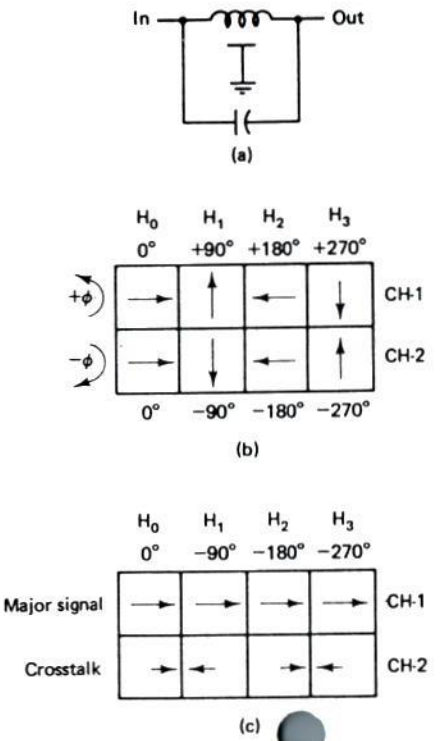


FIGURE 4-20. 1H delay functions.

4-4.5 *Amplifier and Killer Amplifier*

As shown in Fig. 1-44, the color signal from which the crosstalk components have been removed by DL6F0 is amplified by IC6F1, killer amplifier IC6F0, and is applied to IC2F3 (Fig. 1-42) through color output adjust VR6F1. The color signal is mixed with the luminance (Y) signal in IC2F3. Killer amplifier IC6F0 also receives a control signal from the color killer circuit applied at pin 6. When pin 6 is high, the color signal is passed from pin 10 of IC6F0. During a black-and-white program, the color killer control signal is low at pin 6, and no output is obtained from pin 10 of IC6F0. This prevents noise in the color circuit from passing during black-and-white operation.

4-5 VHS SERVO SYSTEM

The majority of the servo circuits described in this chapter are part of the Hitachi VT-8500A. Overall functions of the servo system for this VCR are described in Sec. 1-9.7. The following paragraphs describe details and characteristics for some of the circuits.

4-5.1 *Cylinder Phase Control Circuit*

Figure 4-21 is the overall block diagram of the cylinder phase control circuit. Figure 4-22 shows the related waveforms.

As shown in Fig. 4-21, the 30-Hz cylinder tach pulse from the pulse generator installed in the lower part of the cylinder shaft is supplied to the comparison signal circuit for cylinder phase control in IC501 through pin 19. This cylinder tach pulse is used in both playback and recording. The pulse at pin 19 is applied to the positive pulse amplifier and negative pulse amplifier to be detected separately as positive and negative pulses. The pulse applied to the positive amplifier is detected as the positive pulse and amplified to a level suitable to trigger monostable multivibrator MM 1, which acts as an adjustable delay circuit to determine the video head switching phase. The delay can be changed by the time constant of C522 and R541 connected to pin 18. Channel 1 switching phase is adjusted by R505. The pulse applied to the negative amplifier is delayed by MM 2, as adjusted by R504.

The output from MM 1 and MM 2 is supplied to a flip-flop FF. MM 1 is connected to the reset input of the FF, with MM 2 connected to the set input. The pulse from the FF (waveform F of Fig. 4-22) is the video head switch pulse, called SW30 and supplied to the video luminance and color circuits. Pulse SW30 is adjusted by R504 and R505 to become a 30-Hz rectangular wave with a 50% duty cycle. The output of the FF is converted to a trapezoidal waveform which is applied to the sample-and-hold circuit as a comparison signal. The sample-and-hold circuit also receives a reference signal which is compared with the

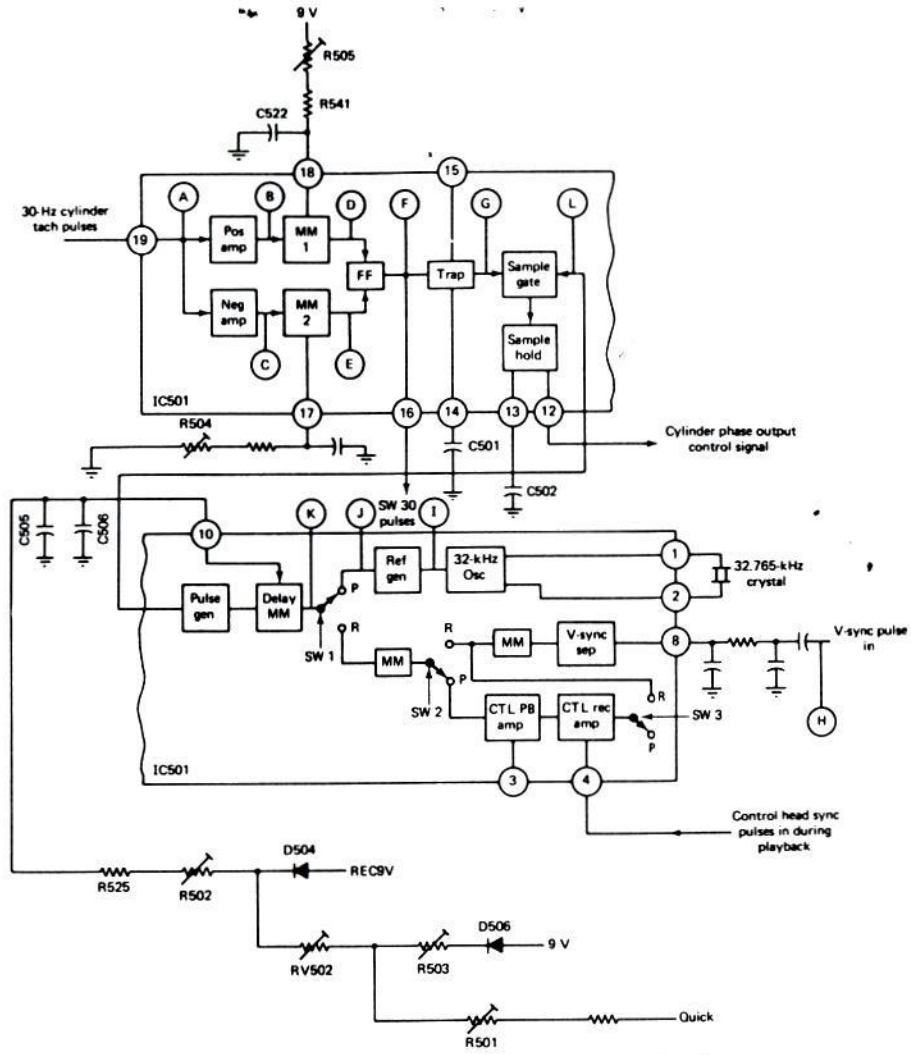


FIGURE 4-21. Cylinder phase control circuit.

trapezoidal signal to produce the desired cylinder phase output control signal at pin 12.

During record, switches SW 1, SW 2, and SW 3 in IC501 are electrically connected to the record position, and the broadcast V-sync signal is used as the reference signal. The V-sync component of the composite sync signal supplied by the luminance circuit is applied to pin 8. The V-sync signal is separated by the V-sync separator and shaped by the monostable multivibrator to produce a 30-Hz rectangular pulse. This pulse is amplified through the control pulse recording amplifier and supplied to the control head (through pin 4), where the

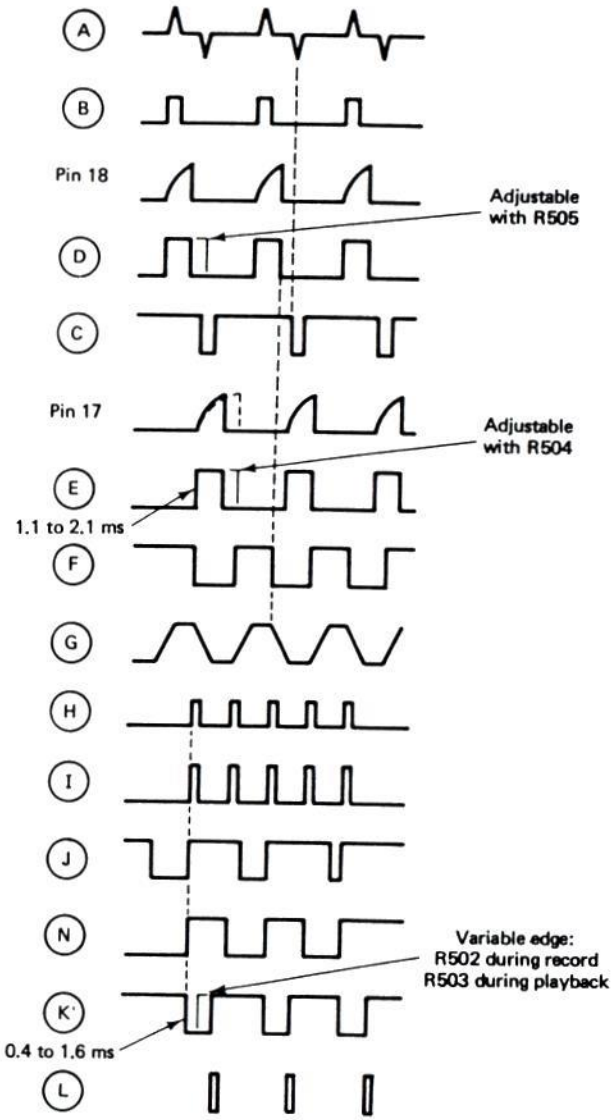


FIGURE 4-22. Waveforms associated with cylinder phase control circuit.

pulse is recorded on tape to become the capstan control signal during playback.

During playback, switches SW 1, SW 2, and SW 3 are electrically connected to the playback position, and the internal crystal-controlled signal is used as the reference signal. The playback reference signal is obtained by dividing the 32.765-MHz signal (developed by the crystal oscillator using an external crystal

connected at pins 1 and 2) by 1093. This 1093 division occurs in the reference generator circuit.

During either playback or record, the delay MM circuit receives a 30-Hz reference signal through switch SW 1. During playback, the time constant of the delay MM is increased to provide correct tracking. Diode D504 is off during playback, and the delay MM time constant is approximately equal to the total of C505, C506, R502, R503, R525, and RV502. Diode D504 is turned on during record by a 9V control voltage, removing RV502 and R503 from the circuit, and decreasing the time constant of the delay MM to the equivalent of C505, C506, R502, and R525. Variable resistor R502 is the record timing control used to set the recorded V-sync signal at the correct position. R501 and R503 provide a similar function during playback (R501 for the quick mode, and R503 for other modes). Refer to Sec. 4–6 for a discussion of the various operating modes.

The pulse generator differentiates the pulse obtained through the delay MM to produce the reference sampling pulse applied to the sample-and-hold (S/H) circuit. When the trapezoidal wave (comparison signal) and the sampling pulse (reference signal) are applied to the S/H circuit, and error voltage corresponding to the phase difference is generated and applied to the capstan speed control circuit (Sec. 4–5.3) through pin 12. Capacitor C502 holds the error voltage between samplings.

If the speed and phase of the cylinder are correct, the trapezoidal and sampling pulses line up as shown in Fig. 4–23. Notice that the sampling pulse lines up in the center of the trailing edge of the trapezoid. When the trapezoid waveform and the sampling pulse are supplied to the S/H stage, the voltage level of the trapezoid ramp is sampled (at the point where the sampling pulse intersects the ramp). This is given as X-volts in Fig. 4–23.

If the cylinder motor speed increases, the trapezoid wave phase leads with respect to the sampling pulse as shown in Fig. 4–24. The sampling position moves lower on the ramp, and the error voltage decreases, making the cylinder motor rotate at a lower speed. If the cylinder motor speed decreases, the trapezoidal wave lags behind the sampling pulse as shown in Fig. 4–25, and the sampling

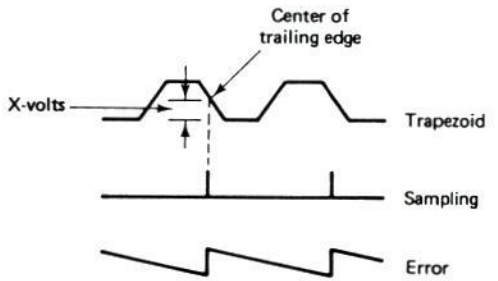


FIGURE 4-23. Relationship of pulses when cylinder speed is normal.

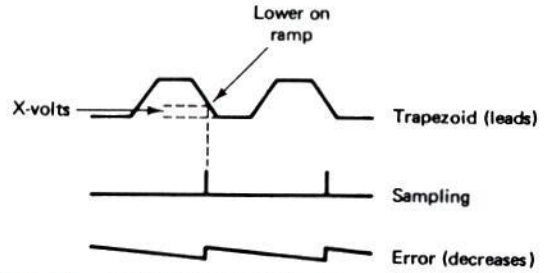


FIGURE 4-24. Relationship of pulses when cylinder speed increases.

position moves higher on the ramp. As a result, the error voltage increases, making the cylinder rotate faster.

In summary, when the sampling pulse is used to sample the trapezoid ramp, a variable voltage results that is in direct relationship to the relative position of the sampling pulse on the ramp. Because this voltage represents video head position, the voltage can be used to control the cylinder motor phase. However, the phase control voltage developed by this circuit is limited to that which can be detected on the slope of the ramp, and is used only as a vernier speed control (or phasing control) voltage. The actual speed of the cylinder motor is controlled by the speed control circuit as discussed in Sec. 4-5.3.

4-5.2 *Capstan Phase Control Circuit*

Figure 4-26 is the overall block diagram of the capstan phase control circuit. Figure 4-27 shows the related waveforms.

As shown in Fig. 4-26, during record, the comparison signal of the capstan phase control is obtained from the frequency generator (FG) built into the capstan motor. The record comparison signal (capstan FG pulse) frequency is 720 Hz in SP, 360 Hz in LP, and 240 Hz in EP operating modes. Refer to Sec. 4-6

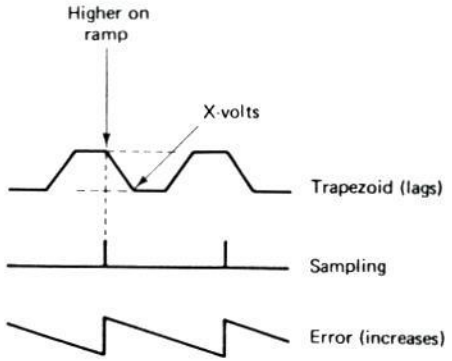


FIGURE 4-25. Relationship of pulses when cylinder speed decreases.

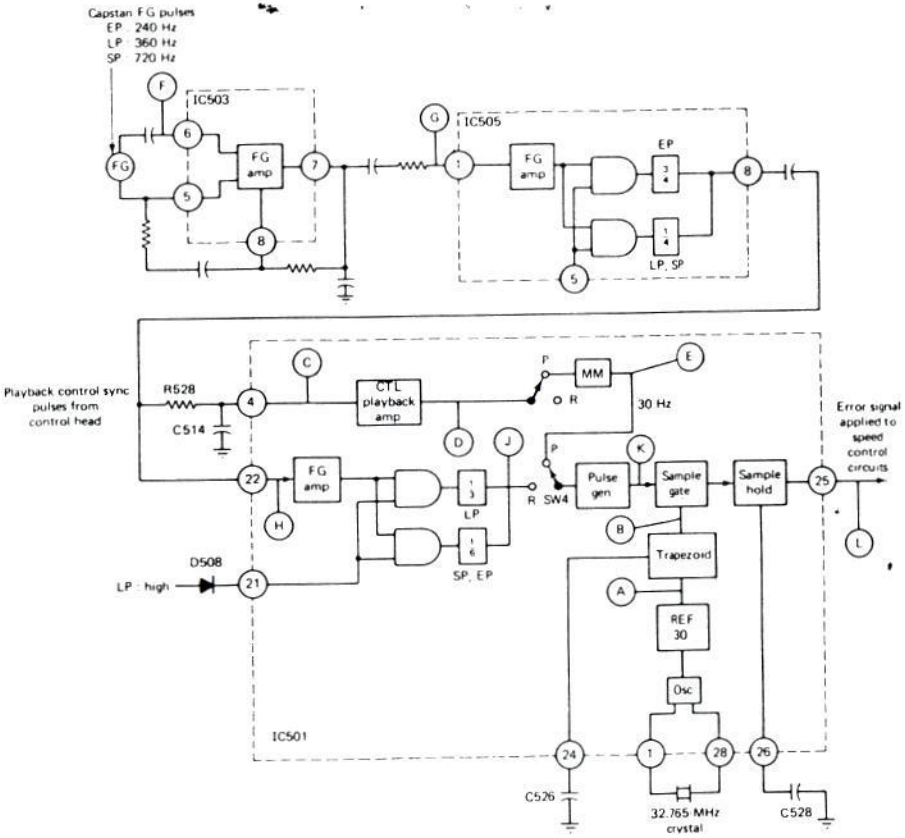


FIGURE 4-26. Capstan phase control circuit.

for a discussion of the operating modes. During playback, the control pulse recorded on the control track during record is detected by the control head and used as the comparison signal.

During record, the capstan FG pulses are amplified by the FG amplifier in IC503. The output from pin 7 of IC503 is applied through pin 1 of IC505 and control gates to a divider circuit. The FG pulses are divided by $\frac{1}{4}$ in the LP and SP modes and by $\frac{3}{4}$ in the EP mode. The output from pin 8 of IC505 is applied through pin 22 of IC501, another FG amplifier, and control gates, to another divider circuit. The FG pulses are further divided by $\frac{1}{6}$ in the SP and EP modes and by $\frac{1}{3}$ in the LP mode.

During playback, the control pulse picked up by the control head is applied to a monostable multivibrator through pin 4 of IC501, low-pass filter C514 and R528, and a control playback amplifier. The 30-Hz playback pulse triggers the multivibrator, which produces a 30-Hz rectangular pulse.

During either playback or record, the pulse generator receives a 30-Hz reference signal through switch SW4. The rectang[illegible] pulse supplied to the pulse

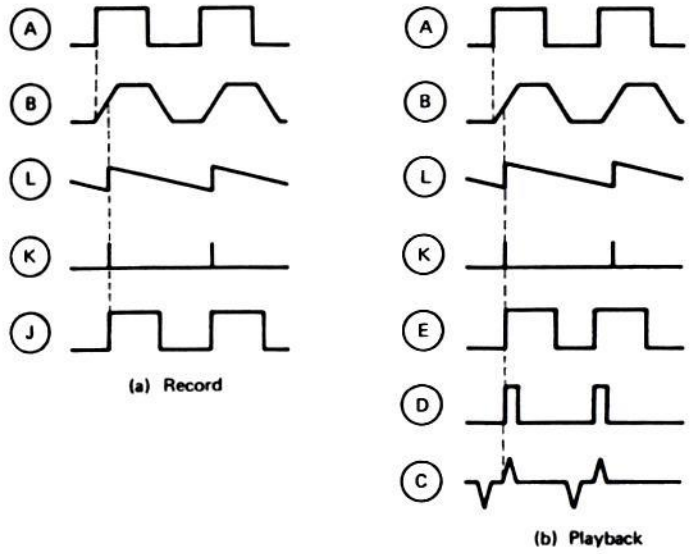


FIGURE 4-27. Waveforms associated with capstan phase control circuit.

generator is converted to a sampling pulse and applied to the S/H circuit as the comparison signal. The S/H circuit also receives a reference signal in the form of a trapezoidal wave. This trapezoidal waveform is obtained by dividing the 32.765-MHz signal (developed by the crystal oscillator) by 1093. The divided signal (in the form of a 29.98-Hz rectangular wave) is converted to a trapezoidal waveform (waveform B in Fig. 4-27).

The trapezoidal wave is sampled in the S/H circuit by the 30-Hz signal produced by the control pulse generator. This produces an error voltage corresponding to the phase difference. The error voltage is applied to the speed control circuits through pin 25. Capacitor C528 holds the error voltage between samplings. Capacitor C526 determines the time constant of the trapezoidal wave.

Basically, the sampling action of the capstan phase control system is similar to that of the cylinder phase control system (Sec. 4-5.1). The difference is, in the capstan servo, the reference signal is the trapezoidal wave and the comparison signal is the sampling pulse. As a result, the sampling position is on the leading edge of the trapezoidal wave (whereas the position is on the trailing edge for the cylinder phase control). When the capstan motor is at the correct speed, the sampling position is at the middle of the ramp as shown in Fig. 4-28. When the capstan motor speeds up slightly, the phase of the comparison signal advances with respect to the reference signal as shown in Fig. 4-29. As a result, the sampling position moves lower on the ramp, and the error voltage is reduced, decreasing motor speed. If the capstan motor slows down, the phase of the comparison signal lags behind the reference signal as shown in Fig. 4-30. As a result, the sampling position moves up the ramp and the error voltage increases, increasing motor speed.

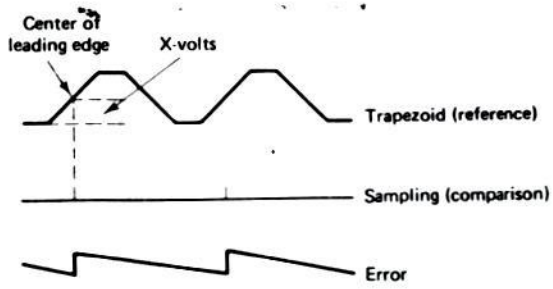


FIGURE 4-28. Relationship of pulses when capstan speed is normal.

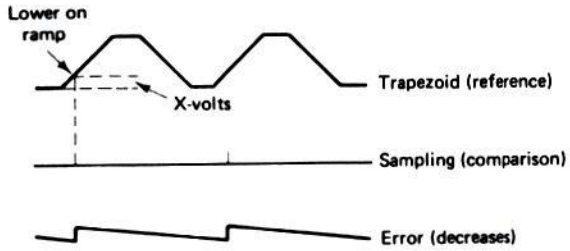


FIGURE 4-29. Relationship of pulses when capstan speed increases.

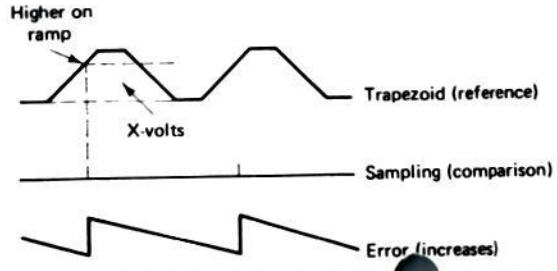


FIGURE 4-30. Relationship of pulses when capstan speed decreases.

As in the case of cylinder phase control, the error voltage developed by the capstan phase control system is limited to that which can be detected on the slope of the ramp and is used only as a vernier speed control (or phasing control) voltage. The actual speed of the capstan motor is controlled by the speed control circuit as discussed in Sec. 4–5.3.

4–5.3 Speed Control Circuit

Figure 4–31 is the overall block diagram of the cylinder speed control circuit. Figure 4–32 shows the related waveforms. A similar circuit is used for capstan speed control.

As shown in Fig. 4–31, the 120-Hz signal output from the cylinder FG is applied to the FG amplifier through pin 6 of IC502 and C543. The FG amplifier has a differential input at terminals 5 and 6 and a feedback output at pin 8. A reference voltage applied to pin 5 is adjusted by R506. The feedback signal is applied through R593 and C549. The output of the FG amplifier is applied to a delay circuit, and to a S/H circuit, through a doubler and former circuit. The signal is shaped by the former and converted to double frequency by the doubler. The delay circuit produces an approximate 20μs delay.

The output from the delay circuit is used as the trigger for the sawtooth generator, which produces a sawtooth wave. The slope of the sawtooth waveform is determined by the time constant of the "C" and "R" connected to pins 11 and 9, respectively. Note that the resistance is made adjustable so that the speed can be set. As the sawtooth wave slope becomes sharper, speed increases.

The output of the sawtooth generator is applied to the S/H circuit, which also receives a delayed sampling pulse from the delay circuit. Capacitor C536 holds the voltage between samplings. The two inputs to the S/H circuit produce an error voltage output at pin 13 (waveform G in Fig. 4–32). The error voltage is applied to the cylinder motor drive (Sec. 4–5.4) through an adder, comparator, amplifier, and motor switch.

The sampling action is shown in Figs. 4–33, 4–34, and 4–35. As shown in Fig. 4–33, the sawtooth ramp is sampled at a fixed level determined by the delayed sample pulse amplitude. Since the lag is constant, when motor speed increases, the sawtooth ramp is steeper, the sampling position moves lower on the ramp, and the error voltage is reduced, as shown in Fig. 4–34. This reduces motor speed. When motor speed is reduced, the sawtooth ramp is less steep, the sampling position moves higher on the ramp, and the error voltage is increased, as shown in Fig. 4–35. This increases motor speed.

The error signal at pin 13 is passed through a low-pass filter composed of R560 and C535 (to remove the sampling frequency component) and applied to the adder through pin 14. The adder also receives an error signal from the phase control circuit (Sec. 4–5.1). The two error signals are added and applied to the motor drive at pin 3 as the speed control signal (Sec. 4–5.4).

The comparator compares the sum of the speed control, phase [illegible]rol, and

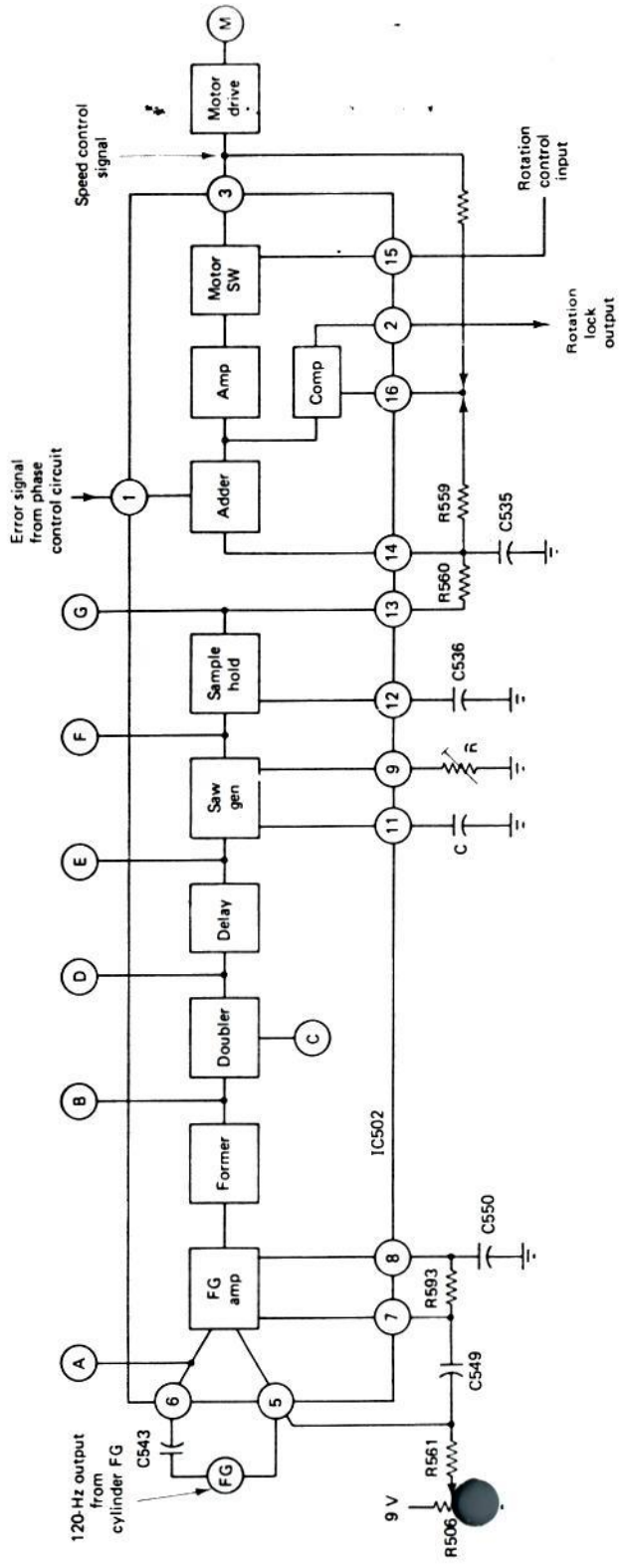


FIGURE 4–31. Cylinder speed control circuit.

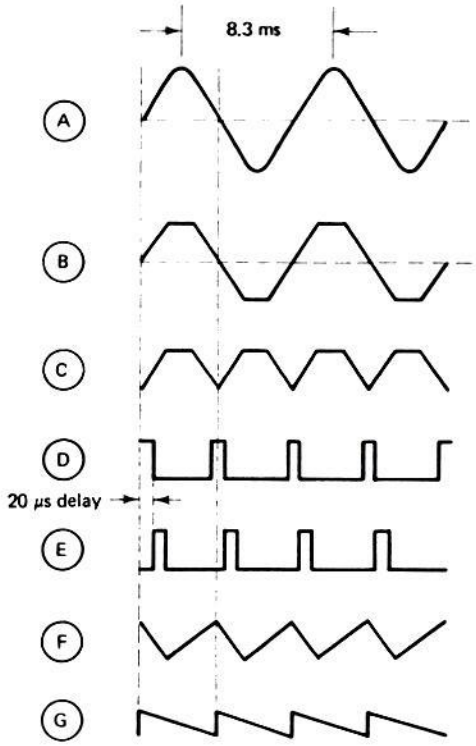


FIGURE 4-32. Waveforms associated with cylinder speed control circuit.

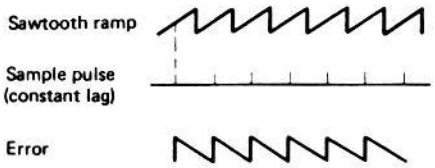


FIGURE 4-33. Sampling action when cylinder speed is normal.

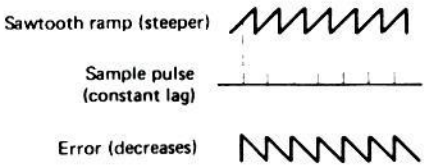


FIGURE 4-34. Sampling action when cylinder speed increases.

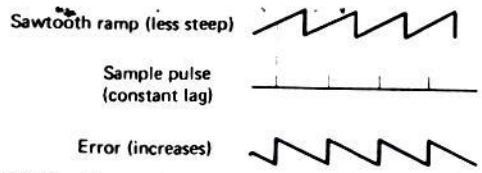


FIGURE 4-35. Sampling action when cylinder speed decreases.

reference voltage outputs. If the motor slows down for any reason (to a point where the servo cannot control the speed properly), pin 2 goes high and the motor stops (as discussed in Sec. 4-6). Pin 2 is normally low.

4-5.4 *Motor Drive Circuit*

Both the cylinder motor and capstan motor are three-phase motors. Figure 4-36 shows the positions of the rotor, stator coils, and Hall element devices of the capstan motor, while Fig. 4-37 shows the same elements for the cylinder motor. (Hall elements operate on the Hall effect principle, and produce a current that is controlled by the magnetic field surrounding the element. When the magnetic field is alternating, the output current from the Hall element alternates.)

Figure 4-38 shows the basic motor drive circuit. Figure 4-39 shows the

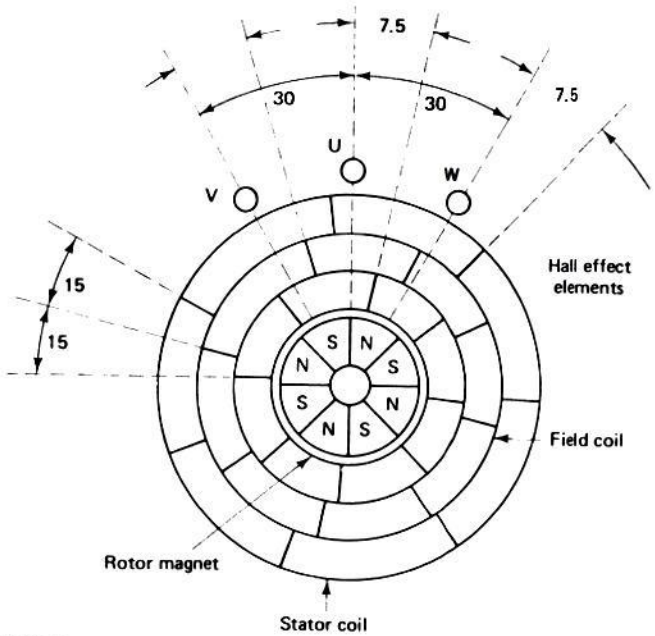


FIGURE 4-36. Positions of rotor, stator coils, and Hall element devices of capstan motor.

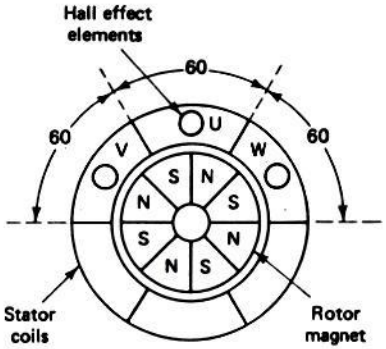


FIGURE 4-37. Positions of rotor, stator coils, and Hall element devices of cylinder motor.

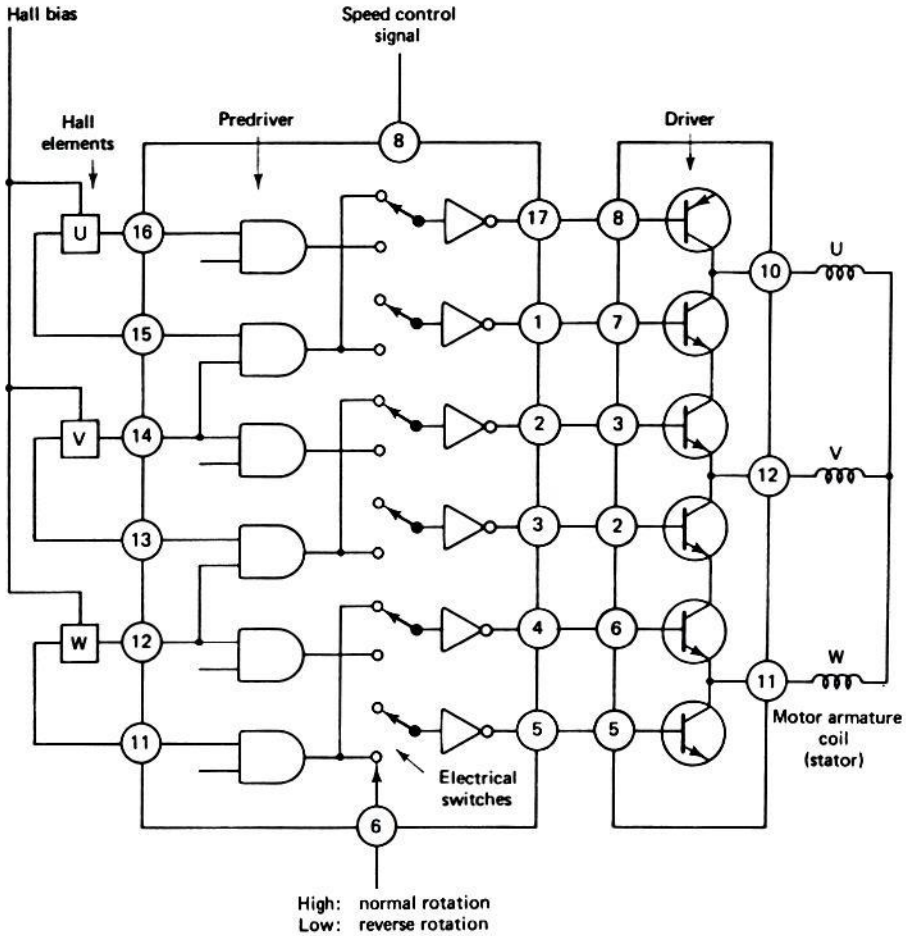


FIGURE 4-38. Basic motor drive circuit.

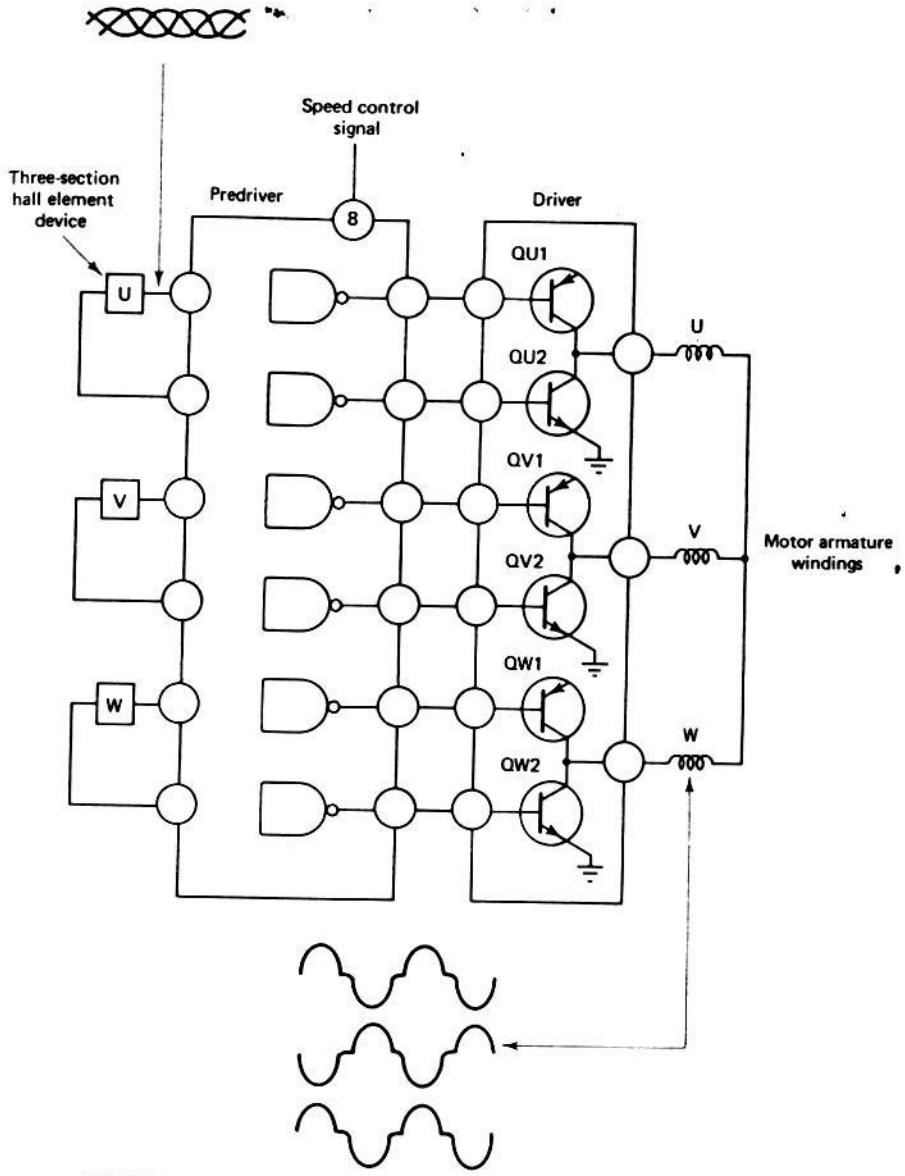


FIGURE 4-39. Cylinder motor drive circuit and related waveforms.

drive circuit for the cylinder motor and related waveforms. As shown, the motor drive system is composed of a Hall element device, a motor predriver, and a driver. When the motor turns, the polarity of the magnetic field applied to the Hall element alternates (because of rotation by the rotor magnet). This produces

a three-phase sine wave with phases U, V, and W (separated in phase by $\frac{2}{3}\pi$) obtained from the Hall element device. The three-phase sine wave is selected and amplified by the predriver, and the resultant current is applied to the motor armature by the driver.

The drive systems of the capstan motor and cylinder motor are essentially the same. However, the cylinder motor does not have a motor reversal provision (at pin 6 as shown in Fig. 4–38).

As shown in Fig. 4–39, the cylinder motor has a three-section Hall element device. The signal obtained from this device is actually a six-phase sine wave. The predriver selects three pairs of Hall element outputs and converts them to three pairs of controlled outputs which are applied to transistors within the driver. Transistors QU1, QV1, and QW1 are active-low and control the current applied to the corresponding armature windings of the motor. Transistors QU2, QV2, and QW2 are active-high, and ground the corresponding windings.

Motor speed depends on the current supplied to the windings. In turn, the amount of current depends on the amplitude of the speed control signal (Sec. 4–5.3) applied to pin 8. The direction of rotation for the cylinder motor is always the same, and only motor speed is subject to control. In the case of the capstan motor, both speed and direction of rotation are controlled. Pin 6 of the predriver is normally high. However, when the capstan must be reversed, pin 6 goes low and the electrical switches within the predriver go to the low position. This reverses the polarity of all three phases of the motor drive signals.

4-6 VHS SYSTEM CONTROL CIRCUIT

Operation of the system control circuit is determined primarily by microprocessors. The use of such microprocessors for system control is typical for many present-day VCRs. The microprocessors accept logic control signals from the VCR operating controls (called operation keys) and from various tape sensors. In turn, the microprocessor sends control signals to the various circuits, as well as drive signals to solenoids and motors.

We will not go into operation of microprocessors here since such information is beyond the scope of this book (and each VCR has its own particular microprocessor applications). However, we do discuss the circuit inputs and outputs to and from the microprocessor, since such circuits are typical for many VCRs. If you want a thorough discussion of microprocessors, your attention is invited to the author's best-selling *Handbook of Microprocessors, Microcomputers, and Minicomputers* (Englewood Cliffs, N.J.: Prentice-Hall, Inc., 1979).

Note that many system control functions are closely related to mechanical operation of the VCR, as described in Chapter 5. Therefore, it is essential that you study the related sections of Chapter 5 when reviewing system control operation.

4-6.1 Overall System Control Circuit Operations

Figure 4–40 is an overall block diagram of the system control circuits. As shown, system control includes microprocessor IC901, which reads in and decodes data from interfaces (from both sensors and operation keys), and microprocessor IC902, which receives decoded sensor and operation key information from IC901. Microprocessor IC901 sends control signals to the main brake and take-

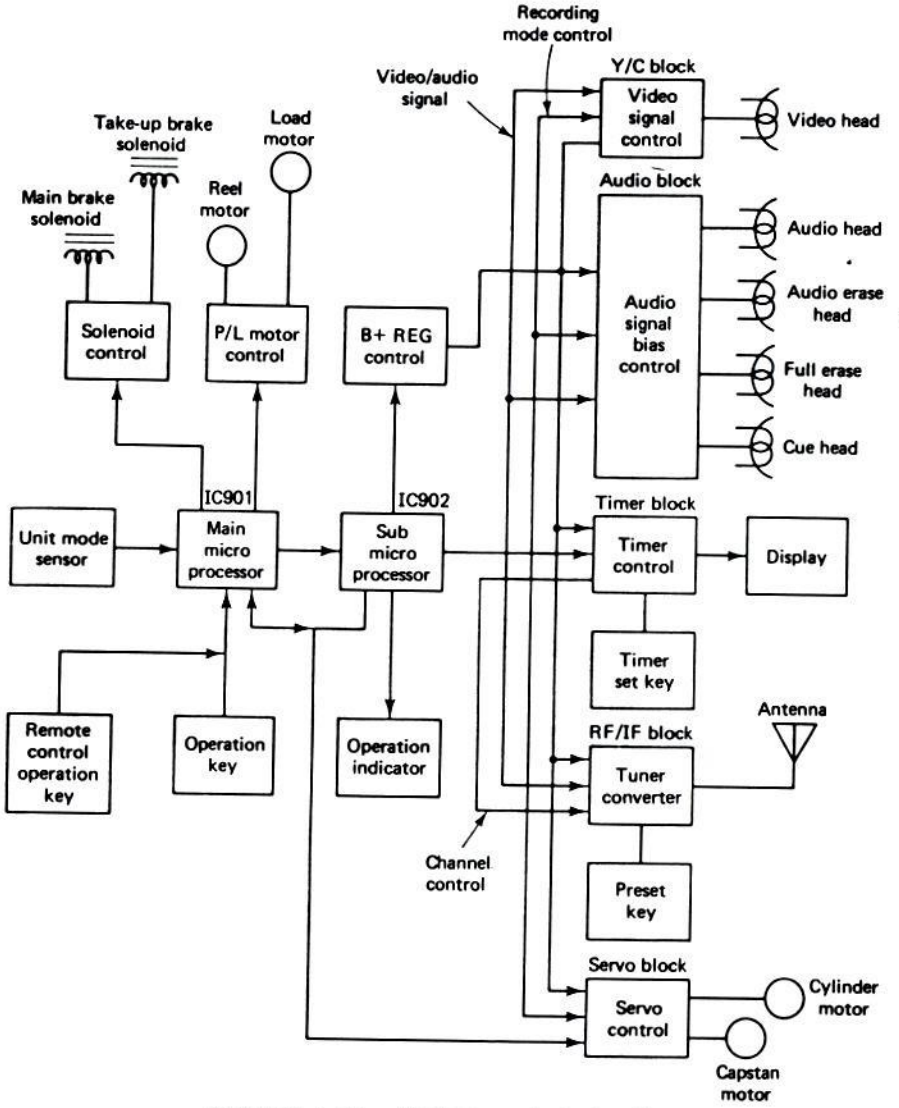


FIGURE 4-40. System control circuits.

up brake solenoids, as well as the reel and load motors. All the remaining control signal outputs come from IC902, which also provides corresponding outputs to the operating indicators (PLAY indicator lamp, REC indicator lamp, etc.).

4-6.2 Operating Key Input

Figure 4-41 shows the basic operation key input circuits. To reduce the number of operation key input lines to IC901, the key operation for each of the 14 modes is converted into a 14-step voltage (designated as V1). This voltage V1 is compared with a voltage V2 produced by a 4-bit D/A (digital-to-analog) converter. IC901 pins 36 to 39 serve as the D/A input. The emitter resistance of Q2 is

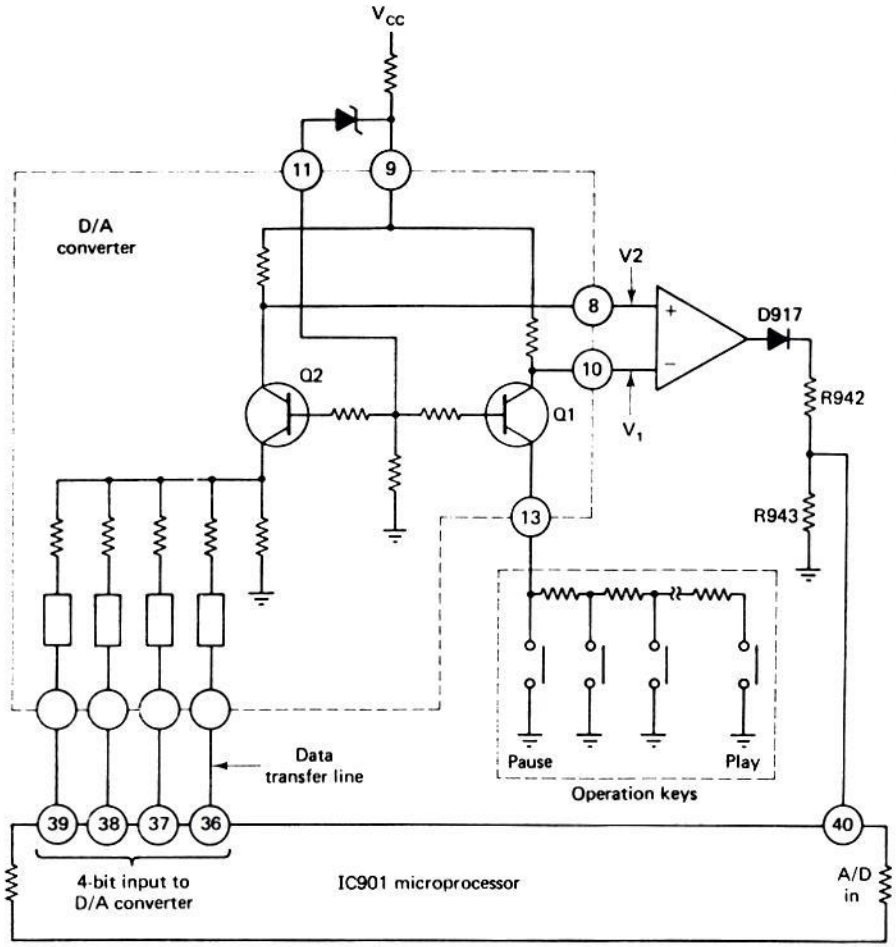


FIGURE 4-41. Operation key input circuits.

changed in 16 steps by means of this input from IC901, thus generating a 16-step voltage V2. The 14-step voltage V1, which corresponds to the selected operation key, is generated by varying the emitter resistance of Q1.

Pin 40 is the input to IC901 for comparison of V1 and V2. Each time the D/A converter counts one step, IC901 checks the comparison at pin 40 to determine the point where V2 is greater than V1 (when the 16-step voltage has reached the selected operation key voltage). When this occurs, IC901 sends the necessary control and indicator signals to IC902. Note that pins 36 to 39 of IC901 form the data transfer line to IC902, as discussed in Sec. 4-6.3.

If you are not familiar with operation of D/A converters, or A/D converters, your attention is invited to the author's best-selling *Handbook of Digital Electronics* (Englewood Cliffs, N.J.: Prentice-Hall, Inc., 1981).

4-6.3 Data Transfer and Read-In

Figure 4-42 shows the relationship between microprocessors IC901 and IC902. The outputs from IC902 are applied to the mode and indicator control circuits. The control signals from IC901 to IC902 are passed (using time sharing) through the 4-bit transfer line, and a 1-bit timing control line (pin 1 of IC901 and pin 8 of IC902). This 5-bit system allows the number of output lines to be reduced.

The 1-bit timing control pulse (pin 1 of IC901) is known as the TX pulse and is used to synchronize operating modes of both ICs. Data bits are stored in IC902

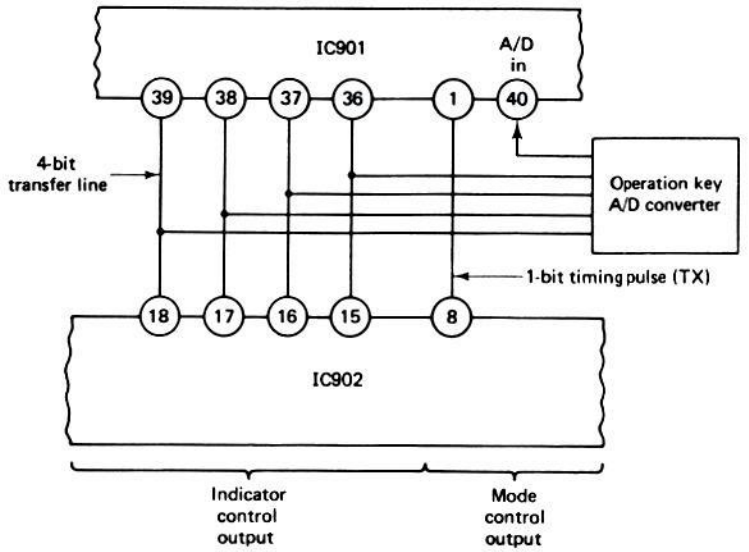


FIGURE 4-42. Relationship between IC901 and IC902 in system control.

until the next data byte is transferred. Data transfer is performed periodically to prevent the information from being altered by noise, and so on. The data bits are renewed repeatedly so that information from IC901 coincides with that of IC902.

4-6.4 Operation Mode Control

As shown in Fig. 4-40, when the operation keys are pressed, signals to indicate the circuit composition and mode (operation indicator) are produced, simultaneously with the mechanism drive outputs for loading, unloading, and so on. The outputs (both indicator and control) continue until a different operation key is pushed. The following is a summary of the 14 operating modes.

In the STOP mode, unloading is completed; the cylinder motor, capstan motor, and reel motor stop; the main brake is applied; and the STOP indicator is lit by the output of IC902 pin 1. When entering the STOP mode from the REC (record) and PLAY modes which require unloading, unloading continues until all the stop functions are performed, but the STOP indicator lights before the start of unloading. IC902 is reset when the POWER switch is turned off and on. However, when the POWER switch is not yet turned on after IC901 is reset, the STOP indicator does not light, but the mechanism condition is the same as in the STOP mode. When the power plug is pulled out, or a power failure occurs during a certain operation, IC901 is reset and the mechanism enters the same mode as the STOP mode (after unloading is completed).

When the PAUSE operation is performed in the STOP mode, the PAUSE indicator is lit by the output of IC902 pin 2. (PAUSE is called FREEZE or FREEZE FRAME in some VCRs.) However, the mechanism keeps in the STOP mode. When going to PAUSE from PLAY, REC, or DUB operation, the PAUSE is latched by IC902 and the VCR enters the corresponding PAUSE mode (a freeze frame picture appears on the TV).

When the PLAY operation is performed, the PLAY indicator is lit by the output of IC902 pin 7, a PB 9V is generated by the output of pin 19, and the loading operation is performed. The PB 9V is applied to audio/video/servo circuits as necessary to perform the playback operation.

The following operations are possible after the PLAY operation has been selected:

With the PAUSE button pressed during playback, the PAUSE indicator is lit and the VCR is in the STILL mode.

With the VCR in the STILL mode, the frame advances each time the FRAME ADVANCE button is pressed.

When the SLOW button is pressed during playback, the capstan servo system is controlled to play at one-half speed.

When the QUICK button is pressed, the capstan servo system is controlled to play at three times normal speed.

When the VIDEO SCANNING ►► mode button is pressed during playback, the capstan servo system is controlled to play at 10 times the EP (extended play) speed. (This mode is called SEARCH or VIDEO SEARCH in some VCRs.)

When the VIDEO SCANNING ◄◄ mode button is pressed during playback, the capstan servo system is controlled to play in the reverse direction at 10 times the EP speed. Reverse play is performed by turning the capstan motor in reverse (Sec. 4-5.4). The tape is taken up by driving the tape supply reel disk with the reel motor. If the VCR is kept in the reverse video scanning mode for more than about 5 minutes, the operation changes over to normal playback. This is to protect the reel motor. Operation of the reel motors is discussed further in Sec. 4-6.7.

The following modes require that the PLAY button be pressed (either simultaneously with, or after, the desired operating mode button is pressed):

When the RECORD button is pressed and the cassette safety tab is not broken, a REC 9V is generated by the output of pin 20, and the audio/video/servo circuits are changed over to the record mode. If the cassette safety tab is broken (Sec. 1-10.2), the record mode is disabled.

When the PAUSE button is pressed in the RECORD mode, the capstan motor turns slightly in reverse and rewinds tape to improve phase matching. Then the loading motor turns in reverse to release the pressure roller from the capstan shaft. The capstan motor continues turning. The PAUSE indicator is also lit. Figure 4-43 shows this sequence.

When the DUB button is pressed and the cassette safety tab is not broken, a PB 9V is generated, the video/servo systems enter the PLAY mode, and the audio system enters the RECORD mode. Under these conditions, audio (from an external microphone or other audio source) is recorded on the audio track of the tape.

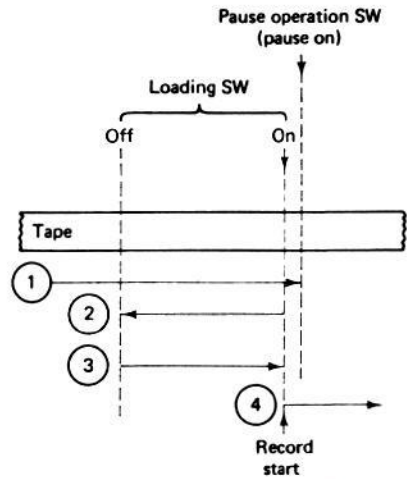


FIGURE 4-43. Sequence when the PAUSE button is pressed in the RECORD mode.

When the PAUSE button is pressed after the DUB button is pressed, the VCR enters the DUB PAUSE mode. The condition of the mechanism is the same as in the STILL mode. The PLAY/DUB/PAUSE indicators are lit.

The following modes do not require that the PLAY button be pressed:

When the F FWD (fast forward) button is pressed, the loading motor rotates normally and a supply brake pressure is applied to the supply reel (to provide back-tension). The reel motor then turns, compressing the FF/REW idler against the take-up reel disk, and the tape is taken up. The F FWD indicator is lit.

When the REWIND button is pressed, the reel motor drives the supply reel to take up the tape.

4-6.5 Stop Control

The VCR is placed in the STOP mode when the STOP button is pressed, when the tape runs to either end (forward and reverse), and when there is mechanical trouble. Figure 4–44 shows the circuits involved. The following summarizes operation of the stop control circuits.

End Sensor Circuit. Both ends of VHS tape are clear (transparent) plastic. The cassette tape passes between an end sensor lamp (also known as a cassette lamp in some VCRs), and two end sensor photo transistors Q81 and Q82. The magnetic portion of the tape prevents the cassette light from reaching the photo transistors. When the tape reaches either end (supply or take-up), the cassette light passes through the transparent portion of the tape onto one end of the end sensor photo transistors. When either Q81 or Q82 receive light, they produce a signal (of about 5 V) to pin 24 (supply) or 25 (take-up) of IC901. This stops and unloads the VCR.

End Sensor Lamp Failure Detector. Should the end sensor lamp burn out or fail for any reason, the VCR is placed in the STOP mode. If this feature were not included, the tape could be broken when run to either end. The end sensor lamp is connected in parallel across ZD904 and R928. If the lamp burns out, the cathode of DZ904 increases. This increase is applied to pin 33 of IC901 through the OR gate and places the VCR in STOP.

Dew Sensor Circuit. The dew sensor output is also applied to pin 33 of IC901 through the OR gate. When humidity is less than about 80%, the resistance of the dew sensor is about 100 MΩ. When humidity increases over 80%, the resistance is less than 3 MΩ and the voltage at the junction of dew sensor R82 and R935 increases. This increase is applied to pin 33 of IC901 and places the VCR in STOP. The STOP indicator flashes to indicate that condensation is present.

Reel Lock Circuit. This circuit detects when the reel motor has stopped rotating, except during modes when the tape should not be running at the normal speed (UNLOADING, LOADING, PAUSE, STOP, SLOW PLAYBACK). NAND gate Q905 is active when the reel disk is rotating, or when operating mode

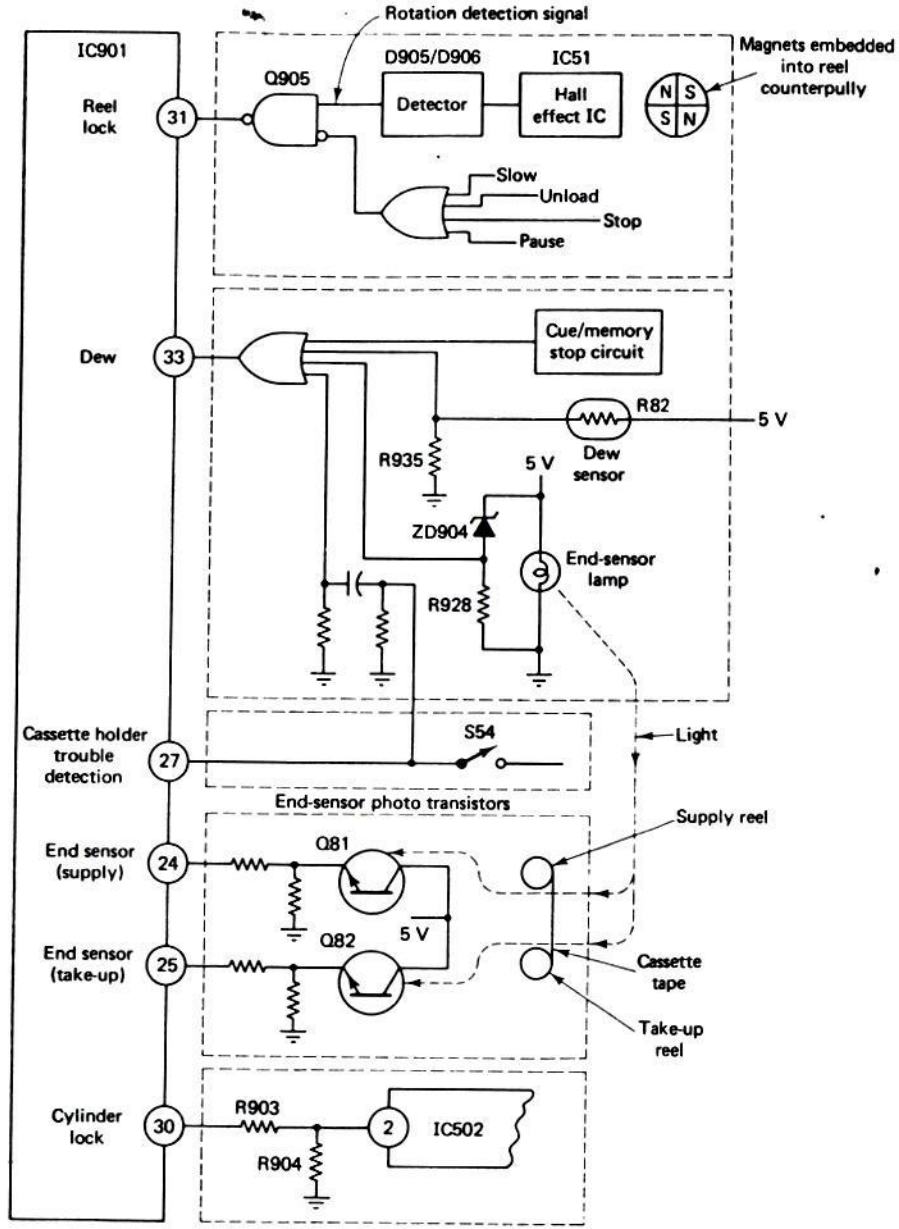


FIGURE 4-44. Stop control circuit.

signals are applied to the OR gate. When reel rotation stops, Q905 is cut off, and IC901 produces unloading and stop after about 8 to 10 s. This is prevented by override mode signals applied to the OR gate. These mode signals take the place of the rotation detection signal.

The rotation detection signal is developed by detectors D905/D906 (which act as a voltage doubler and rectifier), a Hall effect element IC51, and magnets embedded into the reel counterpully. When the reel is rotating, the magnetic field also rotates and causes the Hall IC to produce an alternating current. This alternating current is rectified and doubled by D905/D906 to become the rotation detection signal. If rotation stops, the alternating current stops, as does the detection signal.

Cylinder Lock Circuit. This circuit detects when the cylinder motor stops rotating, or when rotation slows down to a point where the servo can no longer provide proper control. As discussed in Sec. 4–5.3, pin 2 of the cylinder motor speed control IC502 is normally low. When cylinder motor speed drops below a certain point, pin 2 goes high. This high is applied to pin 30 of IC901, through R903/R904, and IC901 instructs unloading and stop.

Cassette Holder Trouble Detection. This circuit detects if the cassette holder is in the eject condition. Switch S54 is operated by the holder. If the eject button has been pushed, the VCR is placed in the STOP mode by switch S54.

4-6.6 Cue/Memory Counter Circuit

Figure 4–45 shows the cue/memory counter circuits in simplified form. The VCR has a tape counter known as the memory counter. This counter displays a number that increases as the tape moves forward and decreases as the tape moves backward. If you make a note of the number corresponding to a particular point on the tape, you can use the counter to help you locate that place. The VCR also has a cueing circuit which records a signal on tape at the start of a program (to detect the start of the program during playback).

Memory Counter Circuit. The counter has a memory capability. To use the memory, you stop the tape at the point you want to return to later, and set the counter reading to "000." To detect that position after running the tape, set switch S2001 to M (memory) and perform rewind. When the VCR rewinds to "000" (actually "999," or one count before "000" in order to avoid missing the starting point), the VCR goes into STOP. This is done when the counter switch closes, applying a 9-V signal to pin 33 of IC901 through Q2003 and D2001. Pin 33 is the same stop control input to IC901 used by the dew sensor, lamp failure detector, and so on, described in Sec. 4–6.5.

Cueing Circuit. The cueing circuit involves both record and playback functions. The cueing signal recorded on tape is obtained from the SW30 signal. This 30-Hz signal is superimposed on the full-erase head bias signal through

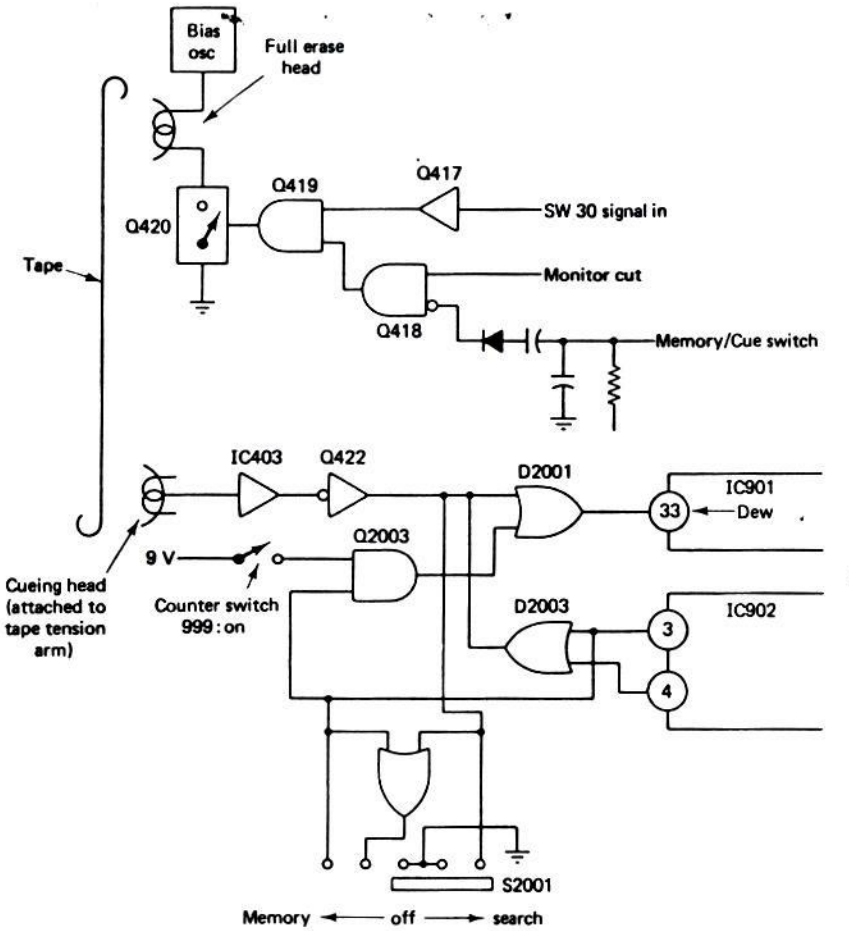


FIGURE 4–45. Cue/memory counter circuit.

Q417, Q419, and Q420. The recording period of the cueing signal is regulated by the time constant circuit connected to the base of Q418 during the trailing edge of the monitor signal. This monitor signal occurs (each time the RECORD button is pressed) during the loading period (at the time the tape is loading for a recording). The SW30 signal is transmitted to the full-erase head at that time, provided that the memory/cue switch is set to cue.

The cueing signal is picked up by the cueing head attached to the tape tension arm, when the memory/cue switch is set to cue, and the servo is operated in the fast forward or rewind modes. Under these conditions, the trailing edge of the recorded SW30 signal is detected by the cueing head is applied to pin 33 of IC901, causing the VCR to go into STOP mode. If several programs have been recorded on tape, with the RECORD button pressed at the beginning of each program, the VCR will stop at each program (during fast forward or rewind).

4-6.7 Loading Motor/Reel Motor Control

Figure 4–46 shows the loading and reel motor control circuits. As shown, the loading and reel motors are controlled by signals from microprocessor IC901 using negative logic (a low output from the IC produces the necessary control action). The microprocessor provides six specific instructions. The reel motor receives a fast-forward control (pin 7, IC901), a rewind control (pin 8), and slow-speed forward control (pin 9). The loading motor receives a loading control (pin 5), an unloading control (pin 6), and a brake control (pin 10).

A tristate signal is applied to the terminals of both the loading and reel motors as necessary. This tristate signal is (1) about 10 V, (2) 0 V or ground, and (3) high-impedance or open. Switches S1 through S6 control these signals. The switches are controlled by logic circuits within IC905 and IC906, which, in turn, are controlled by the six instructions from IC901. When no instruction is produced by IC901, both terminals are set to the high-impedance or open condition. During braking, both terminals are set to 0 V or ground, thus short circuiting the motor. During other instructions, one terminal is connected to 10 V with the opposite terminal connected to ground, causing the motor to rotate in the desired

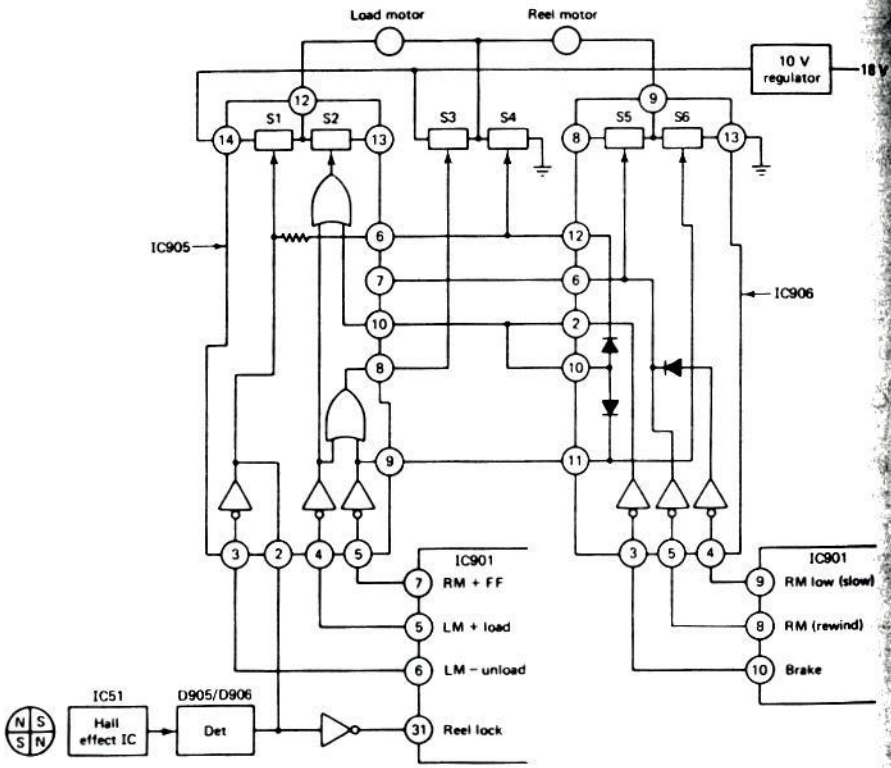


FIGURE 4–46. Loading and reel motor control circuits

direction. When the slow-speed forward control is applied to the reel motor, one terminal is connected to 5 V with the opposite terminal connected to ground. This causes the reel motor to rotate in the forward direction, but at a reduced speed.

4-6.8 Main Brake Solenoid Control

Figure 4–47 shows the main brake solenoid control circuit and associated waveforms. The main brake solenoid applies braking to both reels in the STOP mode or in a mode transition period. This prevents tape slack. The main brake solenoid releases braking when conducting and its shaft is actuated. This conducting state is latched electrically. IC901 produces 50-ms pulses at pins 12 and 13. These pulses trigger the latching action.

For example, when the brake is to be turned off, the 50-ms pulse at pin 12 is inverted by Q53 and causes Q54 to close for 50 ms. This connects the control side of the main brake solenoid to ground, full current is applied, the brake shaft is actuated, and the brake is released. The brake is held in this condition by the latching action. When Q54 closes, the input to Q51 is connected to ground, through R55. This produces a 50-ms low which is inverted to a high by Q51. The high at the output of Q51 closes Q52 and connects the control side of the braking solenoid to ground through R55. This provides sufficient current to hold the solenoid in the brake release condition.

When the brake is to be applied, the negative 50-ms pulse at pin 13 is applied to Q52, causing Q52 to open and disconnecting the brake solenoid from the ground.

4-6.9 Take-Up Brake Solenoid Control

Figure 4–48 shows the take-up brake solenoid control circuit and associated waveforms. Braking is applied to the take-up reel to prevent the tape from being pulled out of the take-up reel during loading and unloading (to provide some back tension on the tape). Braking is also applied during reverse scanning (or reverse visual search) to provide back tension on the tape.

The take-up brake solenoid is controlled by negative pulses from pin 11 of IC901 (except during reverse scanning when the pulses are taken from pins 3 and 4). The take-up brake instruction from pin 11 is inverted by Q907 and applied through D927/D904, and a differentiating network consisting of C51/R64, to Q56. The signal from D927/D924 is also applied directly to Q55. The differentiated signal causes Q56 to close, full current is applied to the solenoid, and the brake is applied momentarily. The brake is held in this condition temporarily by latching action. When Q55 closes, the control side of the braking solenoid is connected to ground through R65. This provides sufficient current to hold the solenoid in the braking condition. During all modes except reverse scanning, the brake is applied long enough to complete the loading and unloading operation.

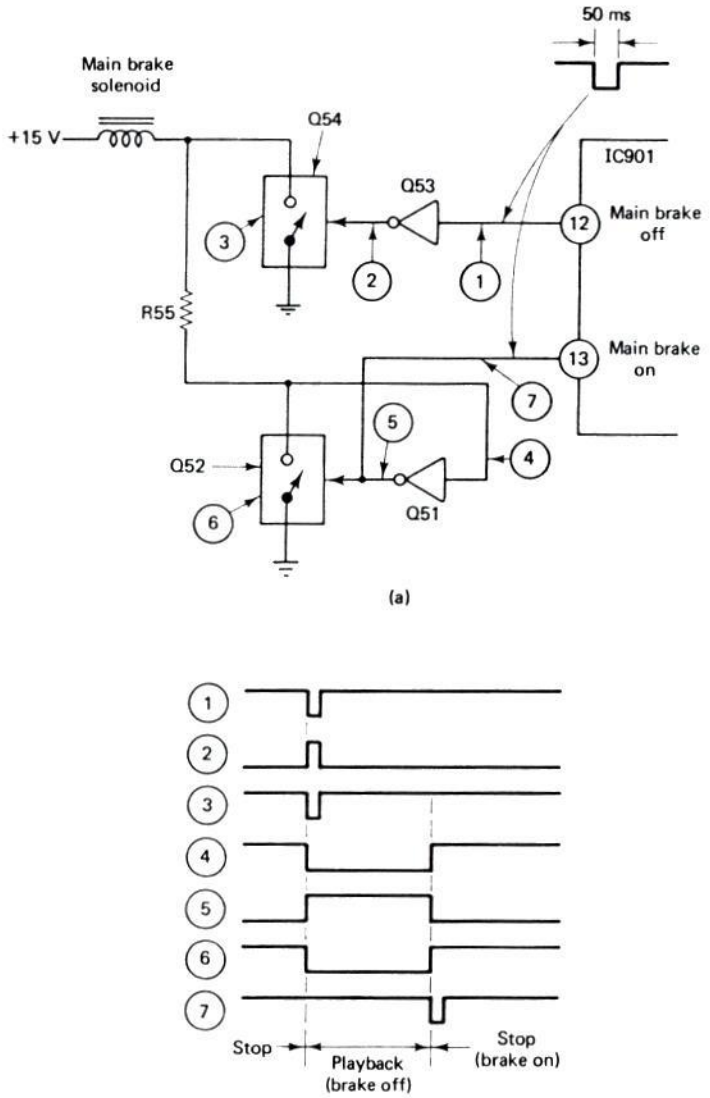


FIGURE 4-47. Main brake solenoid control circuit and associated waveforms.

During reverse scanning, continuous low signals appear at pins 3 and 4, producing a high at the output of Q903. This high causes Q55 and Q56 to close, full current is applied, and the brake is applied. Q56 opens once the differentiated pulse passes, but Q55 remains closed since Q55 is connected directly to the output of D927/D904. With Q55 closed, the solenoid is connected ground

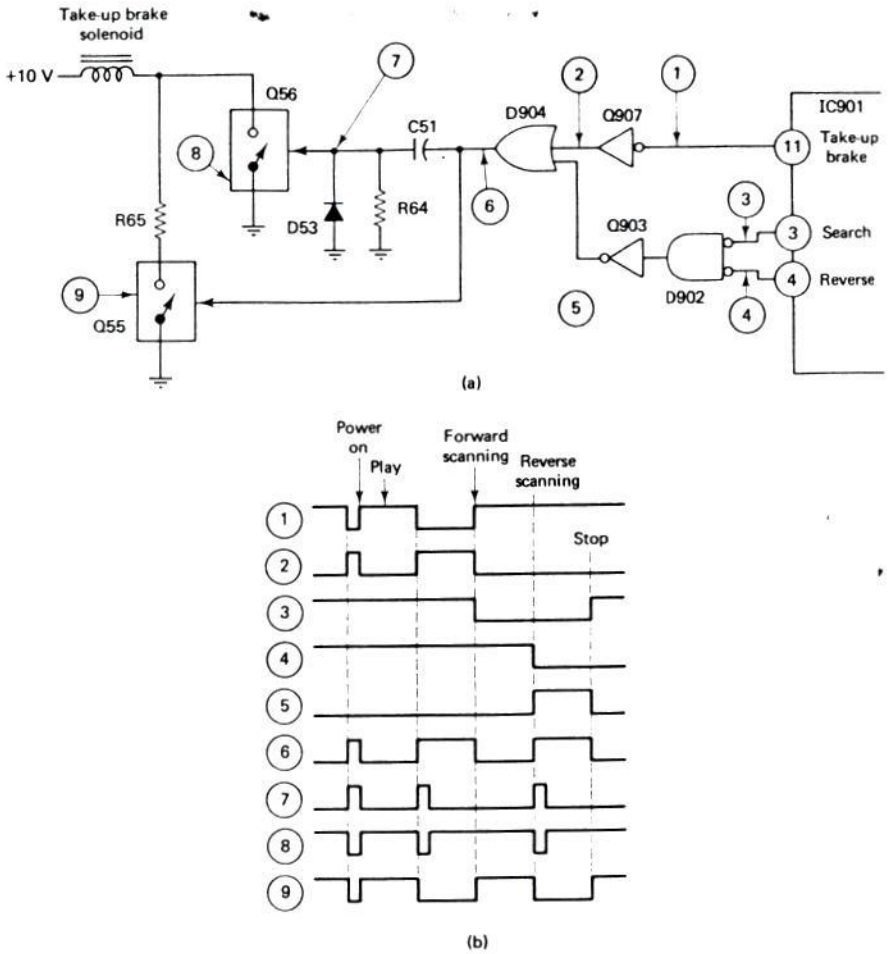
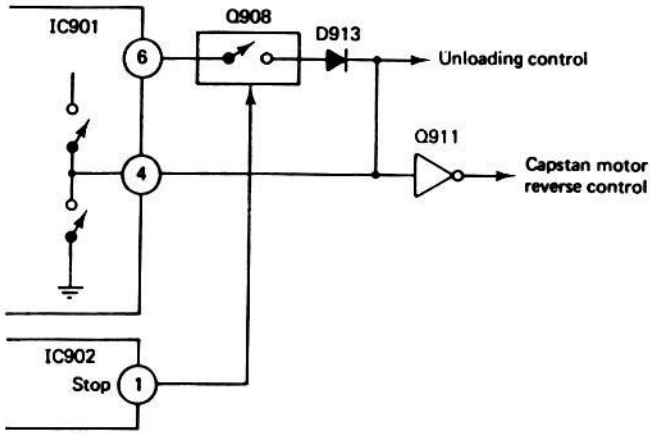


FIGURE 4-48. Take-up brake solenoid control circuit and associated waveforms.

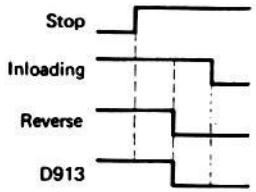
through R65. This provides sufficient current to hold the solenoid in the braking condition, as long as the signals at pins 3 and 4 of IC901 are applied during reverse scanning.

4-6.10 Tape Protection Control

Figure 4-49 shows the tape protection control circuit and associated waveforms. The purpose of this circuit is to prevent the tape from breaking when a reverse instruction is given from a fast-forward condition. This can be accomplished if the unloading instruction occurs simultaneously with the reverse instruction. When the stop instruction is given, braking is applied to the take-up reel first and, after



(a)



(b)

FIGURE 4-49. Tape protection control circuit and associated waveforms.

about 50 ms, a reverse rotation instruction is applied to the capstan motor. Next, a reverse rotation instruction is given to the supply reel, and the loading motor is reverse rotated to remove slack. This moves the guide base to the stop position, and feeds tape into the cassette.

The supply reel rotates at slow speed before the loading motor starts rotation and, after that, at fast speed in the reverse direction. The capstan motor is first braked and stopped by the reverse instruction, and then the capstan motor begins to rotate in the reverse direction. However, in the forward scanning mode, the capstan motor rotates at 10 times normal speed (10 times EP), so reversal is delayed due to the flywheel effect of the motor when the reverse instruction is first given. Under these conditions, it is possible that when the supply reel starts to rotate in the reverse direction, the capstan motor could still be rotating in the forward direction. In such a case, the tape could be pulled in both directions simultaneously, resulting in tape breakage.

To protect the tape from such breakage, unloading is performed to release

the compression of the capstan and pressure roller (pinch roller), simultaneously when a reverse instruction is given. This is accomplished by the circuit of Fig. 4-49. When the stop instruction at pin 1 of IC902 is applied to Q908, the unloading control signal at pin 6 of IC901 is applied to pin 4 of IC901 and to the capstan motor reverse control circuit simultaneously. Therefore, unloading and capstan reverse control are performed simultaneously.