SONY®

Training Manual

Projection Television

Circuit Description and Troubleshooting

Course: TVP-08

Course Description and Troubleshooting:
RA-4 Chassis

Prepared by: National Training Department
Sony Service Company
A Division of Sony Electronics Inc.

Course presented by_____

Date_____

Student Name _____

Sony Service Company
A Division of Sony Electronics Inc
Printed in U.S.A.

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Features

Overview

The models covered by this manual are the new KP53XBR200 and the KP61XBR200. These two models are electrically identical. The differences have to do with screen size. Therefore they use different cabinets, screens, mirrors and tubes. These sets also have a Self Diagnostic system.

Picture

The two models share the following picture features:

- **Advanced Pro-Optic System** – Sony technology that allows full corner to corner focusing.
- **New Extended Definition CRT** – Allows corner to corner focusing to be increased by 25% over last year's model.
- **MICROFOCUS Lens System**
- **Digital Reality Creation (DRC)** – DRC uses line doubling and pattern recognition algorithms to take the NTSC signal to a near HDTV equivalent. This will be discussed in more detail later.
- **Double Scan Technology**
- **Auto Focus Full Digital Convergence** – Allows the setting of V and H center and skew by the customer. This convergence system can produce a sharper picture and is less susceptible to drift due to aging or shipment.
- **High Performance Video Processor**
- **3D Digital Comb Filter**
- **Brightview Dual Component Screen** – The screen contains a Thin Film Fresnel that brightens and sharpens the picture, and a Fine Pitch Lenticular screen that achieves higher resolution by using black stripes to increase contrast.
- **Built-in High Contrast Screen**
- **First Surface Mirror** – Unlike most mirrors, the reflective surface is on the front of the mirror glass. This improves brightness and contrast, and eliminates ghosting caused by the reflected light passing through the glass.
- **Advanced Velocity Modulation**
- **Advanced High Voltage Regulation** – Eliminates distortion and focus fluctuations that occur when changes in brightness levels cause changes in the high voltage.
- **Noise Reduction**
- **Shading Compensation** – Eliminates color shift and hot spots that can occur due to the angle of the picture tubes to the mirror.
- **Wideband Video Amplifier**
- **Multi Image Driver** – Digital-editing technology that provides versatility in controlling on-screen images. Used in Picture and Picture and Channel Index modes.
- **Twin View Picture-in-Picture** – Allows for viewing two pictures simultaneously and the ability to expand either image up to double its normal size.
- **Free Layout Picture-in-Picture** – Allows the PIP window to be placed anywhere on the screen.
- **XDS (Extended Data Service)** – Receives data information services that some stations may broadcast. This data includes time, station call letters, etc.

Audio

The two models share the following audio features:

- **MTS Stereo with dbx NR**
- **Dolby Pro Logic Surround Sound**
- **Front Left/Right Audio Power - 20Wx2**
- **Center Audio Power – 20W**
- **Surround Audio Power – 15Wx2**
- **Center speaker input for use with a separate Dolby Pro Logic A/V Reciever**

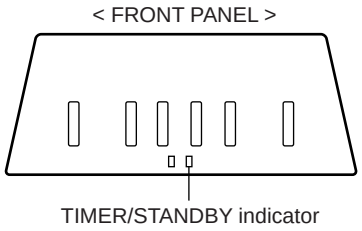
NOTES

Self-Diagnostics

Overview

The RA-4 chassis employs a Self-Diagnostic system that uses the Timer LED and an on screen menu to help indicate where the problem with the set has occurred. You will generally have to use the flashing LEDs since the set will be shut down. AC power must be disconnected in order to turn the set off once shutdown has occurred.

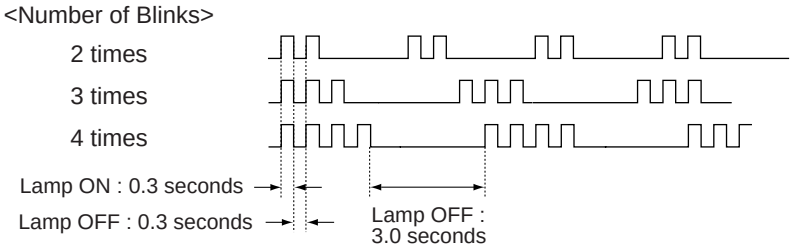
When a failure occurs, all of the circuits covered by the Self-Diagnostics, except AKB, send a signal to the OSD CPU. The OSD CPU sends data to the Main CPU that indicates how many times the Timer LED will flash. The AKB circuit located in the Video Processor IC sends data over the I2C bus directly to the Main CPU. In addition, each circuit, except AKB and High Voltage, send a signal to the latch circuit to shut the set down when failure occurs.



•EXAMPLE

<Diagnosis Items>

- +B overcurrent
- +B overvoltage
- Vertical deflection stop



The number of times the LED blinks may correspond to that shown in the following table:

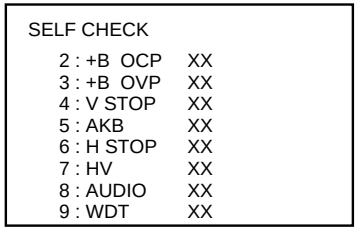
Diagnosis item	Standby/ sleep lamp, Number of blinks	Self-diagnosis screen display, Diagnosis item : Results
• Power not ON	Not lit	
+B OCP detection	LED blinks 2 times	2 : +B OCP XX
+B OVP detection	LED blinks 3 times	3 : +B OVP XX
V detection	LED blinks 4 times	4 : V STOP XX
AKB detection	LED blinks 5 times	5 : AKB XX
H detection	LED blinks 6 times	6 : H STOP XX
HV abnormality detection	LED blinks 7 times	7 : HV XX
Audio abnormality detection	LED blinks 8 times	8 : AUDIO XX

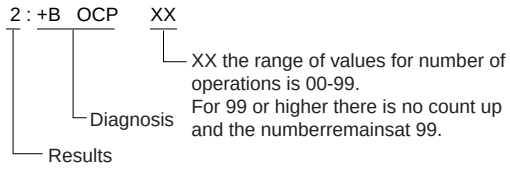
∗ : XX the range of values for number of operations is 00-99. For 99 or higher there is no count up and the number remains at 99.

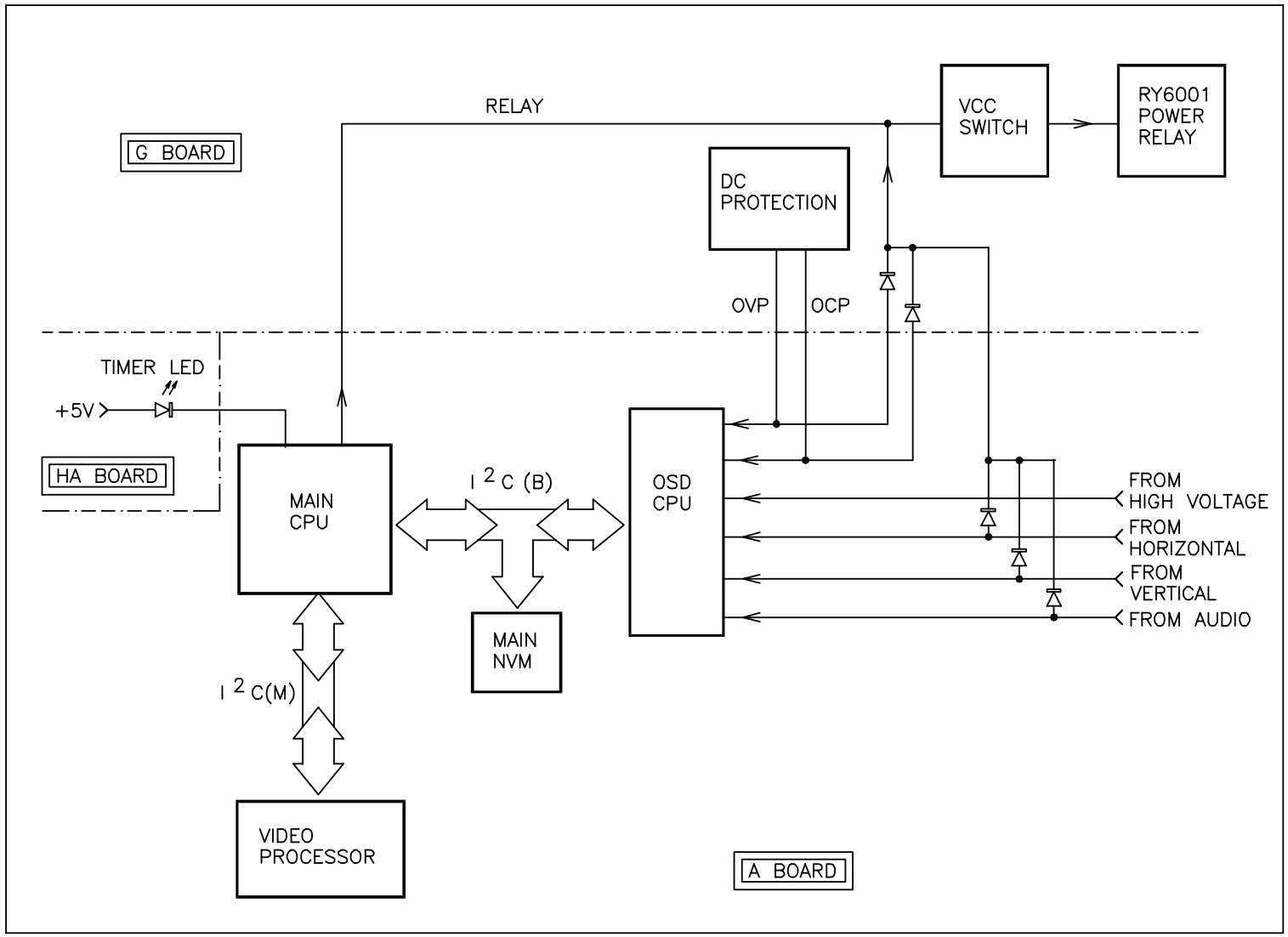
If the problem is intermittent and you can get the set to operate, you can display a menu showing the number of times failures have occurred. This is done by pressing the following sequence of buttons on the remote.

Display Channel 5 Vol - Enter

The display will look as follows.







SELF–DIAGNOSTICS

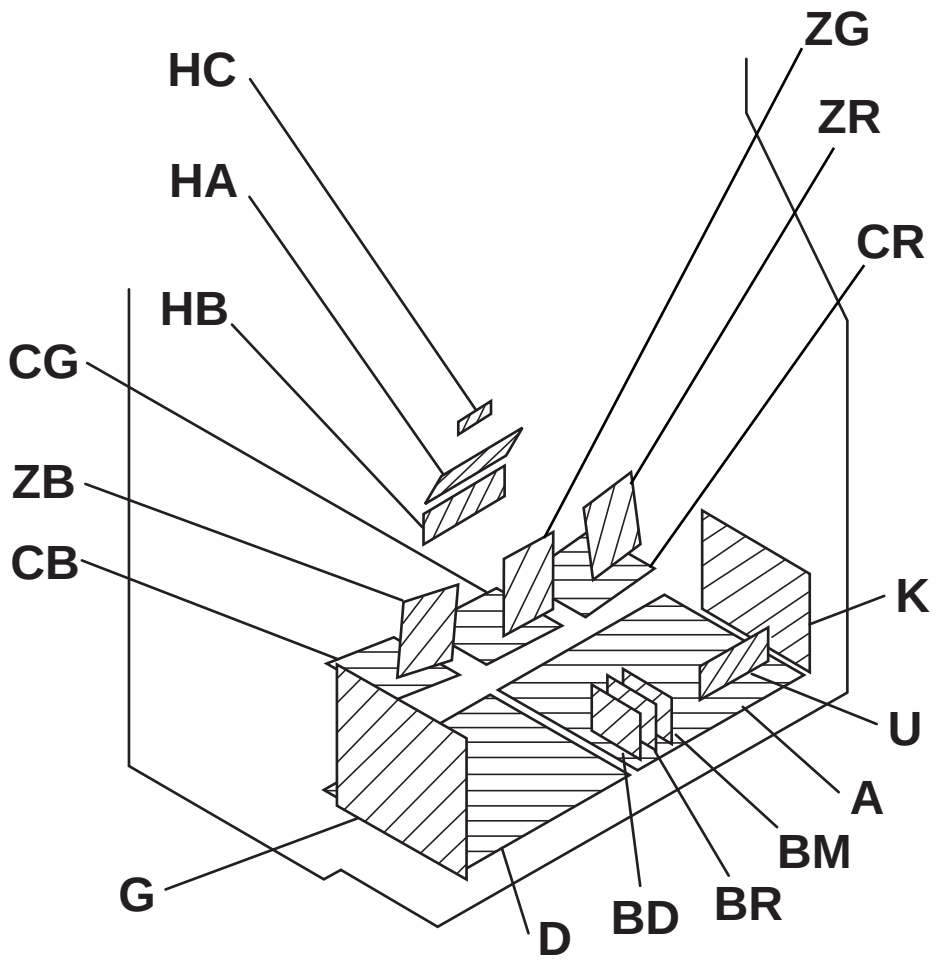
TVP08J80 1043 12 21 98

Board Descriptions

Overview

The models covered by this manual are the new KP53XBR200 and the KP61XBR200. These two models are electrically identical. The differences have to do with screen size. The table below shows which circuits are present on each of the boards. This will help if you are doing board level (SAYS) or component level repair.

Name	Circuits contained
A	Tuners, A/V switching, RGB processing, H Jungle, VDSP, Syscon
BD	Auto registration (Digital Convergence)
BM	MID (Multi Image Driver)
BR	DRC (Digital Reality Creation)
CR,CB,CG	CRT drive and IK feedback.
D	H and V deflection, Sub-deflection, HV, HV Regulation
G	Power supply
HA	Front panel controls, Power and Timer LEDs
HB	Front video inputs, Auto Focus and Setup buttons
HC	Remote sensor
K	Audio Processing and Audio Outputs
U	S Link Input/Output
ZR,ZG,ZB	Hor. and Vert. deflection and sub-deflection coils, VM


ZG
HC
ZR
HA
CR
HB
CG
ZB
CB
K
U
A
BM
G
D
BD
BR

Power Supply Block

AC Input

When the unit is first plugged in, AC power passes through two line filters and is applied to the Standby Power Supply. This is a switching power supply that produces the Vcc source voltage and the standby +5V (RM+5V) for System Control. When the set is turned ON, the AC input is applied through RY6001 Power Relay to the switching B+ rectifier, which supplies power to the Converter circuit. The switching B+ rectifier is monitored at each of its outputs. The negative side of the switching B+ rectifier is monitored to ensure that RY6002 is activated. RY6002 is closed to bypass the In-Rush Current Limiter Resistor when the set is turned ON. When RY6002 is closed, it shunts In-Rush Current Limiter Resistor so that the negative side of the bridge is connected to ground. If the relay is not closed, a voltage will be developed to shut down the set. The positive side of the switching B+ rectifier is monitored to hold the secondary voltages down if the AC voltage should be too low. This is performed by monitoring the switching B+ voltage and applying that voltage to the soft start circuit. This is done because of the excessive current draw when the switching B+ is low.

Power ON

When Power ON is selected using the remote or the front panel switch, a signal is sent from IC1008 Main-CPU to the Vcc switch section on the G board. The Vcc circuit sends voltage from the Standby supply to the Oscillator and Soft Start circuits. When this voltage reaches IC6003 Oscillator, it begins oscillating. The Soft Start circuit is activated at the same time. This circuit keeps the oscillator at a certain frequency (175KHz) for a specified period of time. This keeps the initial start up voltage low and prevents excessive back EMF from destroying the converter transistors. When regulation begins, the normal operating frequency is around 73KHz.

Converter

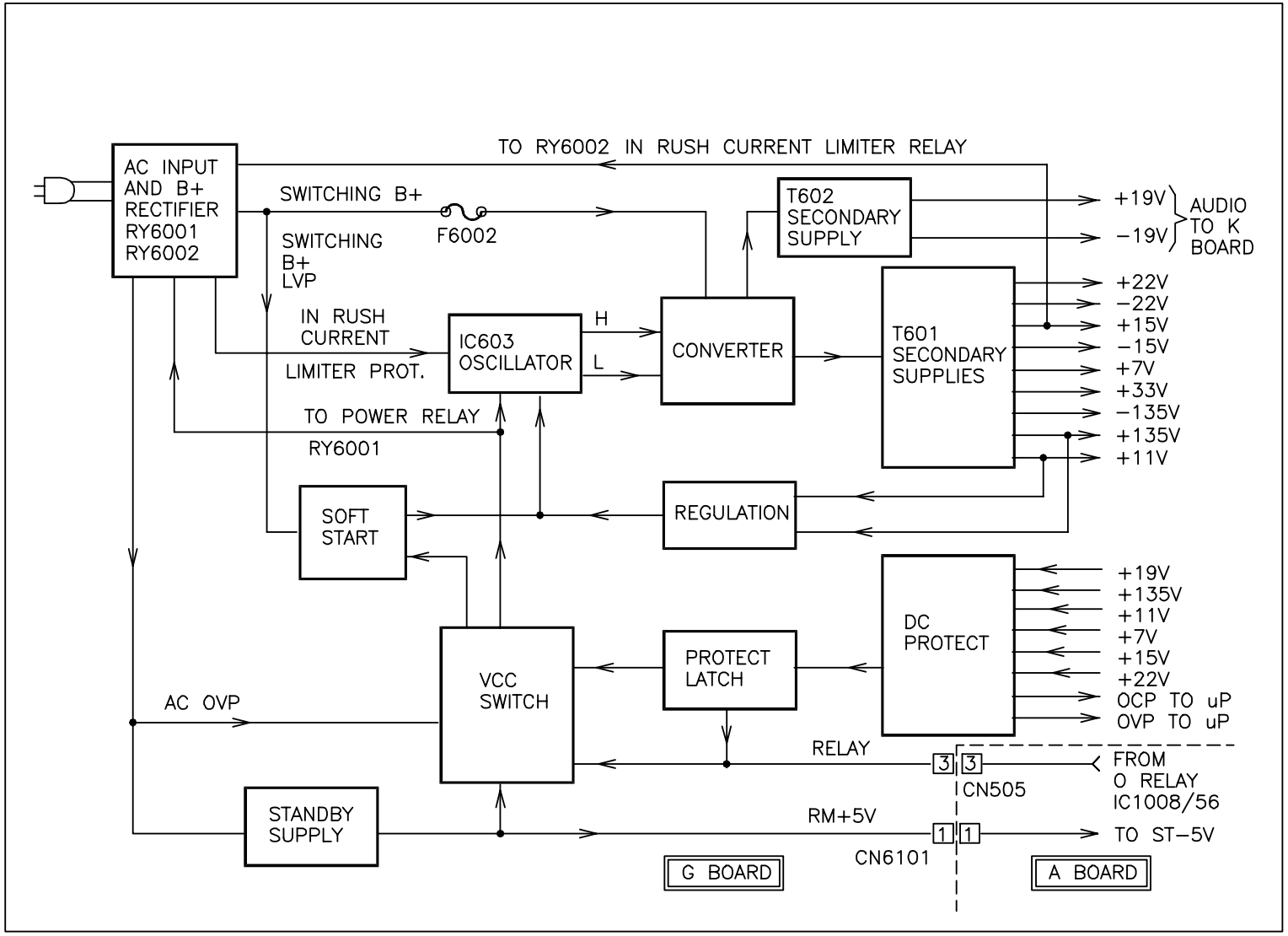
When the Oscillator circuit begins oscillating, it outputs two signals that are 180 degrees out of phase. These signals are applied to the converter circuit. The converter circuit contains two Driver ICs that drive two push pull transistor circuits. These circuits drive two transformers that create the AC voltages, which are rectified by the two secondary supply circuits to power the rest of the set.

Regulation

Once the secondary supplies begin to generate DC voltages we can begin to regulate their output. This is done using the +11 volt and +135 volt lines. The +11 volt line is used to power the regulation circuit while the +135 volt line is monitored to regulate the supplies. The +135 volt line is sent to the regulation circuit to produce an error voltage that is fed back to the oscillator circuit. This voltage controls the pulse width and frequency of the oscillator. Changes in the frequency cause changes in efficiency of the transformers, which in turn cause the voltage to become lower or higher.

Protection

In addition to the three protection circuits on the AC side of the supply, there are additional circuits on the DC side. The +135V line is checked for OVP and OCP. If one of these conditions occurs, a voltage is sent to the protect latch to turn it ON. The latch shuts down the set by turning OFF the Vcc switch. A voltage is also sent to the System Control circuit for the self-diagnostic system. In addition, the 11V line is compared to the +19, +22 and +7 volt lines. If these voltages fall below a specified level, the protect latch will be activated and the set will shut down. There is no indication in the self-diagnostic menu that this circuit has been activated.



POWER SUPPLY BLOCK

TVP08J1 962 12 15 98

AC Input and Switching B+

Overview

The AC Input and Switching B+ circuit is used to filter the AC line voltage and generate the DC voltage necessaary to run the switching supply.

AC Input

AC enters the G board at CN6004 when the unit is plugged in. It then passes through F6001 and L6001 and L6002 Line Filters. L6002/3 is the High side of the AC line and splits off to two places. It is used to power the Standby +5V supply and is connected to one of the contacts of RY6001 Power Relay.

There are a few protection components in place in addition to F6001 Fuse. There are two spark gaps across the AC line at CN6004 AC Input. There is also one across the AC line after F6001 Fuse. Two capacitors, C6001 and C6002, are present on either side of L6001 Line Filter. VD6001 is a VDR across the L6002/1 and 3 for spike protection.

Troubleshooting

Problems in this area are usually the result of line spikes or lightning. If you have a dead set and suspect lightning damage, you should remove the G board by removing one screw and pulling it out. A quick visual check can be performed by looking on both sides of the board for burnt traces or components. If F6001 is open, be sure to check for any burnt components. If everything looks OK, then check the voltage across VD6001. If the line voltage is not present there, continue to work your way back checking across the AC line until you find an open component.

B+ Rectifier

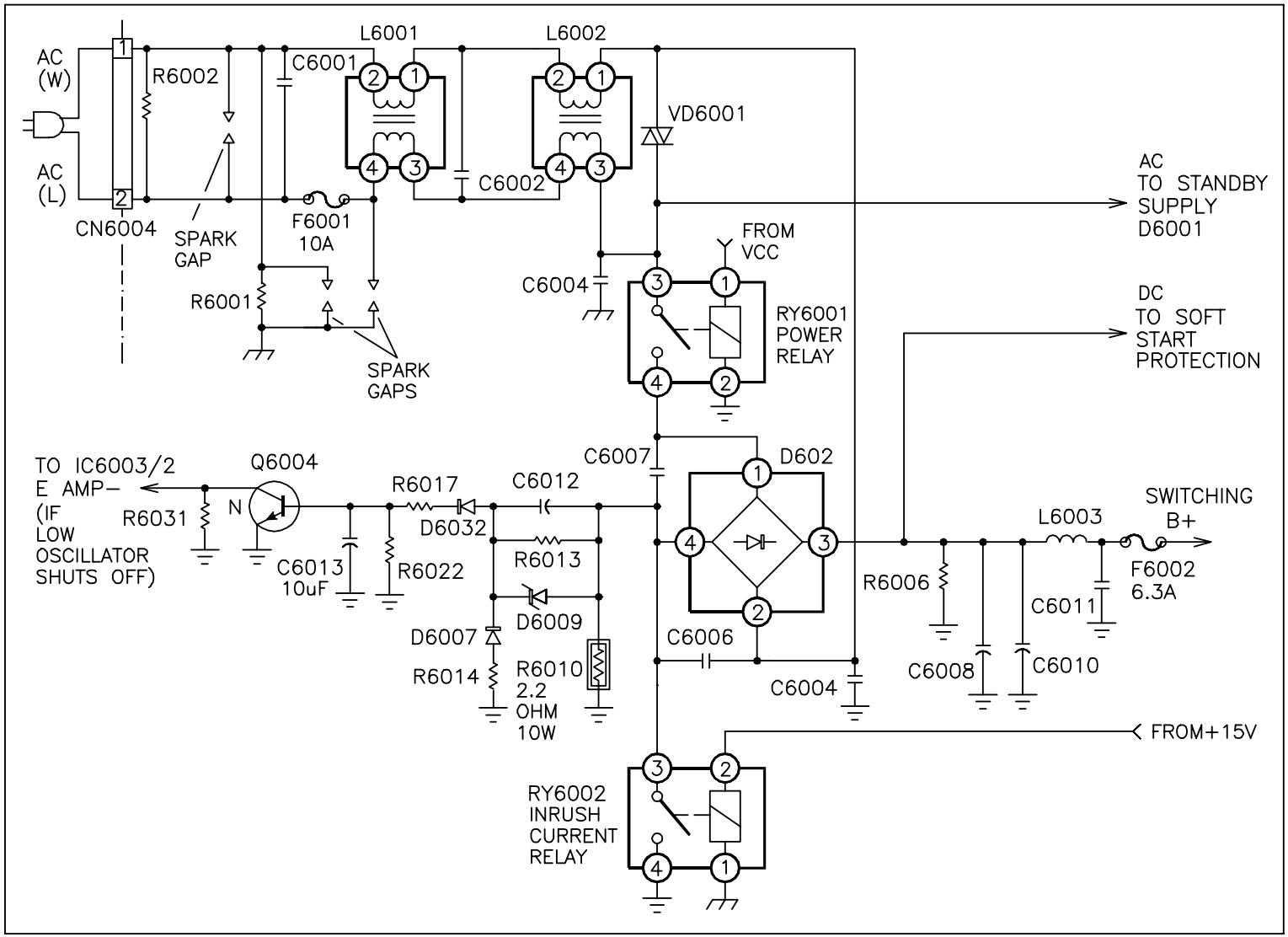
When power is turned ON, the AC line voltage is applied across D602 Bridge Rectifier because RY6001 Power Relay is closed. D602/3 + outputs 130 volts which is filtered by C6008, C6010 and L6003. This voltage is used as the B+ for the switching power supply converter circuit and is fused by F6002. D602/4 is connected to ground through R6010 In-Rush Current Limiter at initial power ON. When the secondary supplies begin to run, RY6002 will be closed which connects D602/4 - to Hot ground.

Switching B+ Low Voltage Protect

Both outputs of the D602 Bridge Rectifier are monitored to cause shutdown of the set. D602/3 + has a sample voltage sent to the Soft Start circuit to monitor for under voltage. If the voltage at this point is too low, the Soft Start circuit will raise the frequency of the switching supply, thereby lowering the secondary output voltages and disabling regulation. The lowering of the secondary voltages will also cause RY6002 to open or may shut the set down. Due to the fact that the power supply voltages will be lowered, the set will indicate an AKB shutdown by flashing the Timer LED five times, pausing, and then repeating. This action will be discussed in greater detail in the Soft Start section.

In-Rush Current Limiter Protect

D602/4 is monitored to ensure that the R6010 In-Rush Current Limiter has been switched out of the circuit by RY6002. If it has not, a voltage will be developed across it that is rectified and sent to the base of Q6004 AC Protect. If Q6004 AC Protect is turned on, IC6003 Oscillator will be shut down. This will cause no output from the switching supply. Keep in mind that there will be 150 volts present at F6002 since the power relay is still turned ON. In addition, the Timer LED will flash twice, pause and repeat. You will not be able to shut the set OFF using the remote or the front panel switch. The set will have to be unplugged to attempt to re-start the set.



AC INPUT & SWITCHING B+

TVP08J2 963 12 15 98

Standby Power Supply

Overview

The Standby Power Supply is used to develop the voltages that are required by the set in order for it to turn ON. One of these voltages is used to supply power to the System Control ICs. This voltage is a regulated 5 volts and is called RM+5. The other voltage is used as the source voltage for Vcc, which is the low voltage supply for the switching power supply. The AC input to the standby supply is monitored for overvoltage. It will shut the Vcc switch OFF if there is a problem.

Standby Switching Supply

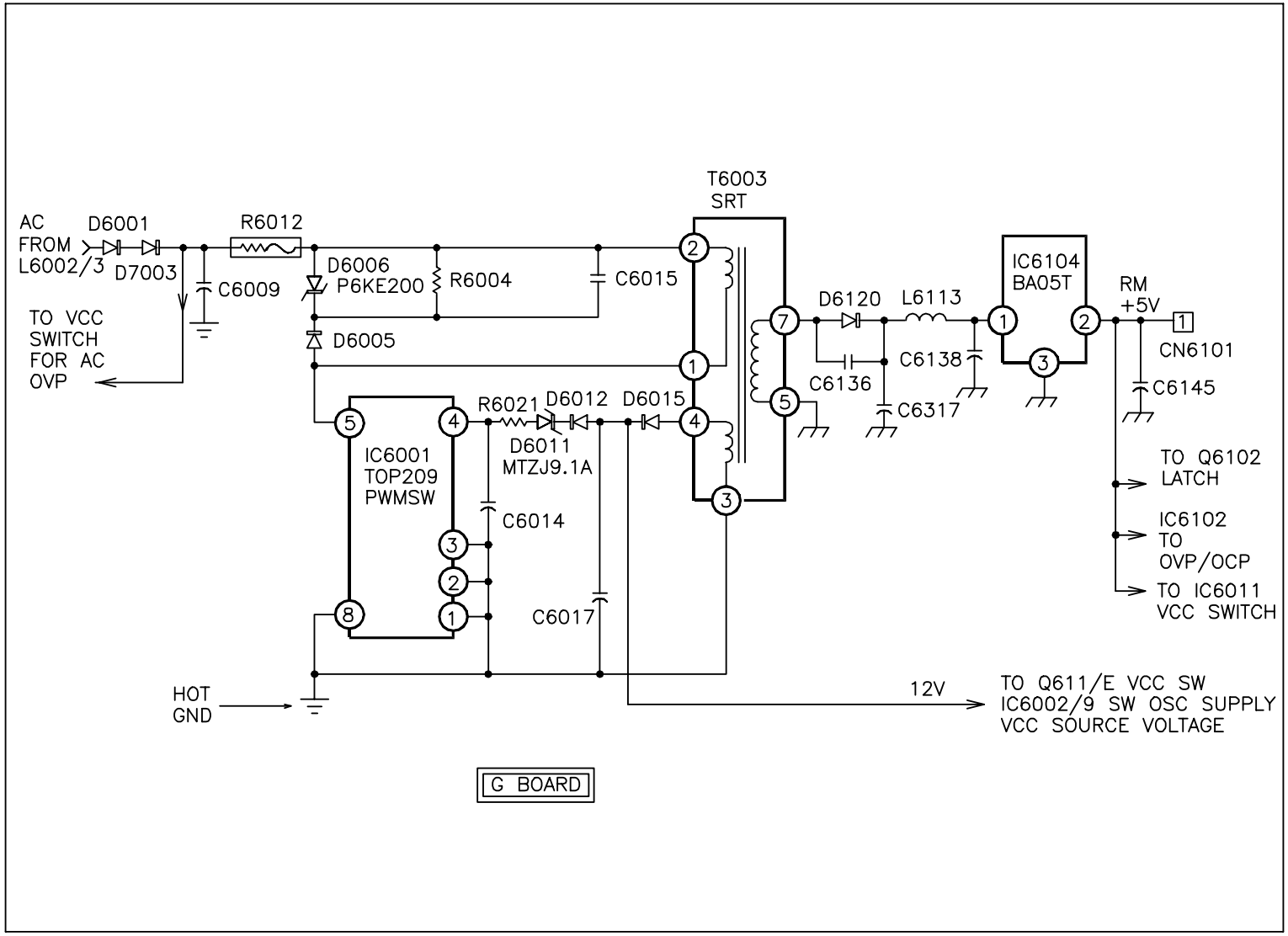
The line AC from L6002/3 is rectified by D6001 and D6003 and filtered by C6009. This voltage is monitored for overvoltage via D6035 and is used to power the standby supply. This voltage then passes through fusible resistor R6012, then to T603 SRT. IC6001 is connected to T6003/1 and begins switching when the voltage arrives. IC6001 PWMSW is a self-starting N-channel MOSFET switching device with a self contained oscillator and error loop amplifier used for regulation.

RM+5

As IC6001 PWMSW voltages are induced in the secondary windings of T6003 SRT, one of these voltages is used to develop the RM+5 line. The signal from T6003/7 is rectified by D6120 and filtered by C6137, C6138 and L6113. This voltage is input to IC6104/1. IC6104 5-Volt Regulator outputs 5 volts from pin 2. This is the RM+5 line on the G board. It is called ST-5V on the A board.

Regulation

The secondary winding at pins 3 and 4 of T6003 SRT develops a voltage that is rectified by D6015. This voltage is used for two purposes. It is the source voltage for the Vcc switch and the feedback voltage for regulation. This voltage passes through D6012, D6011 and R6021, and is input to IC6001/4. Pin 4 is the regulation input for IC6001 PWMSW.



STANDBY SUPPLY

TVP08J3 964 12 17 98

Vcc Switch (Power On)

Overview

When Power On is selected, IC1008 Main CPU sends a signal to the G board to turn ON the Vcc switch. The Vcc voltage powers the Soft Start, Oscillator and Driver circuits. There is a connection from the latch circuit to shut OFF the set if there is a problem on the DC side of the power supply. In addition, there is a connection from the Standby Source Voltage that will shut down the supply if the AC line voltage becomes to high.

Power ON

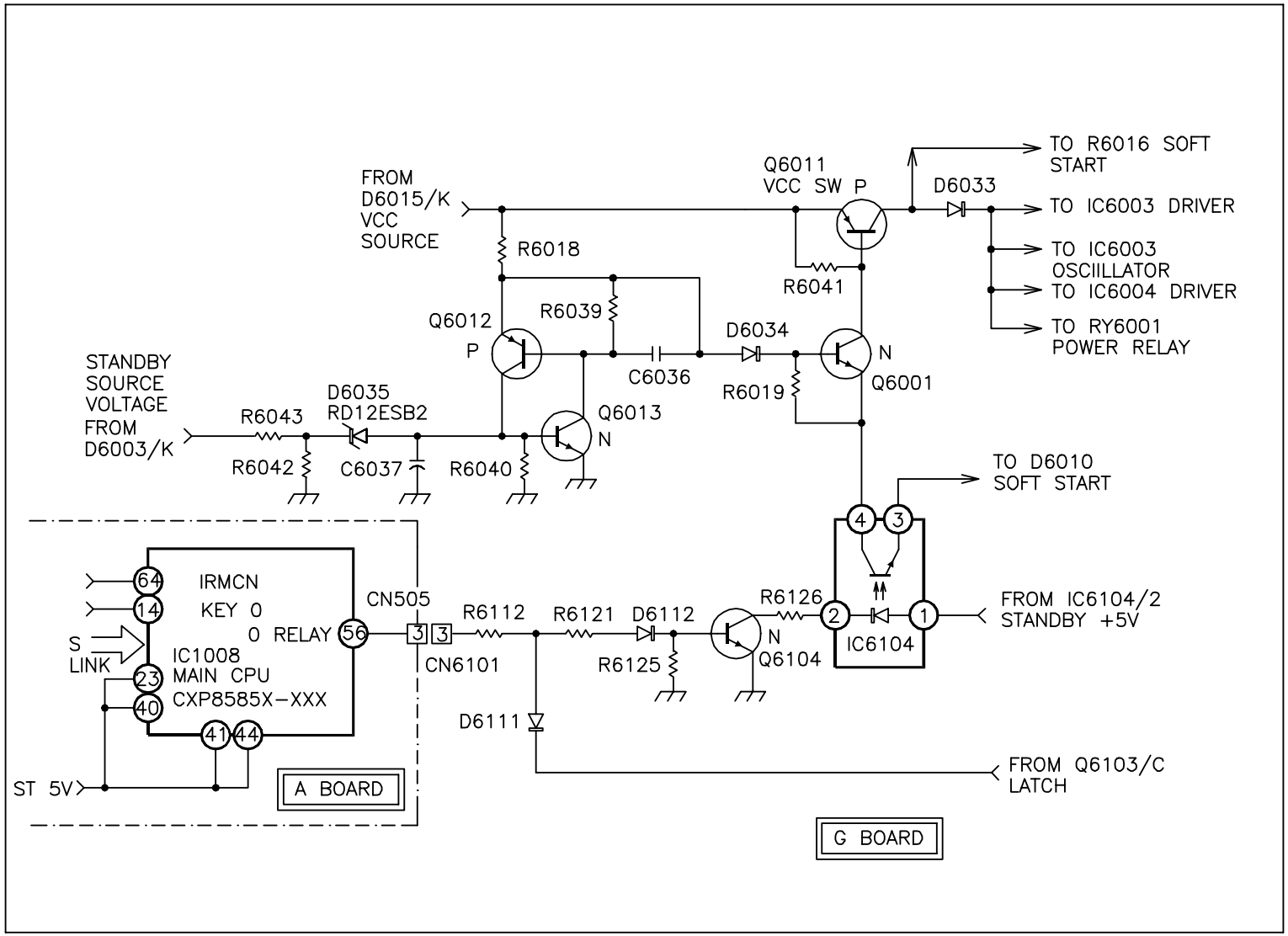
When Power ON is selected using either the remote or the front panel switch, 5 volts is output from IC1008/56 O Relay. This voltage travels from CN505/3 on the A board to CN6101/3 on the G board. It then goes through R6112, R6121 and D6112, placing .6V at Q6104/B. This turns Q6104 ON and causes Q6104/C to pull IC6104/2 to ground. This turns the phototransistor inside IC6104 Vcc Switch ON. When this occurs, current flows through the B-E junction of Q6001. When Q6001 turns ON, it causes Q6011 VccSW to turn ON. This switches the Standby voltage through Q6011 VccSW where it is called Vcc. Vcc turns RY6001 Power Relay ON, as well as powering the Soft Start, Oscillator and Driver circuits.

DC Protect

The DC protection latch circuit is connected through D6111 to the power ON line at the junction of R6112 and R6121. When the protection latch is activated, it pulls the O Relay line LOW and turns power OFF by turning and holding Q6014 OFF.

AC Protect

The Standby Source voltage is monitored in case there is an overvoltage problem on that line. If the voltage from the Standby Source voltage goes too high, it will cause the voltage at the cathode of D6035 to rise above 12.6 volts. The voltage at Q6013/B will be enough to turn it ON. When this occurs, Q6013 conducts, causing Q6012 to conduct. This action causes the Q6001 to turn OFF, thereby shutting down the set.



VCC SWITCH

TVP08J4 965 12 15 98

Soft Start

Overview

A Soft Start circuit is necessary to keep the oscillator that drives the switching circuit above the normal operating frequency of the tuned circuit that is in the switching supply circuit. If this frequency is not above the normal operating frequency at start up, the voltage at the secondary could become too high and cause damage to the set. The soft start circuit causes the oscillator to start at a frequency high above the normal operating frequency by holding the regulating voltage down at initial turn ON of the set. This circuit is also activated if the Switching B+ voltage falls below a certain level.

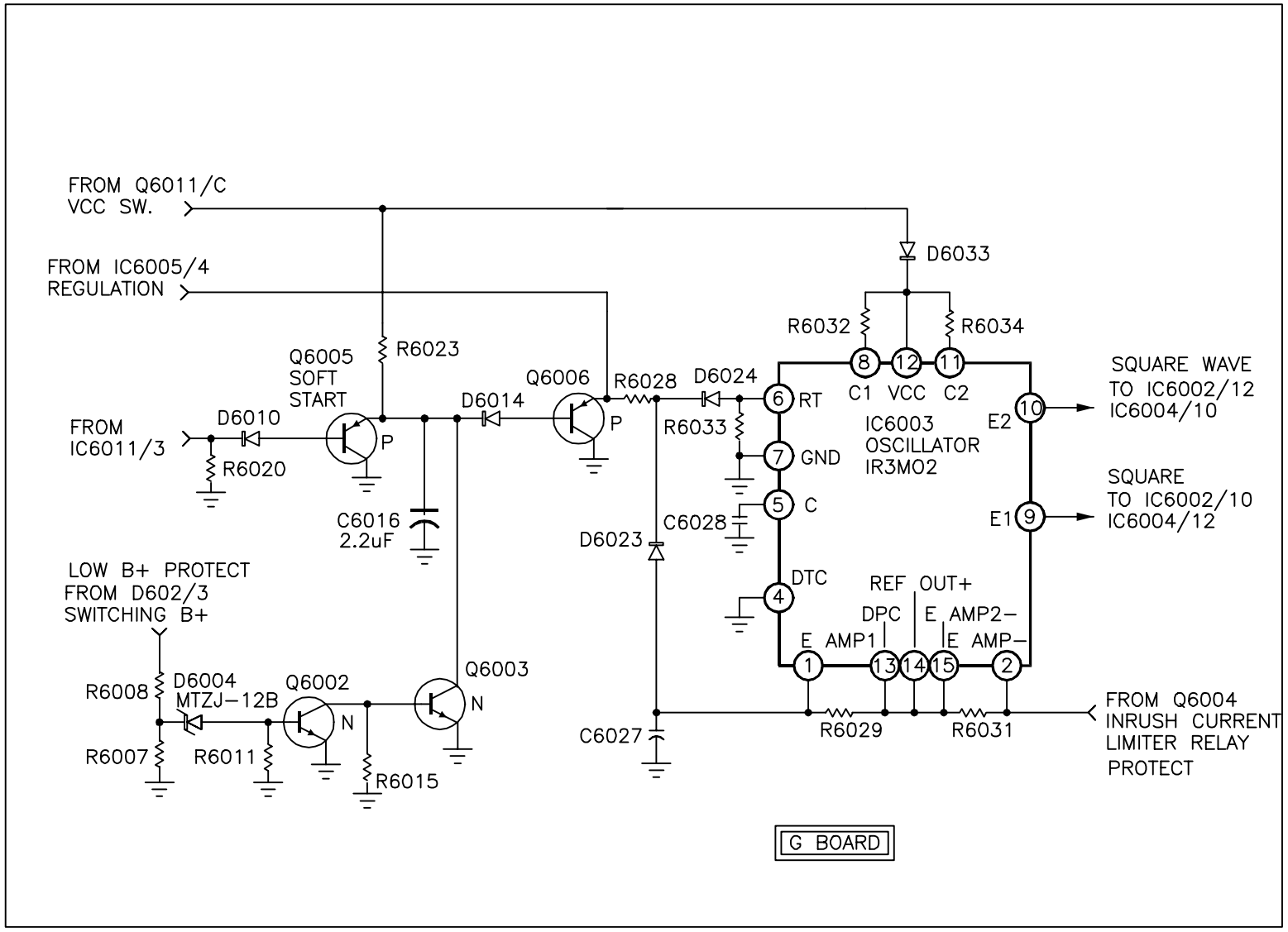
Soft Start – Power ON

When Power ON is selected, the Vcc switch supplies voltage to IC6003 Oscillator. This oscillator is connected to the regulation line that begins to develop voltage. This voltage is held LOW at Q6006/E while C6016 is charging. Once C6016 is charged, the regulation line is controlled by IC6005/4.

Q6005 provides a discharge path for C6016 when the set is turned OFF. This is important because if C6016 is not completely discharged, the oscillator may output the normal operating frequency during Power ON. The discharge path would be through Q6005/C-E junction. Q6005 is OFF during the set's operation because of the voltage applied to it from IC6011/3. Be careful when measuring voltages at Q6005/B as this circuit is easily loaded by a meter or a scope. It is best measured using a scope and a 10X probe.

Soft Start - LVP

The soft start circuit can also be activated if the voltage from D602/3 Switching B+ goes too low. When the voltage across R6007 drops below 12.6 volts, it will cause Q6002 to turn OFF. This causes Q6003 to turn ON. When Q6003 is ON, the cathode of D6014 will be held at ground potential. This is the same condition that occurs at turn ON, therefore the oscillator will oscillate at a high frequency and this will reduce the output voltages from the secondary supplies. If this occurs while the set is operating, it will shutdown. The set will act as if there was an AKB failure, the Timer LED will flash five times, pause and then repeat.



SOFT START

TVP08J5 979 12 17 98

Converter

Overview

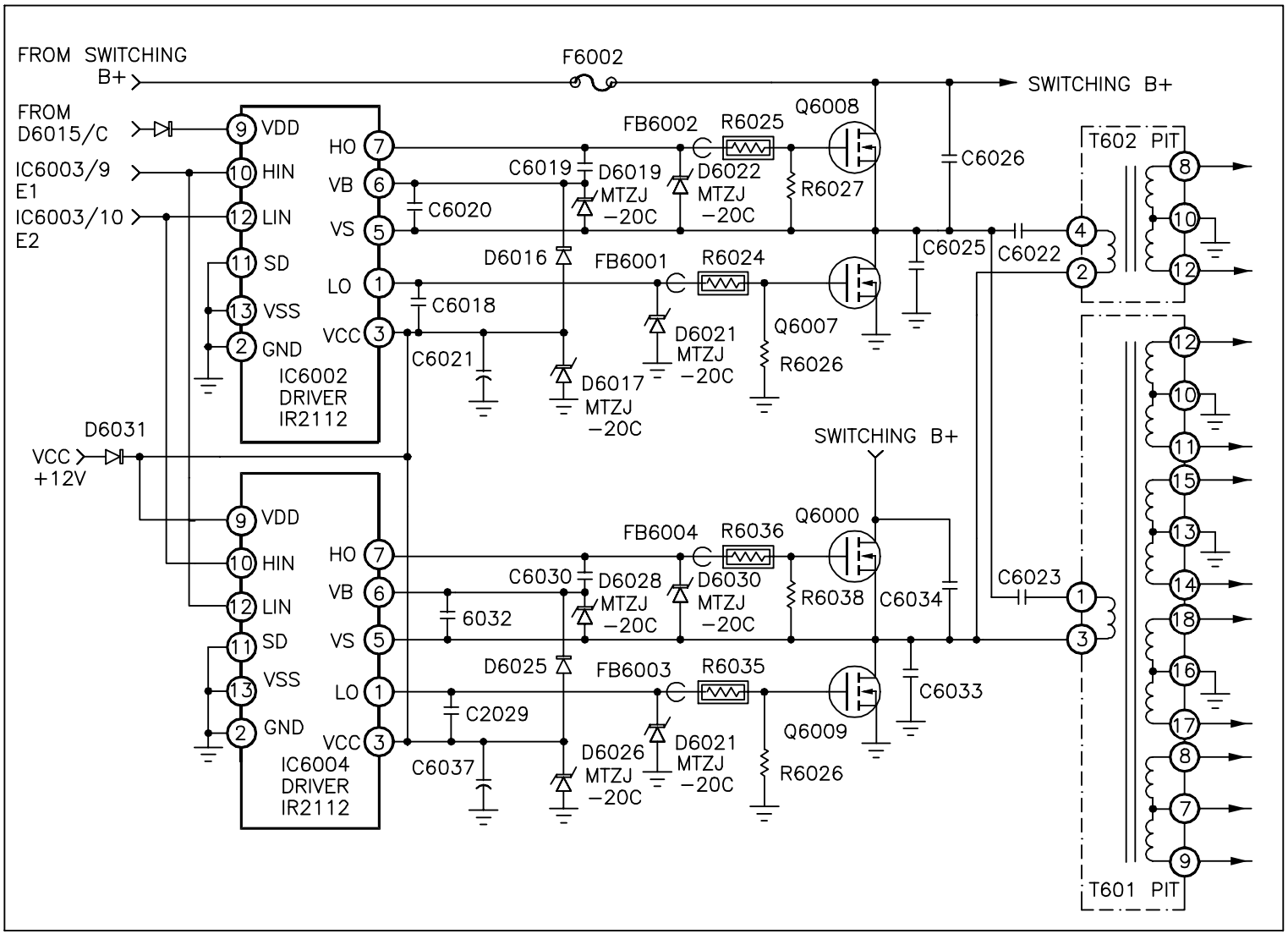
Simply put, the converter circuit switches the DC Switching Supply B+ ON and OFF to create an AC signal. The converter in this set consists of two Driver ICs that drive two sets of N-channel MOSFET transistors. The drivers use the output signal from the oscillator to switch the transistors. These transistors are switched 180 degrees out of phase and are parallel with the two Power Input Transformers.

Operation

Two signals 180 degrees out of phase are applied to the Hi and Lo side inputs. The Hi side input of IC6002/10 is the same phase as the Lo side input at IC6004/12. The Low side input at IC6002/12 is the same phase as the Hi side input at IC6004/10. These signals are amplified and output in phase with their inputs.

The Hi side of each of these drivers has a floating power supply that boosts the output level of the signal. The input to this supply is at IC6002/6 and IC6004/6. The return is at pin 5 of IC6002 and IC6004. This floating supply allows a 130 Vpp signal to be output for each Hi side driver.

If IC6002/7 is outputting a High signal, then Q6008 turns ON. When Q6008 is ON, it allows the 130-volt Switching B+ to be present at Q6008/S. This voltage is applied to IC6002/6, the floating supply input, and also to C6022 and C6023. The signal seeks ground through Q6009, which is always ON when Q6008 is ON. Current flows through the transformers T602 and T601 while C6022 and C6023 are charging. At the same time, the signal outside of IC6002/1 Lo side output is Low. When the signal at Q6008/G goes Low, the signal at Q6007/G goes High. This causes C6022 and C6023 to be connected to ground. At the same time, Q6010 is turned ON and Q6009 is turned OFF. This causes current to flow through the transformers T601 and T602 and capacitors C6022 and C6023. This cycle continues while the set is running and causes sine waves to be seen at T601/1 and T602/4. This signal is induced into the secondary of the transformers to produce the power supply output.



CONVERTER

TVP08J6 981 12 17 98

T602 Secondary (Audio B+)

Overview

The secondary winding of T602 PIT is used to develop two voltages - +/- 19 volts. These voltages are used to power the K board, which contains all of the audio circuits.

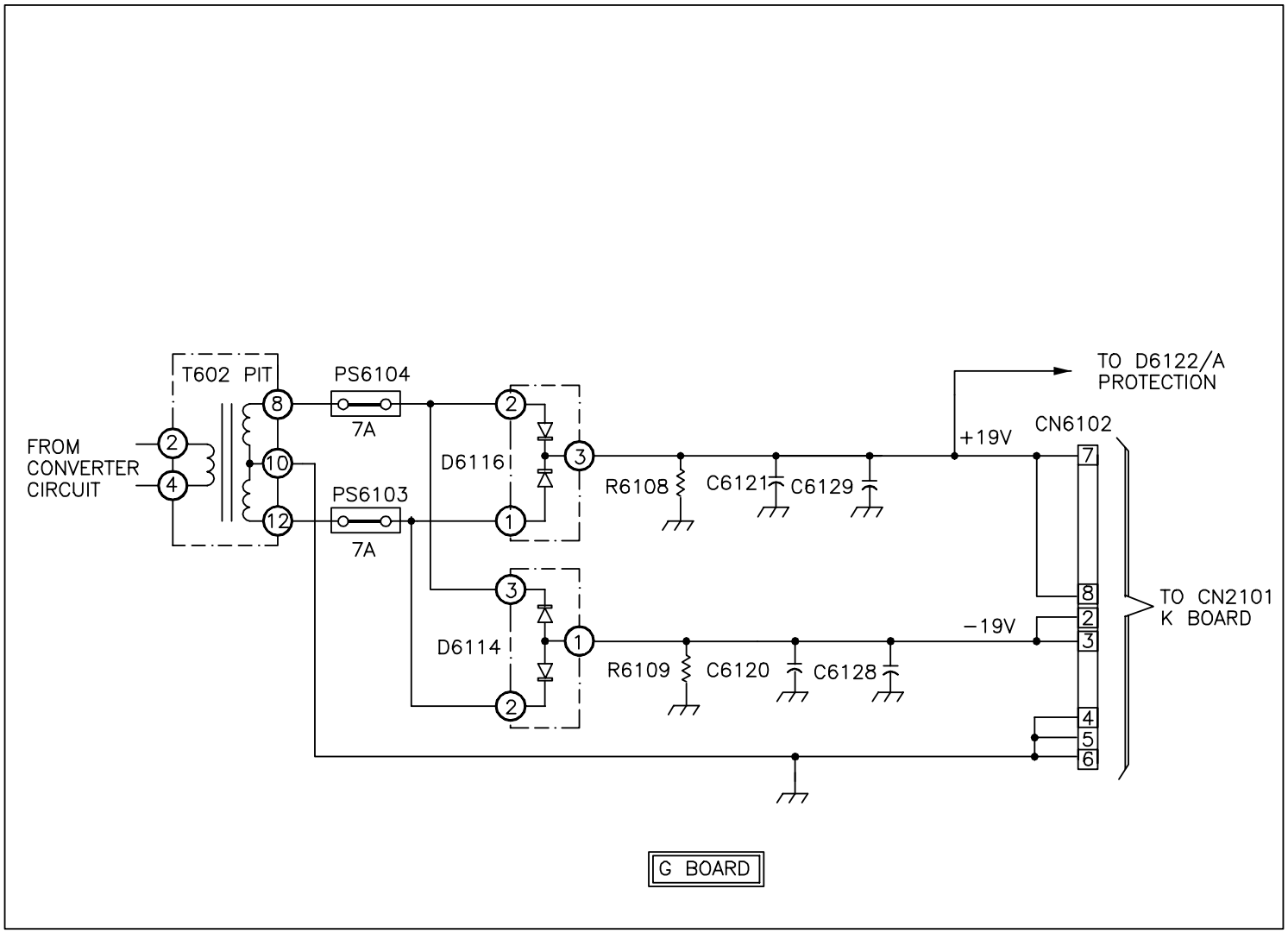
Operation

The voltage induced into the secondary winding of T602 is used to develop +/- 19 volts. This voltage is used to supply the Audio section (K board) and is fused with PS6103 and PS6104.

This voltage is rectified by D6116 and filtered by C6121 and C6129 to create the +19 volt supply. It is also rectified by D6114 and filtered by C6120 and C6128 to create the –19 volts. The +19 volt supply is output at CN6102/7 and 8. It also goes to D6122/A, which is part of the protection circuitry. The –19 volt supply is output at CN6102/2 and 3.

Troubleshooting

If the rest of the power supply is working, but there is a problem with these supplies, you should suspect a problem on the K board. The set can be run with CN6102 unplugged. If the correct voltages are measured at CN6102, then the problem is on the K board. If PS6104 and PS6103 are open, it would be a good idea to power the unit without CN6102 disconnected. If everything appears to be OK, check the K board for shorts on the +/- 19 volt lines. If none are found, then plug CN6102 in and power up the unit.



T602 SECONDARY (AUDIO B+)

tvp08j7a 983 12 15 98

T601 Secondary-1

Overview

There are four secondary windings on T601 PIT. The voltages induced in these windings are used to power everything in the set, except for the audio section. The voltages developed here are +/- 15 volts, +/- 22 volts, +11 volts, +7 volts, +/- 135 volts and +33 volts.

+/- 15 Volts

The voltage from the winding of T601/11 and 12 is applied across D6105 Bridge Rectifier. C6119, C6132 and L6108 filter the positive output of D6105/3. This output is used for three things. First, it is applied to Q6106/E, which turns Q6106 ON and allows current to flow through its E-C junction. It passes through R6141 to RY6002 In Rush Current Limiter Relay. It turns the relay ON when the voltage is sufficient. If the voltage does not rise to a sufficient level or there is a problem with Q6106, the set will shut down. Next it is sent to D6126/A, which is part of the protection circuitry. Lastly it is sent to CN6105/3, CN6106/5 and CN6104/2 where it is sent to the D and A boards.

The negative output from D6105/3 goes through R6122, R6123 and R6124, which are parallel. C6118, C6131 and L6109 then filter this voltage. It is then output from CN6105/4 and CN6106/6, both of which go to the D board.

These lines are used to produce other voltages on the D board. These voltages are +/- 12 volts and +/- 5 volts.

+ 11 Volts

The voltage from the winding of T601/11 and 12 is applied across D6102 through L6103 and L6104. C6122, C6133 and L6110 filter the rectified voltage. This voltage is used on the G board by the regulation and protection circuits and it exits the G board at CN6104/11 to the A board.

The +11 volt supply is used on the A board to produce the +9 volt supply.

+/- 22 Volts

The voltage from the winding of T601/14 and 15 is applied across D6108 through PS6105 and PS6106. C6125, C6135 and L6112 filter the rectified voltage. The voltage is used on the G board by the protection circuit and it exits the G board at CN6105/1.

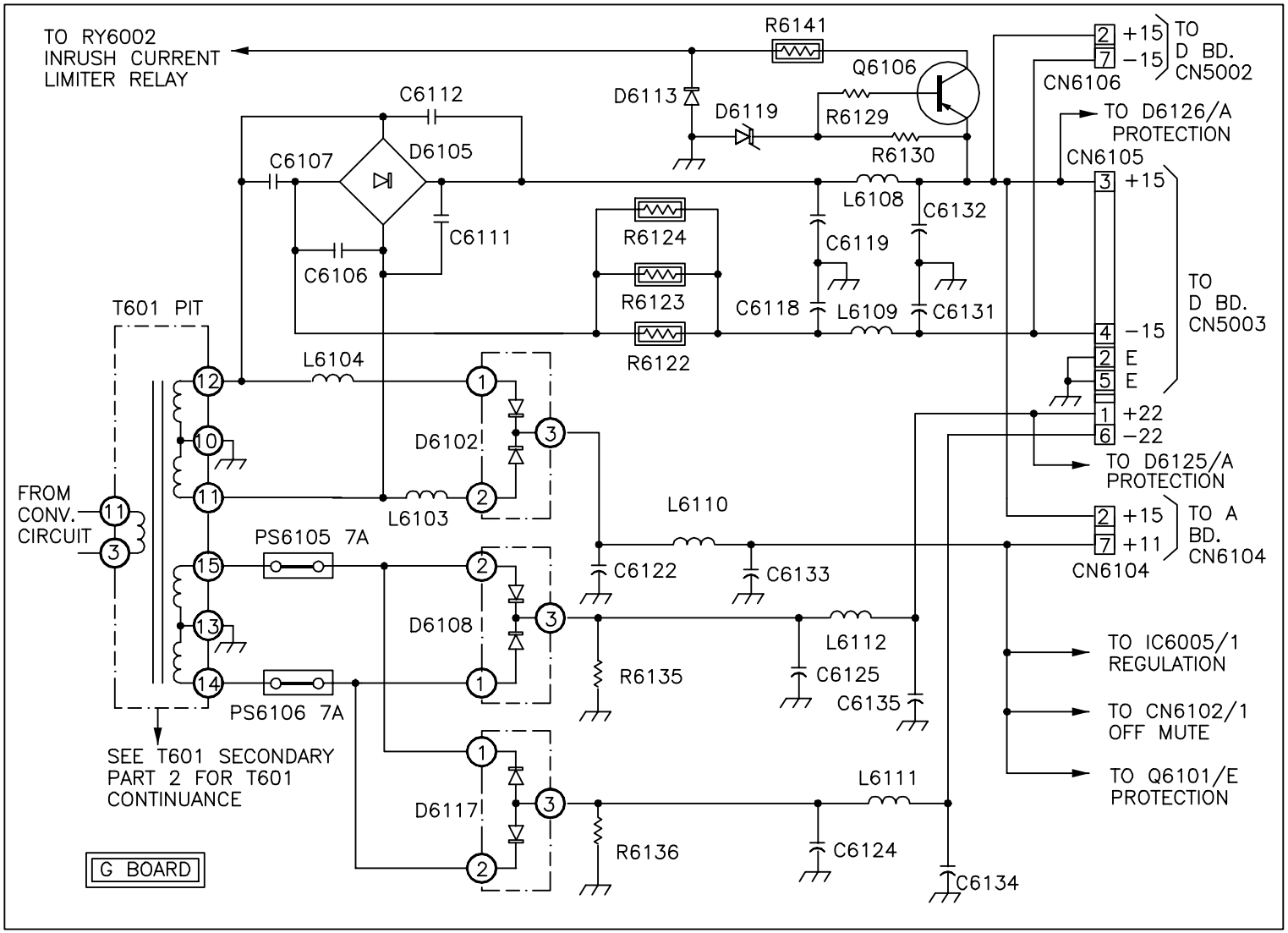
The winding of T601/14 and 15 is applied across D6117 through PS6105 and PS6106. C6124, C6134 and L6111 filter the rectified voltage which leaves the G board at CN6105/6.

The +/- 22volt lines are used to power only the Convergence amplifiers on the D board.

Distribution

The table below shows the circuits powered by the voltages previously discussed:

Supply	Circuits
+15	Vertical Out IC5004, 12 Volt regulator IC5002 (D board), IC502 12 Volt regulator (A board)
-15	Vertical Out IC5004, -12 Volt regulator IC5001
+12(D)	V, H, B+, HV, and IK protection circuits, Shading, HV control, PWM, H Saw, Auto Registration sense and switching, 5 Volt regulator IC8004
+12V(A)	H Jungle IC507, VM and IK buffers
-12	Shading, HV control, H Saw, H pulse shaper,-5 Volt regulator IC8003
+5	BD board (Auto Registration)
-5	BD board (Auto Registration)
+11	Off Mute Q547, 9 Volt regulator IC505
+9	TU501, TU502 Video Processing, AVU switch
+22	Convergence Amplifiers IC5005 and IC5006
-22	Convergence Amplifiers IC5005 and IC5006



T601 SECONDARY (PART 1)

TVP08J8 982 12 21 98

T601 Secondary-2

+7 Volts

The voltage from the winding of T601/17 and 18 is applied across D6109 through PS6101 and PS6102. C6117, C6126 and L6107 filter the rectified voltage. The voltage is used on the G board by the protection circuit and exits the G board at CN6104/4 and 5.

The +7 volt supply is used to produce three other voltages on the A board. They are Def +5 volts, +5 volts and +3.3 volts.

+135 Volts

The voltage from the winding of T601/8 and 9 is applied across D6104 and D6107. C6114, C6123 and L6106 filter the rectified voltage. The voltage is used on the G board by the protection and regulation circuits and is also used to produce the +33 volt line. It exits the G board at CN6106/1.

The center tap of the secondary located at T601/7 is connected through R6118. As the load draws more current, the voltage across R6118 falls closer to being negative. The OCP circuit monitors this voltage.

-135 Volts

The voltage from the winding of T601/8 and 9 is applied across D6103 and D6106. C6113, C6127 and L6105 filter the rectified voltage. It exits the G board at CN6106/3.

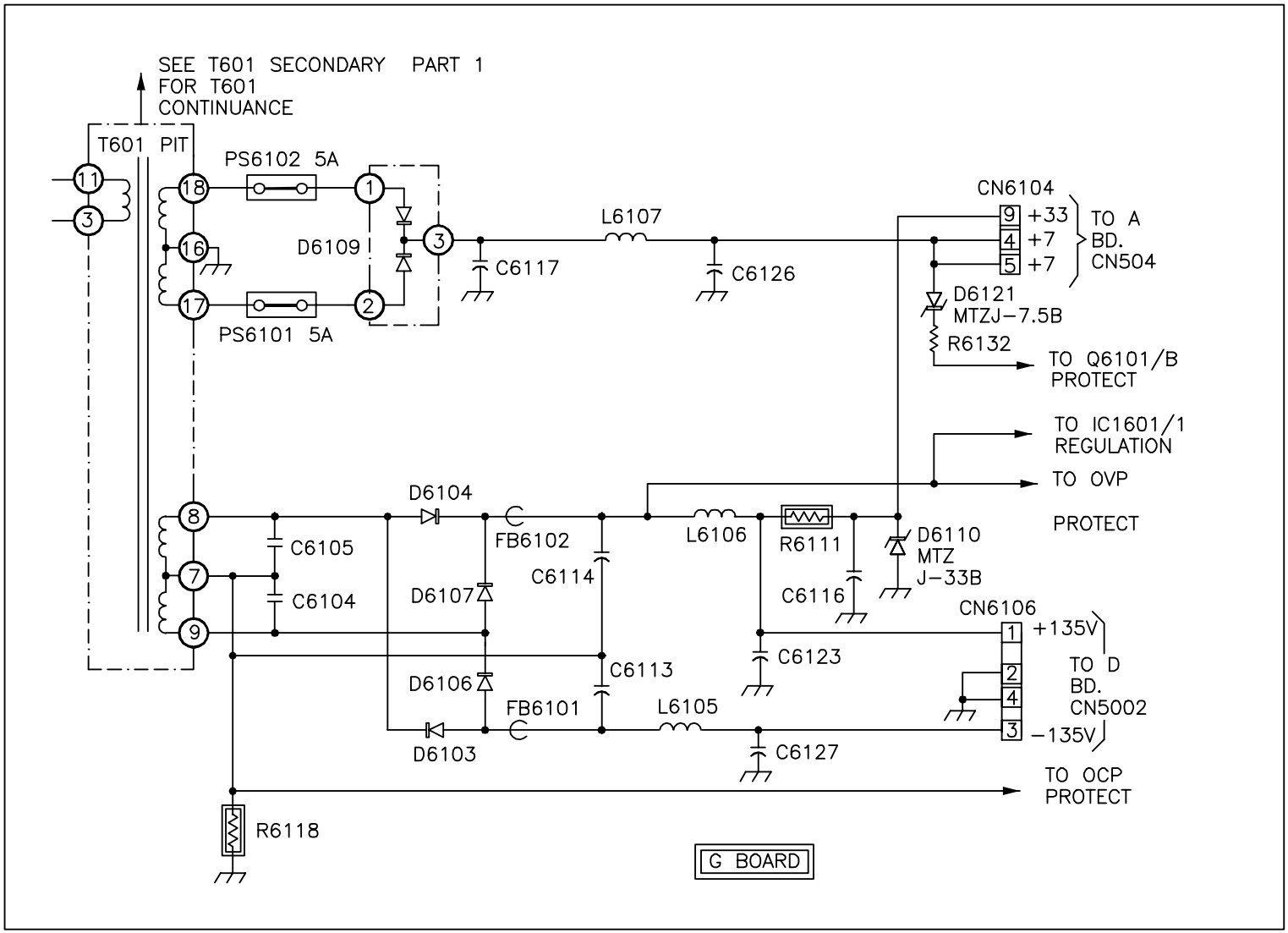
+33 Volts

The +135 volt line goes through R6111 Current Limiting resistor. On the other side of R6111 is D6110 Zener Diode and C6116. The zener is used to drop the +135 volts down to 33 volts. The voltage exits the G board at CN6104/9.

Distribution

The table below shows the circuits that are powered by the voltages previously discussed:

Name	Circuits
+7	Def +5V regulator IC503, +5V regulator, 3.3V regulator
Def +5	VDSP IC512, H BLK Delay IC517, ½ H + Odd/Even IC508, Vout Reference IC5004, BD board
+5	TU501, TU502, Sync Switch IC509, IC1304 Frame Memory IC1304, A/D Converter IC1309, BM board, BD board
+3.3	3D Comb Filter IC1306, BR board, BM board
+135	FBT T8003, LOT T8002, HV Drive, HV out
-135	Pincushion, Horizontal, HV Regulation
+33	TU501, TU502



T601 SECONDARY (PART 2)

TVP08J9A 1027 12 16 98

Regulation

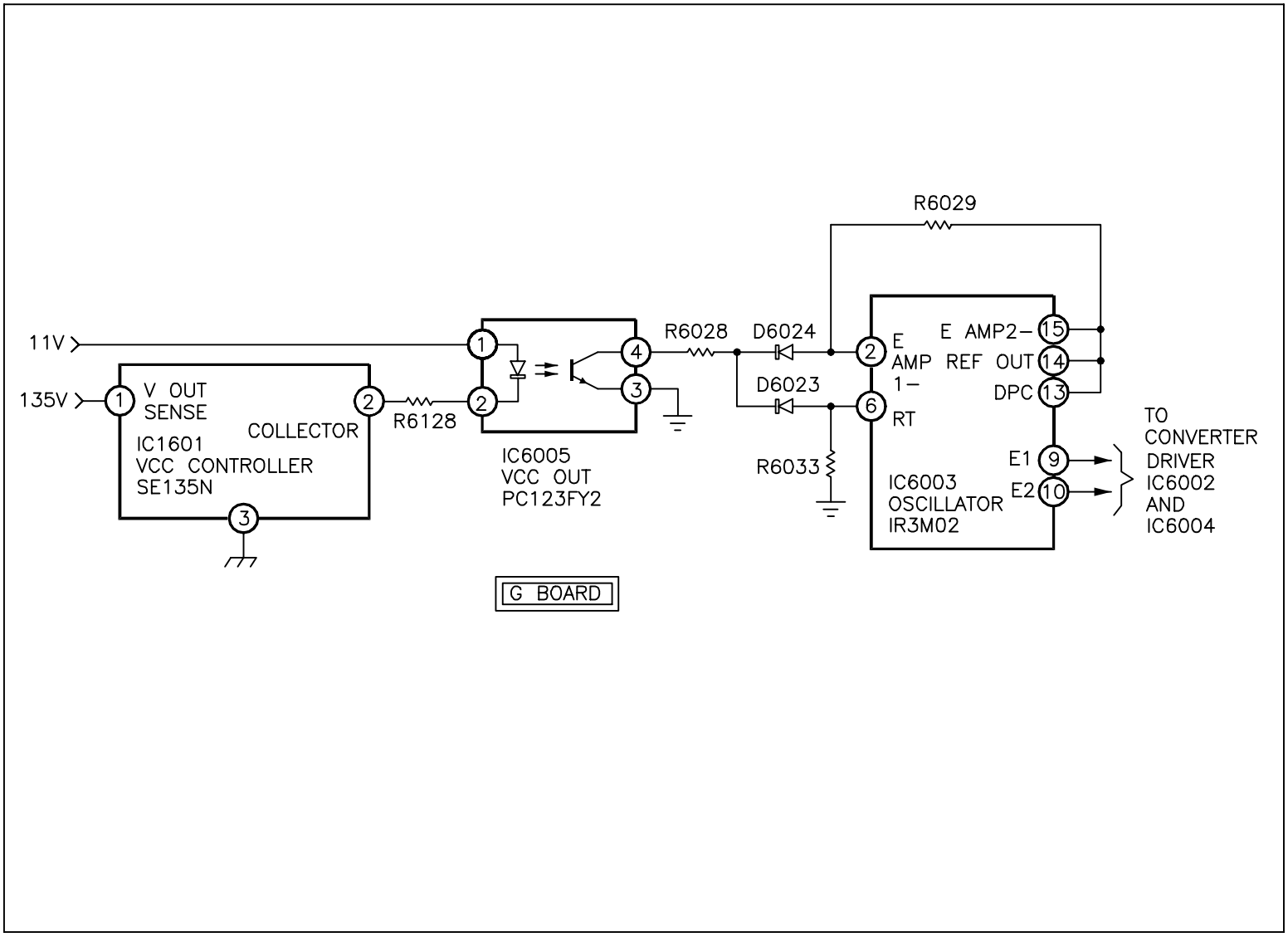
Overview

The regulation circuit is used to provide a control voltage that determines the oscillating frequency of the IC6003 Oscillator. This is done by using the +11 volt line for this circuit's supply and the +135 volt line as the input.

Operation

The +11 volt line is applied to IC6005/1 and then goes through the internal LED connected between pins 1 and 2 of IC6005. The voltage at IC6005 is applied through R6128 to IC1601/2. IC1601 VCC Controller varies the resistance between IC1601/2 and ground. When the voltage on the +135 volt line goes down, the resistance between IC1601/2 and ground also goes down. This causes the current through the internal LED of IC6005 to increase, thereby increasing the brightness of its light. The increase in the brightness of the internal LED causes more current to flow between the C-E junction of the internal transistor inside IC6005. When this transistor conducts harder, it causes more current to flow through D6023 and D6024. This in turn lowers the voltages at IC6003/2 and 6. When these voltages are lowered, the frequency output of IC6003 Oscillator is lowered. The oscillator output is at IC6003/9 and 10. When the frequency output is lowered, it becomes closer to the resonant frequency of the power supply, increasing the voltage on the +135 volt line.

If the voltage on the +135 volt line should rise, the resistance at IC1601/2 and ground will also rise. This causes the current through the internal LED of IC6005 to decrease, which decreases the brightness of the light. The decrease in the brightness causes less current to flow through the C-E junction of the internal transistor inside IC6005. When less current flows through the C-E junction of this transistor, it causes the voltages of IC6003/2 and 6 to rise. This in turn causes the frequency output at IC6003/9 and 10 to increase. This will lower the voltage on the +135 volt line.



REGULATION

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DC Protection

Overview

The RA-4 chassis employs protection for over and under voltage, as well as over current for the +135 volt line. The +22, +19 and +7 volt lines are monitored for low voltage. IC6102 is used to sense over voltage and over current for the +135 volt lines.

Shut Down

Shut down occurs whenever a condition in the protect circuits causes the Q6103/B to go HIGH. A HIGH on Q6103/B turns it ON, causing it to turn ON Q6102. This drops the drive voltage to Relay Drive Q6104/B, turning it OFF. This removes the ground return path for IC6011 and the unit shuts OFF. During shutdown, the voltage from the RM+5 volt line maintains the latch.

+135 Volt Over Voltage

The +135 volt line is input to the protection circuit through D6101 and then to a voltage divider consisting of R6101 and R6102. The voltage developed across R6101 is applied to IC6102/5 Non-inverting input. IC6102/6 Inverting input has a voltage applied to it from the voltage divider consisting of R6110, R6103 and R6104. IC6103 is a programmable zener diode, which is used to stabilize the reference voltage at IC6102/6. This voltage is approximately 2.4 volts and will vary about .1 volts since the entire circuit uses a floating ground. If the voltage at IC6102/5 rises above the 2.4-volt reference, then the output at IC6102/7 will go HIGH. This occurs when the +135 volt line is at about +146 volts.

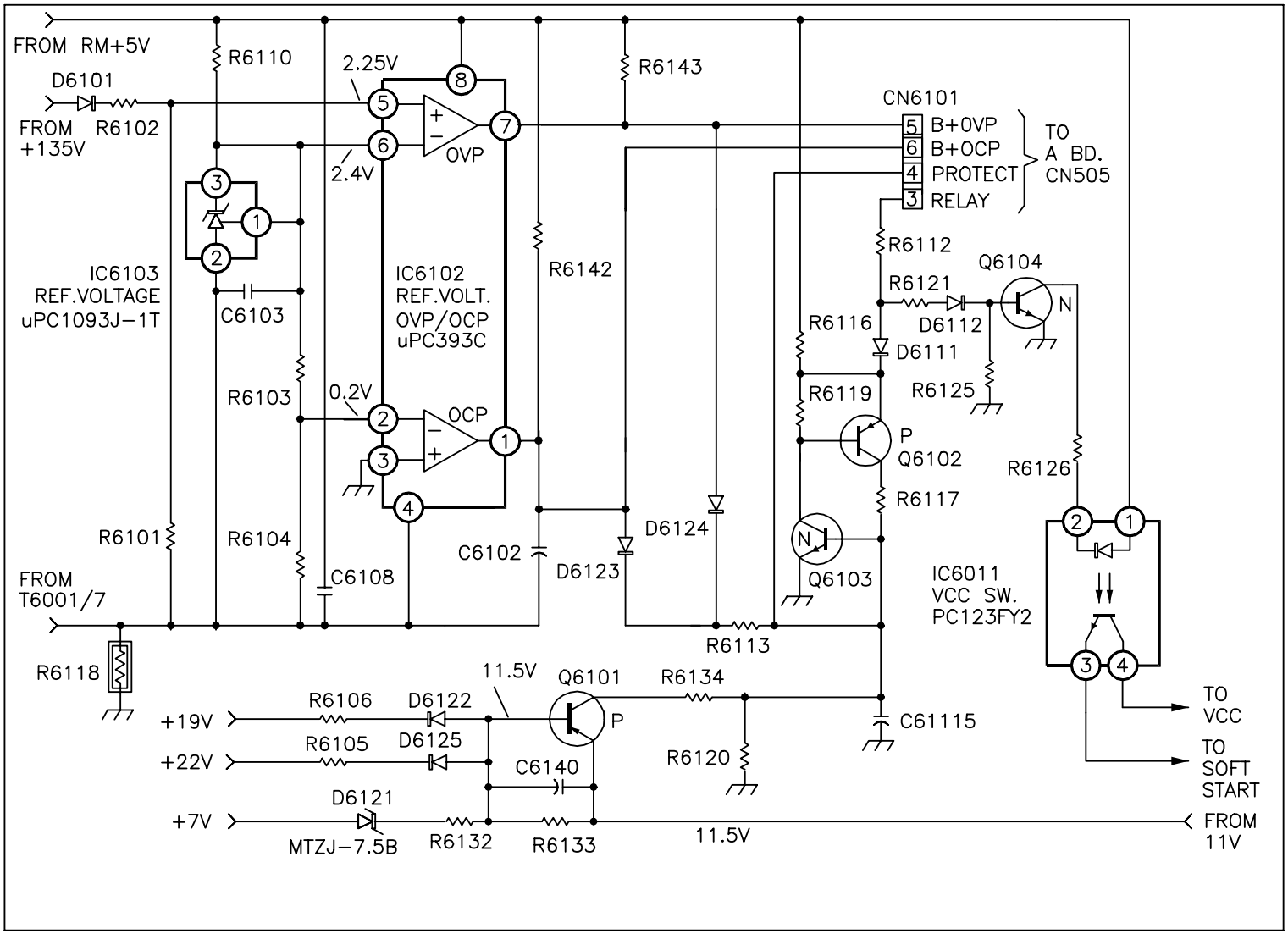
This High output is then applied to the latch circuit and to IC1009 on the A board for the Self Diagnostic feature. If OVP occurs, the Timer LED will flash three times. See the Protection Block section for more details.

+135 Volt Over Current Protection

The over current protection circuit works by monitoring the voltage divider network that consists of R6110, R6103, R6104 and R6118. Essentially we can look at this as the voltage across R6118 since the voltage at IC6102/2 will change with it. This resistor is connected between T601/7 and ground. Since T601/7 is the center tap of the winding that supplies the +135 volt line, any rise in current sourced by that line will cause the voltage across R6118 to lower. This voltage is input into IC6102/2 Inverting input. IC6102/3 Non-inverting input is connected to ground. Therefore, if the current draw on the +135 volt line should cause the voltage at IC6102/2 to become negative, a HIGH will be output at IC6102/1. This HIGH output is applied to the latch circuit and also to IC1009 on the A board for the Self Diagnostic feature. If OCP occurs the Timer LED will flash twice. See the Self-Diagnostics section for more details.

+19, +22, +7 Volt LVP

This protection circuit works by looking at the difference in voltage between the +19, +22 and +7 volt lines and the +11 volt line. If the +19 or +22 volt lines should drop .6 volts below the +11 volt line, this would cause Q6101 to turn ON. If the +7 volt line should drop below 3.5 volts, this would also cause Q6101 to conduct. When Q6101 conducts, it places the +11 volt line on its collector. When this occurs, the latch circuit turns ON and shuts the set down. When this circuit is activated, there is no indication given by the Self Diagnostic circuit. See the Self Diagnostics section for more details.



DC PROTECTION

TVP0811A 1025 12 16 98

PS Troubleshooting

Overview

The key to troubleshooting shutdown problems is to determine if the problem is on the power supply board (G) or one of the other boards in the set. In this section we will give you steps to follow to make this distinction.

Troubleshooting

Often shutdown problems occur too quickly for an indication to be given by the self-diagnostics (flashing Timer LED). These are usually caused by the power supply, but not always. The procedure below will guide you towards the resolution of this type of a problem by notifying you if the problem is with the power supply's G board.

Symptom: Shutdown - No indication given by self-diagnostics. Timer LED continuously flashes.

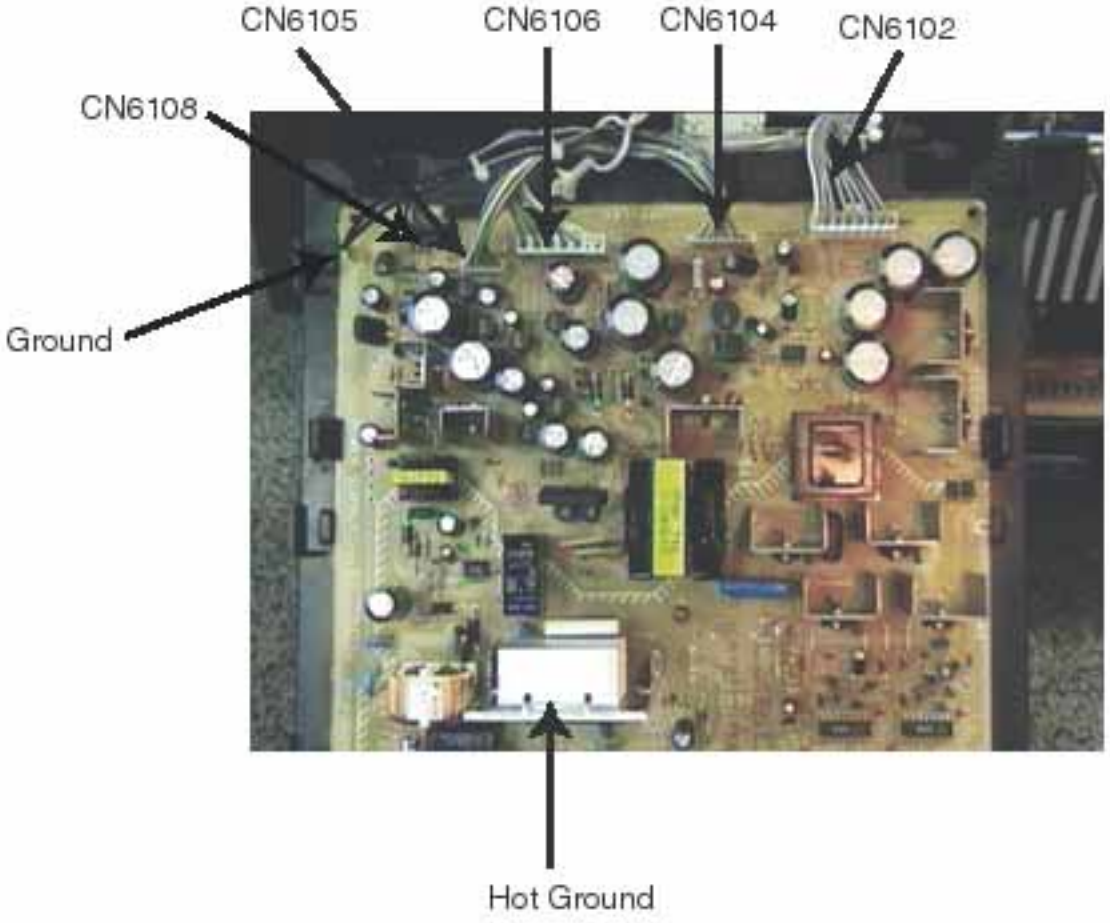
1. Unplug CN6106 from the G board. If the set comes up with sound but no picture, replace or repair the D board. If the picture does not come back up, reconnect the plug to CN6106 and move to the next step.
2. Unplug CN6102 from the G board. If the set comes up with no sound, replace or repair the K board. If the sound does not come back up, reconnect the plug to CN6102 and move to the next step.
3. Unplug CN6105 from the G board. If the set comes up, replace the D board or replace IC5005 and IC5006. If it does not, move to the next step.
4. Check fuses PS6101 and PS6103 on the G board. These fuses are for the +7 volt line. If they are open, the set will shut down immediately. If they are OK, move to the next step.
5. We have unplugged all the connectors at this point that can be disconnected and have the set partially run. We can run the set fully unloaded if we lower the AC voltage. First fully unload the G board from the rest of the set by unplugging CN6102, CN6104, CN6105 and CN6106. Now supply 55VAC to the set and press the power button on the remote or the front panel. The power relay will click and the Timer LED will flash continuously. Now you can check the voltages of the power supply using the table below. It is very important that you use 55VAC. If you raise the voltage to 60V, the supply will shut down because of OVP. If the voltage is below 50VAC, there will not be enough voltage to turn on the power relay and it will chatter.

The following table shows the voltages present with the supply fully unloaded and 55 volts AC applied.

Measurement Point	Normal Voltage	Voltage Unloaded with 55VAC applied
CN6106-1	+135	+78
CN6016-3	-135	-133
CN6106-5	+15	+9.9
CN6106-6	-15	+12
CN6105-1	+22	+10.7
CN6105-6	-22	-10.9
CN6104-4	+7	+5.6
CN6104-7	+11	+10.3
CN6104-9	+33	+31

Other problems

- More often than not, no sound is caused by a problem with PS6103 and PS6104. Please note this is a very unlikely problem. Shutdown caused by the K board is often indicated by the self-diagnostic circuit, causing the Timer LED to flash eight times. If this type of shutdown occurs, unplug CN6102. If the set operates but there is no sound, replace or repair the K board.
- If the set displays a symptom of no sub deflection, fuses PS6105 and PS6106 on the G board should be checked.



Location	Normal Voltage		Location	Normal Voltage
CN6102/2 and 3	-19 Volts		CN6105/3	+15 Volts
CN6102/7 and 8	+19 Volts		CN6105/4	-15 Volts
CN6104/2	+15 Volts		CN6105/12	-22 Volts
CN6104/4 and 5	+7 Volts		CN6106/1	+135 Volts
CN6104/7	+11 Volts		CN6106/3	-135 Volts
CN6104/9	+33 Volts		CN6106/5	+15 Volts
CN6105/1	+22 Volts		CN6106/6	-15 Volts

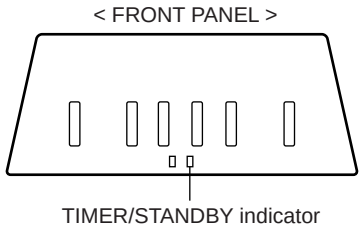
Protection Block

Overview

The RA-4 chassis employs a Self-Diagnostic system that uses the Timer LED and an on screen menu to help indicate where the problem with the set has occurred. Generally you will have to use the flashing LEDs since the set will be shut down. In order to turn the set off once shutdown has occurred, AC power must be disconnected.

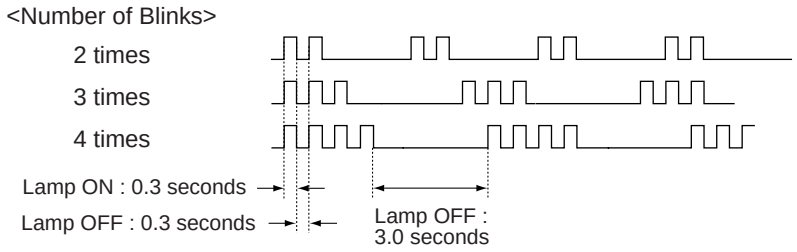
Diagnostic Indication

When a problem occurs that causes shutdown, the Timer LED may blink in a pattern as shown below:



•EXAMPLE

<Diagnosis Items>
- +B overcurrent
- +B overvoltage
- Vertical deflection stop



The number of times the LED blinks may correspond to that shown in the following table:

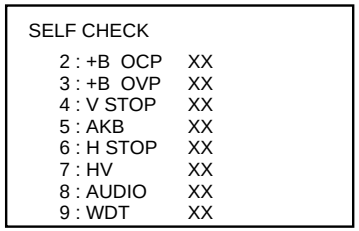
Diagnosis item	Standby/ sleep lamp, Number of blinks	Self-diagnosis screen display, Diagnosis item:Results
• Power not ON	Not lit	
+B OCP detection	LED blinks 2 times	2 : +B OCP XX
+B OVP detection	LED blinks 3 times	3 : +B OVP XX
V detection	LED blinks 4 times	4 : V STOP XX
AKB detection	LED blinks 5 times	5 : AKB XX
H detection	LED blinks 6 times	6 : H STOP XX
HV abnormality detection	LED blinks 7 times	7 : HV XX
Audio abnormality detection	LED blinks 8 times	8 : AUDIO XX

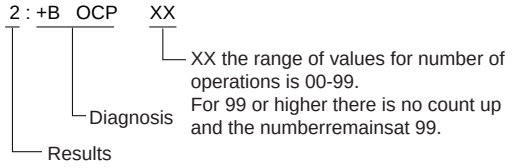
∗ : XX the range of values for number of operations is 00-99. For 99 or higher there is no count up and the number remains at 99.

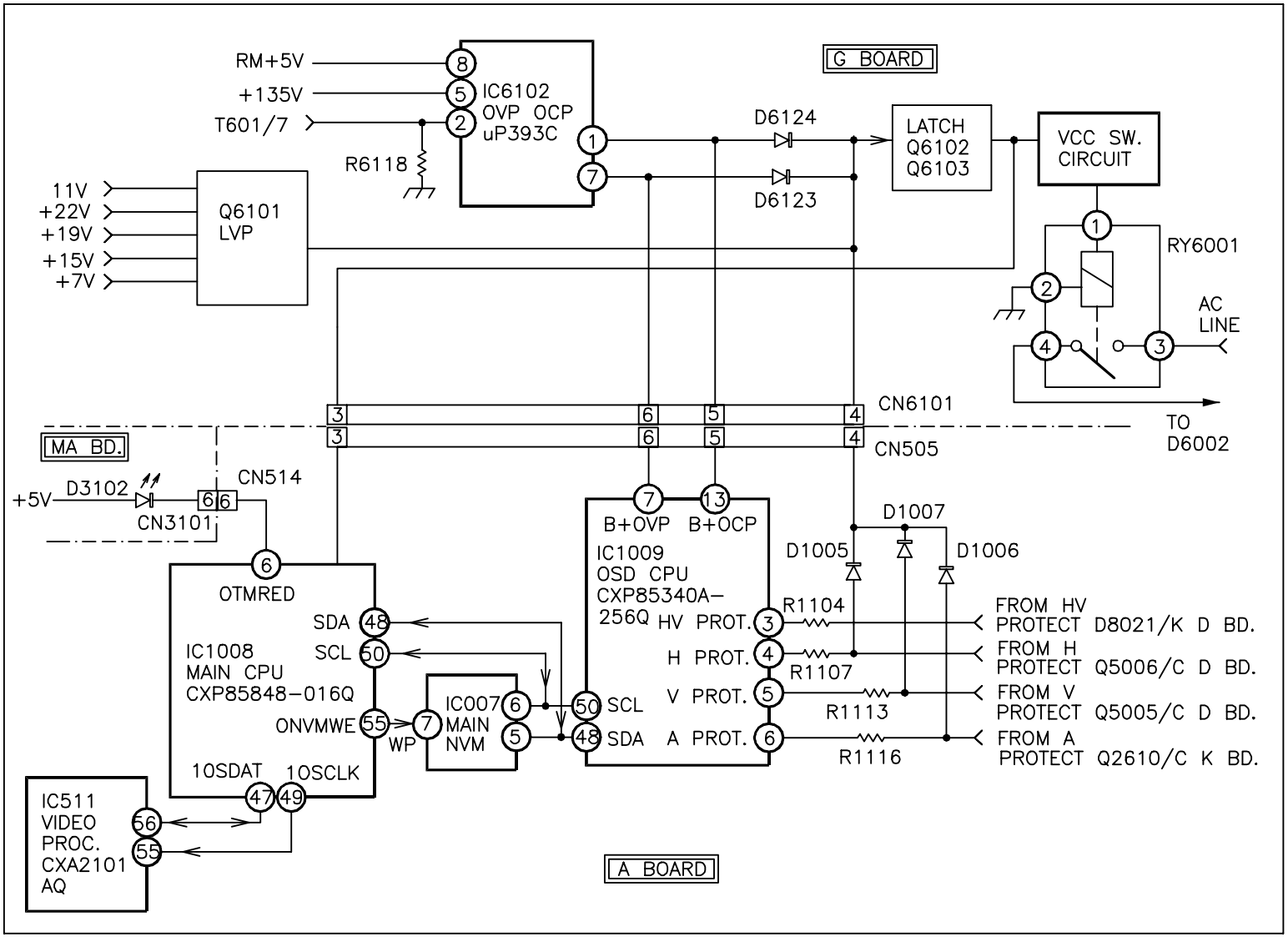
If the problem is intermittent and you can get the set to operate, you can display a menu showing the number of times failures have occurred. This is done by pressing the following sequence of buttons on the remote.

Display Channel 5 Vol - Power

The display will look as follows.







PROTECTION BLOCK

tvp08j48 1026 12 18 98

This display can be cleared by pressing **8 and Enter** in this mode.

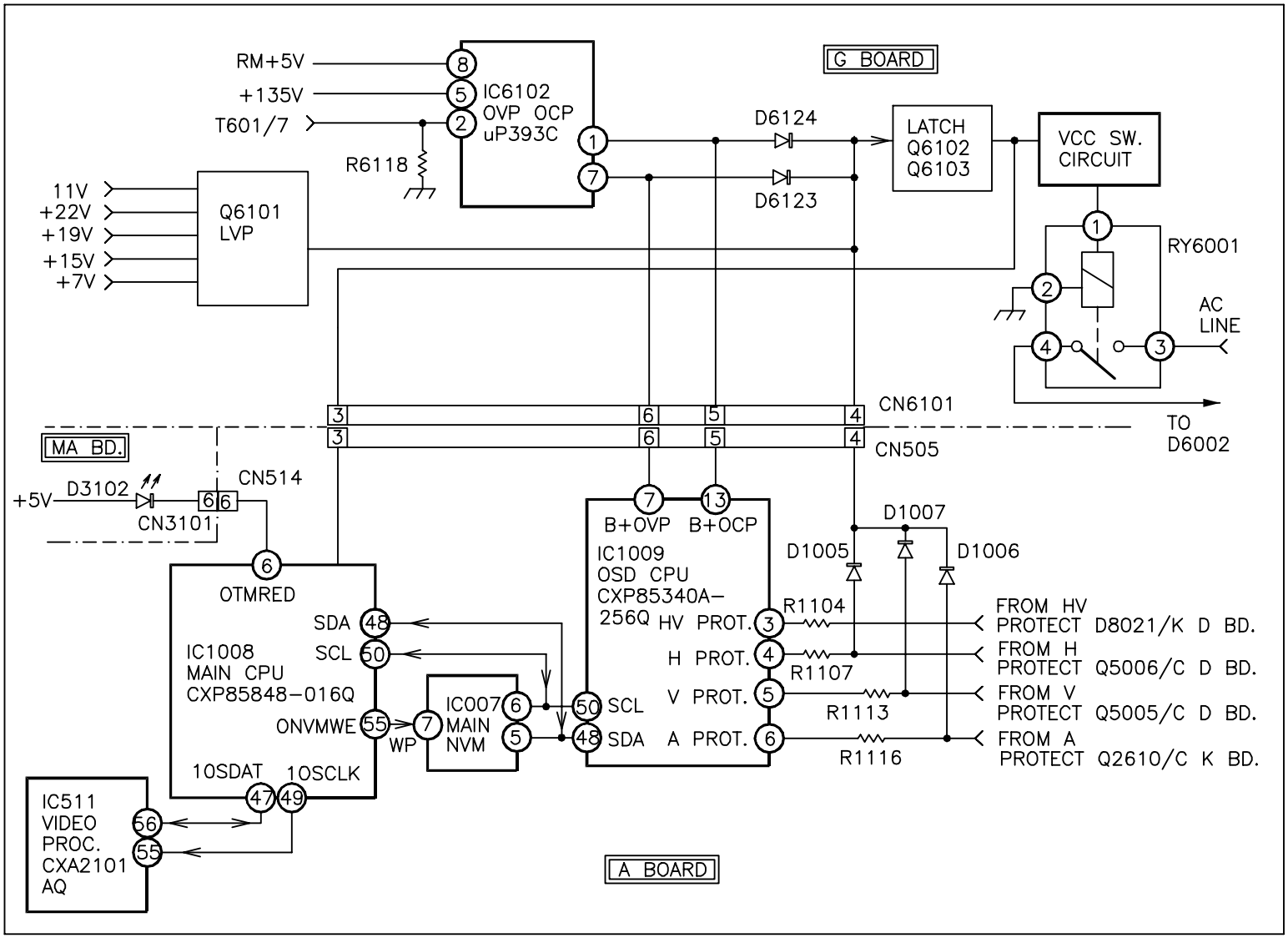
There may be situations when the diagnostic system will not work. These situations generally occur when there are power supply problems with the set. When this occurs, the LED will blink continuously at .3 second intervals. More information on troubleshooting these problems will be covered in the power supply section. Keep in mind that other power supply problems could cause a false indication to be given by the Self-Diagnostic section.

Circuit Description

All of the circuits that can be indicated by the self-diagnostic have an input to IC1009 OSD CPU, except for the AKB circuit. The indication from AKB is sent over the I²C data lines to IC1008 Main CPU. This data is then sent to IC1009 OSD CPU to be displayed. These indicators are from protection circuits, which will be discussed in more detail in the individual circuit descriptions. They all output a HIGH when they are activated. When a failure is received from one of the circuits, it is stored in IC1007 NVM. This can be helpful when problems are intermittent. Keep in mind that failures might not always indicate the correct circuit. For example, if there is an intermittent HV failure, the indication could be displayed as AKB failure.

In addition to sending a signal to the OSD processor, all of these protect lines are connected to the power supply latch on the G board, except for AKB and HV. This means that if there is a protect condition indicated by any circuit except AKB or HV, the set will shut down. When the set shuts down, the Timer LED will blink as stated previously. The set must be unplugged before you can attempt to operate it when a shutdown occurs.

There is also an additional LVP circuit on the G board that will not be indicated when a failure occurs. This is due to a problem in this area that causes a number of dilemmas and usually occurs too quickly for an indication to be given. When there is a failure in this area, the Timer LED will flash continuously every .3 seconds.



PROTECTION BLOCK

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Reset

Overview

There are two reset circuits in the RA-4 chassis. The first reset occurs at initial plug-in, and the second each time the set is powered ON. The initial plug-in reset only resets IC1008 Main CPU. All other ICs that need resetting are reset each time the set is turned ON.

Initial Reset

When the set is plugged-in, Standby +5 volts is developed on the G board. This voltage is sent to the A board from CN6101 to CN505. This voltage is called RM+5 on the G board and ST-5V on the A board. It is then applied to IC1008 Main CPU and IC1010 Reset. The purpose of IC1010 Reset is to hold the reset line low until the voltage on the ST-5V line reaches a threshold around 4.3 volts. When this threshold is reached, IC1010/4 is released from ground and current flows through pull-up resistor R1117 and R1126. In reset, IC1008/9 I Reset is held low until C1033 charges. C1034 and C1036 are used to filter out any noise or spikes that may occur on the reset line. IC1008 Main CPU will begin to function after reset occurs.

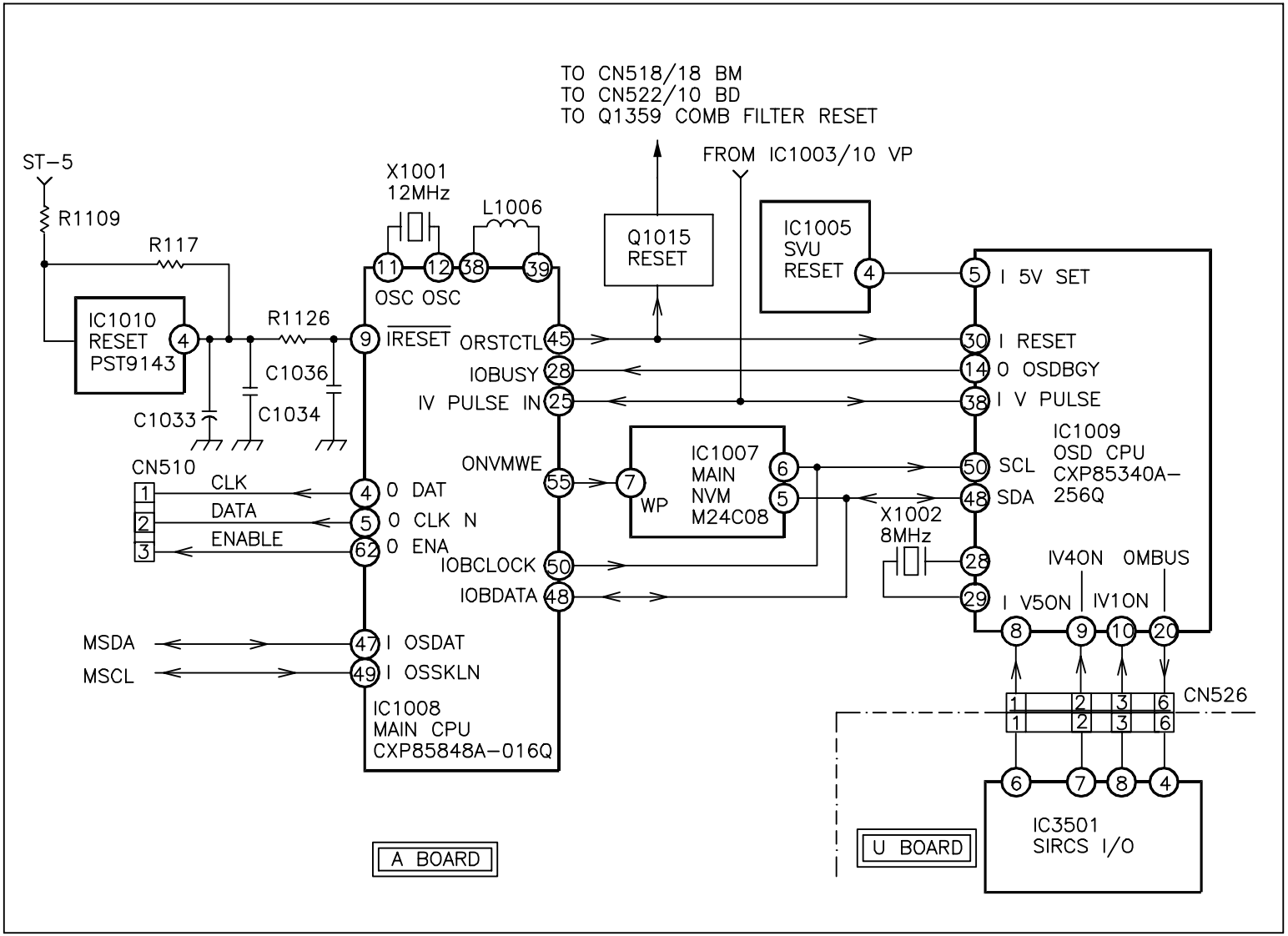
After IC1008 Main CPU is reset, the data is read from IC1007 NVM and stored in its own internal RAM. This data contains information on such things as global video settings, video mode presets and user settings, etc. It does not contain the data for Registration or MID settings. After this data is read, the data and clock lines will be high with periodic low going pulses. The CPU is now awaiting further instructions. This B I²C bus is the only active bus when the unit is in standby mode. While the set is running, it will have the same data present as the Main or M I²C bus.

If the reset line is held LOW for some reason, the set would appear to be completely dead. X1001 and X1002 would continue to oscillate. IC1008/38 and 39 are only active when Closed Caption is selected. These pins are for CCD OSD horizontal positioning and will have a 12 MHz signal on them when closed captioning is ON. IC1008/48 B Data and IC1008/50 B Clk would be HIGH with no activity on them. You would normally always see some activity on these lines.

Power ON Reset

When the set is powered ON, there is a LOW going reset pulse sent from IC1008/45 O RSTCTL to IC1009/60 I Reset that resets IC1009 OSD CPU. This reset pulse is also sent to Q1015 Inverter. Q1015 inverts this pulse to a HIGH going reset pulse. It is then distributed to other parts of the set that need resetting. This reset pulse is sent to CN518/18, which is connected to the BM board, and CN522/10, which is connected to the BD board. It also goes to Q1359 Inverter where it is inverted and then sent to IC1306/57 RST B. IC1306 is the 3D Comb Filter. Once this reset has occurred and the set is operating, timing for the I²C bus is set by the VP pulse, which is input to IC1008/25 and IC1009, as well as the other CPU's in the set. This pulse allows synchronization of the data. Once it is received, there will always be activity present on the M and B I²C busses.

One "bug" that may be encountered, although very rarely, has to do with reset and S-Link. You may experience a problem since IC1009 OSD CPU is not reset at initial plug-in and the S-Link signal is input to IC1009 OSD CPU. If an S-Link power up signal is sent to the set after it was unplugged and then plugged back in, but before it was turned ON, the set may not respond to the S-Link signal. However if the set was unplugged, re-plugged and turned on at least once, this will not occur.



RESET

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System Block Diagram

Overview

This section discusses the System Block for the RA-4 chassis and will show the four different I²C busses. The B bus is active during standby. The M bus is the main bus and controls most of the set. The P bus is part of the auto-registration circuit and controls this circuit's functions. Finally, the MID bus controls the MID functions such as PIP and Twin-View.

The diagram also shows two 3-line busses. IC1009 OSD CPU uses one to communicate with IC1004 OSD Processor. The other bus is used by IC1008 Main CPU to control IC2105 Dolby Processor.

B (Standby) Bus

The B bus is the only bus that is active in the standby mode. It will have the same data on it as the M bus during regular set operation. There are only three ICs on this bus. They are IC1008 Main CPU, IC1007 NVM and IC1009 OSD CPU. In addition to these ICs, the factory test connector is on this bus. This is so that data can be written right to the NVM during production. It also allows for outside control of the set on the production line. This connector would be the one that the Registration Jig for the RA1 and RA2 chassis' would be connected. That jig is not usable on the RA4 chassis due to the different convergence system.

Connector or IC	MSDA	MSCL
IC1008 Main CPU	48	50
IC1009 OSD CPU	50	48
IC1007 NVM	6	5

M (Main) Bus

The I²C bus controls most of the set. There is activity on it at all times when the set is powered ON. Any IC on the bus could cause loading problems. The following table shows which pins on each IC are on the bus. If there is a loading problem, these pins can be lifted from the IC to find the problem.

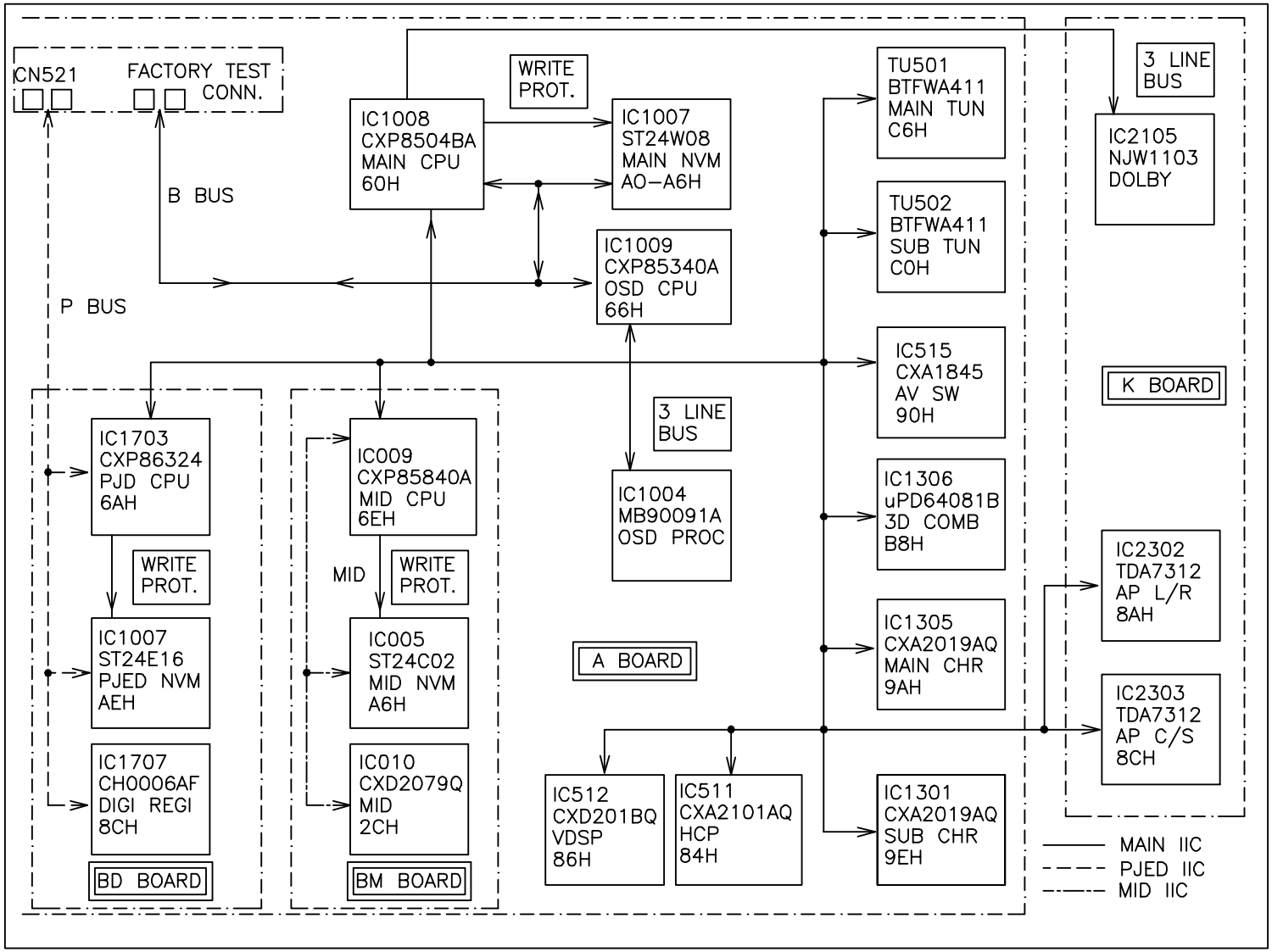
Connector or IC	MSDA	MSCL
CN518 (BM)	15	14
CN521 (Bus Connector)	10	11
CN522 (BD)	15	14
IC511 Video Processor	56	55
IC515 AV Switch	32	31
IC1008 Main CPU	47	49
IC1301 Sub Chroma	37	36
IC1305 Main Chroma	37	36
IC1306 3D Comb	60	59
IC2302 L/R Tone Control	29	30
IC2303 C/S Tone Control	29	30
TU501 Main Tuner	SDA	SCL
TU502 Sub Tuner	SDA	SCL

P (Auto Registration) Bus

The P data bus handles the operation of the registration circuit. It operates independently of the M bus. There will always be activity on this bus when the set is ON. This is because the IC1703 PJED CPU instructs IC1707 Regi Correction to read data from IC1704 NVM to refresh its internal RAM. These commands are sent every vertical period and it takes approximately 20+ vertical periods to refresh all the data. The reason we refresh so often is due to registration malfunctions that occurred during CRT arcing and ESD tests.

MID Bus

The MID bus is located on the BM board and controls the functions of the MID circuit. Commands are sent from IC1008 Main CPU to IC009 MID CPU, which commands IC010 MID Controller to carry out MID functions. Data is only sent during MID operation.



DATA COMMUNICATION BLOCK DIAGRAM

TVP08J36 1019 12 21 98

Video Path Block

Inputs

The two tuner video outputs along with all video signals that enter the unit, except the Video 5 component input, are input into IC515 A/V Switch. IC515 A/V Switch switches these video signals to three different paths. The first is the main video path, next is the sub video path and last is the select output. The select output is used to send a composite version of an input to an output jack on the rear panel. This is selectable in the setup menu. The default setting is to output the main video.

Main Video

The main video path is used to carry composite or Y/C (S Video) to IC1306, the 3D Comb Filter. If a composite signal is used, it is looped out of and back into IC515 A/V Switch, then back out to IC1306 3D Comb Filter. If an S Video input is used, then the Y signal is looped out and then back into IC515 A/V Switch along the same path as the composite input. It then goes to IC1306, 3D Comb Filter. The C signal is output from IC515 A/V Switch to IC1306, 3D Comb Filter.

IC1306 3D Comb Filter is used to separate Y and C signals from the composite signal input, and also performs some of the necessary noise reduction and video processing adjustments. If a Y/C signal is input, then IC1306 3D Comb Filter will just perform its noise reduction and video processing functions. The C signal is output to IC1305 Main Chroma Decoder. The Y signal is output to IC1307 YUV Switch where it is switched though to IC1305 Main Chroma Decoder.

IC1305 Main Chroma Decoder takes the Y and C input signals and converts these signals to component video. Component video consists of Y, B-Y and R-Y. These signals are also known as Y, U and V and Y, Pb and Pr. In this book we will refer to these signals as Y, U and V. These main Y, U and V signals are then input to IC1307 YUV Switch.

IC1307 YUV Switch switches between the main YUV signals and the YUV signal from Video 5 component input. It also mixes in the Closed Caption Data from IC1008 Main CPU. The CCD signal is input as a RGB signal and matrixed to be output as part of the main YUV signal.

The outputs from IC1307 YUV Switch are then input to the BR board (DRC) and the BM board (MID). The BR board outputs signals that are the main video signal and these outputs are input to IC511 Video Processor. The BM board is used for PIP and Twin View functions.

Sub-Video

The sub-video path is used to carry sub-video to the BM board where it is converted for PIP and Twin-View functions. If a composite signal is input to IC515 A/V Switch, it would be output to CM501 Glass Comb Filter and then input back to IC515 A/V Switch as Y and C. If the signal were an S Video input, it would pass directly to the Y and C outputs of IC515 A/V Switch.

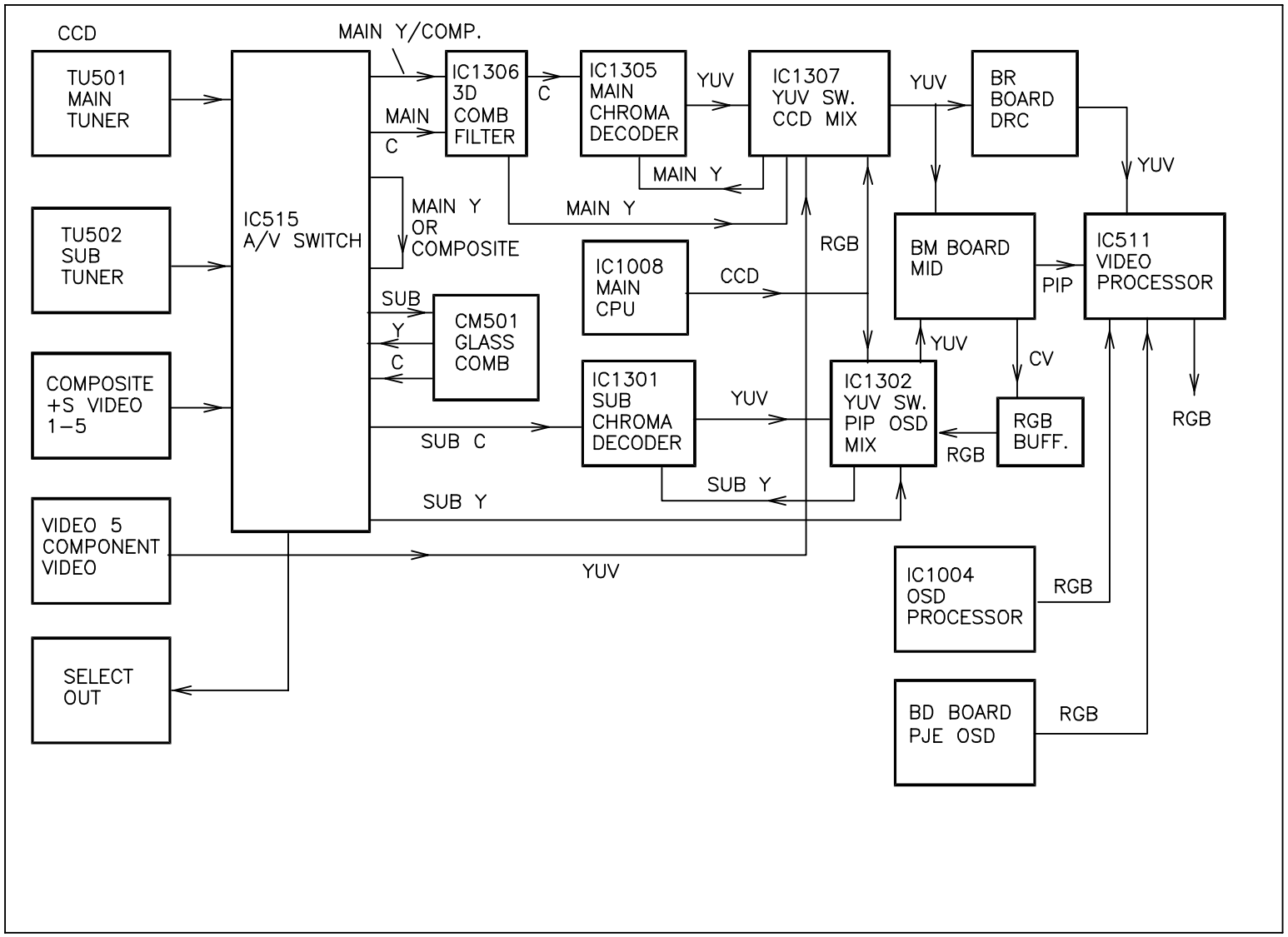
The C signal is input to IC1301 Sub Chroma Decoder while the Y signal is input to IC1302 Sub YUV Switch and then switched to IC1301 Sub Chroma Decoder.

IC1301 Sub Chroma Decoder takes the Y and C input signals and converts these signals to component video. These sub Y, U and V signals are then input to IC1302 Sub YUV Switch.

IC1302 Sub YUV Switch is used to select between the sub YUV inputs and the YUV input from the Video 5 component input. It also mixes in the Sub-video OSD, which comes from the BM board, into the sub YUV signal. The output of IC1302 Sub YUV Switch is output as YUV into the BM board for use with PIP and Twin View functions. The signals from the BM board are input to IC511 Video Processor.

IC511 Video Processor

The IC511 Video Processor is used to switch or mix in the appropriate signals among its many functions. These signals are the main YUV, sub YUV, OSD RGB and PJED OSD RGB signals. These signals are converted to R, G and B to be output to the video amplifiers on each of the C boards.



VIDEO PATH BLOCK

TVP08J49 1028 12 3 98

Input Switching

Overview

The two tuners' video outputs, along with all video signals that enter the unit except the Video 5 component input, are input to IC515 A/V Switch. In accordance with commands received from IC1008 Main CPU, IC515 A/V Switch switches these video signals to three different paths. The first is the main video path, second is the sub video path and third is the select output.

Inputs

The five video inputs each have separate composite and S Video inputs and all are contained in one package as shown by J505 in the related drawing. Each package also contains left and right audio inputs. All of these jacks input to IC515 A/V Switch where they are switched to the appropriate parts of the circuit by I²C data from IC1008 Main CPU (not shown).

IC515 A/V Switch is able to determine if the S video input is being used because of an internal switch in the S video jack. This switch is connected to a voltage divider that is connected to the S Switch input for each of the 5-video inputs. If there were an S video source connected, then the S SW input would be LOW. This causes the internal switch in IC515 A/V Switch to allow the S video input to be passed to the Y and C outputs. If there is nothing plugged in to the S video jack, the voltage on the S Switch line will be 2.5 volts. The operation of the Video 5 circuit is somewhat different because it also has component video input. There is a switch on the Pr input that goes to an additional circuit that places five volts on the S switch line. No video will pass to the Y and C outputs when a cable is plugged in to the Pr input. This will be discussed further in the YUV Switch section.

In addition to the 5-video inputs, there are also two tuner inputs. These tuners are all the same type so that this set may have the audio swap function when using PIP features. The sub tuner will never produce the main picture. If a picture swap takes place when using PIP, the tuners will be re-tuned. The main and sub tuner's video signals each pass through identical buffers before being input to IC515 A/V Switch. In addition, audio is input to IC515 A/V Switch from each tuner. The tuners are not re-tuned for the audio swap function.

Outputs

Main Video

IC1008 Main CPU determines what input will be switched to each output by interpreting the customer's input and sending commands to IC515 A/V Switch for proper execution.

Regardless of which input is selected for the main picture, it will follow the following path: The composite video or Y signal will be output from IC515/38 V Out 1 to Q533 Buffer. It is then input to IC515/49 Y In and switched through IC515 A/V Switch to be output at IC515/56 Y Out. The main composite or Y signal is then sent to the main Y buffer before being input to IC1309. IC1309 is an A/D Converter that will digitize the composite or Y signal for input to the 3D Comb Filter.

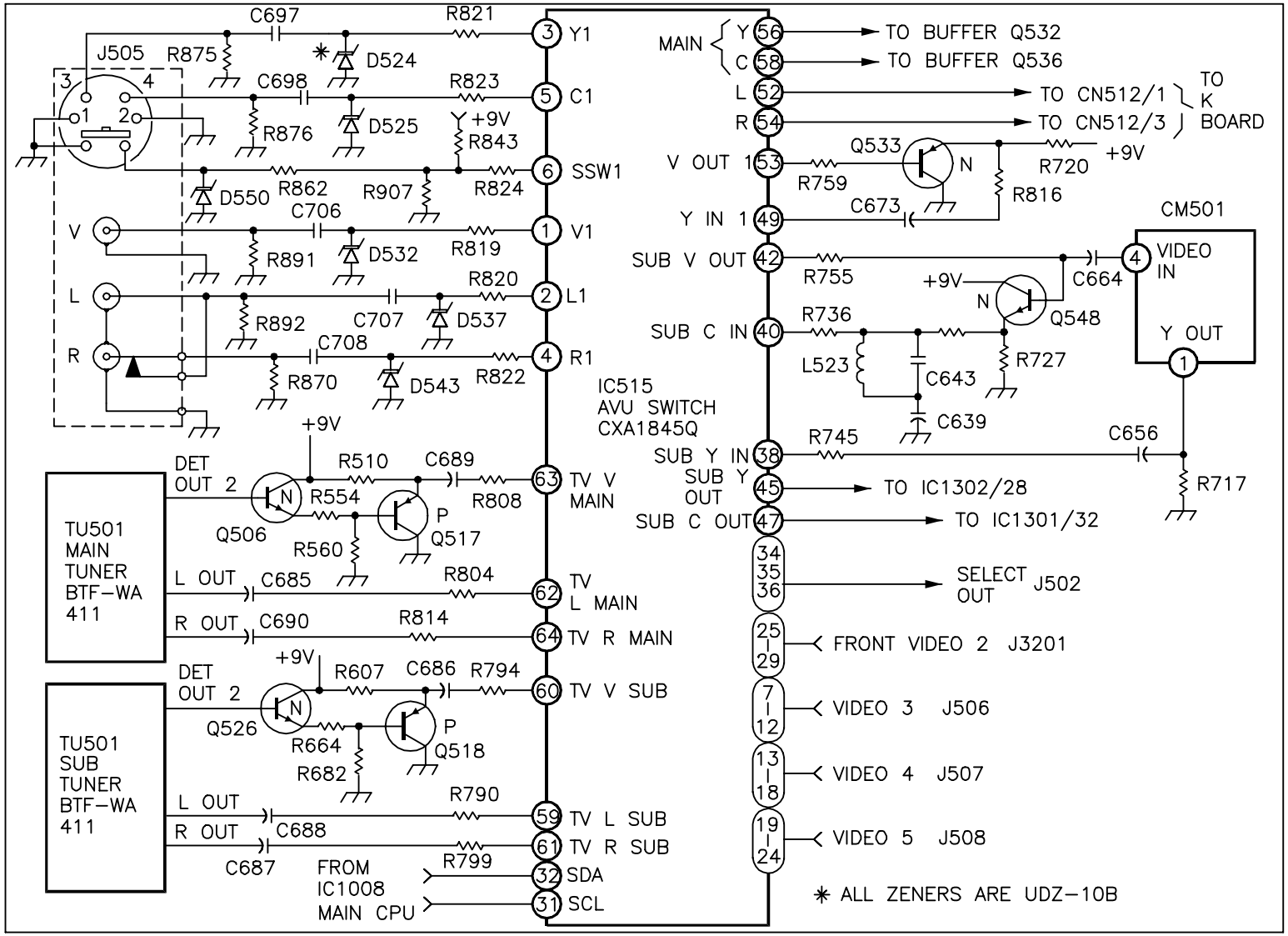
If an S video input is selected, then the C signal will be output at IC515/58 C Out. It is input to the main C buffer before being input to IC1306/96. IC1306 is the 3D Comb Filter.

Sub Video

If a composite sub video input is selected, it is output at IC515/42 Sub V Out and then sent to CM501/4 Glass Comb Filter. CM501 Glass Comb Filter is used to separate the Y signal from the chroma in the composite sub video signal. The Y signal is output CM501/1 and input to IC515/38 Sub Y In. The composite signal is also input to the base of Q548, which uses L523 and C643 and C639 to filter out the 3.58 MHz chroma signal. The signal is then input to IC515/40 Sub C In. The sub Y and C signals are output from IC515/45 and 47 respectively. If an S video signal is input, the signals will be output directly at IC515/45 and 47.

Select Out

The select out outputs one of the input signals as composite video from IC515/34, along with audio from IC515/34 and 36. The selected output is determined using the setup menu. These signals leave the set at J502.



INPUT SWITCHING

TVP08J23 997 12 17 98

Main Y and C Buffers

Overview

The purpose of the Y and C buffers is to pass the signal from the input switching circuit to the 3D Comb Filter. While performing this, the circuit filters out unwanted frequencies above 7 MHz. In addition to these functions, this circuit also separates the horizontal and vertical sync from the Y or composite video signal.

Y Buffer

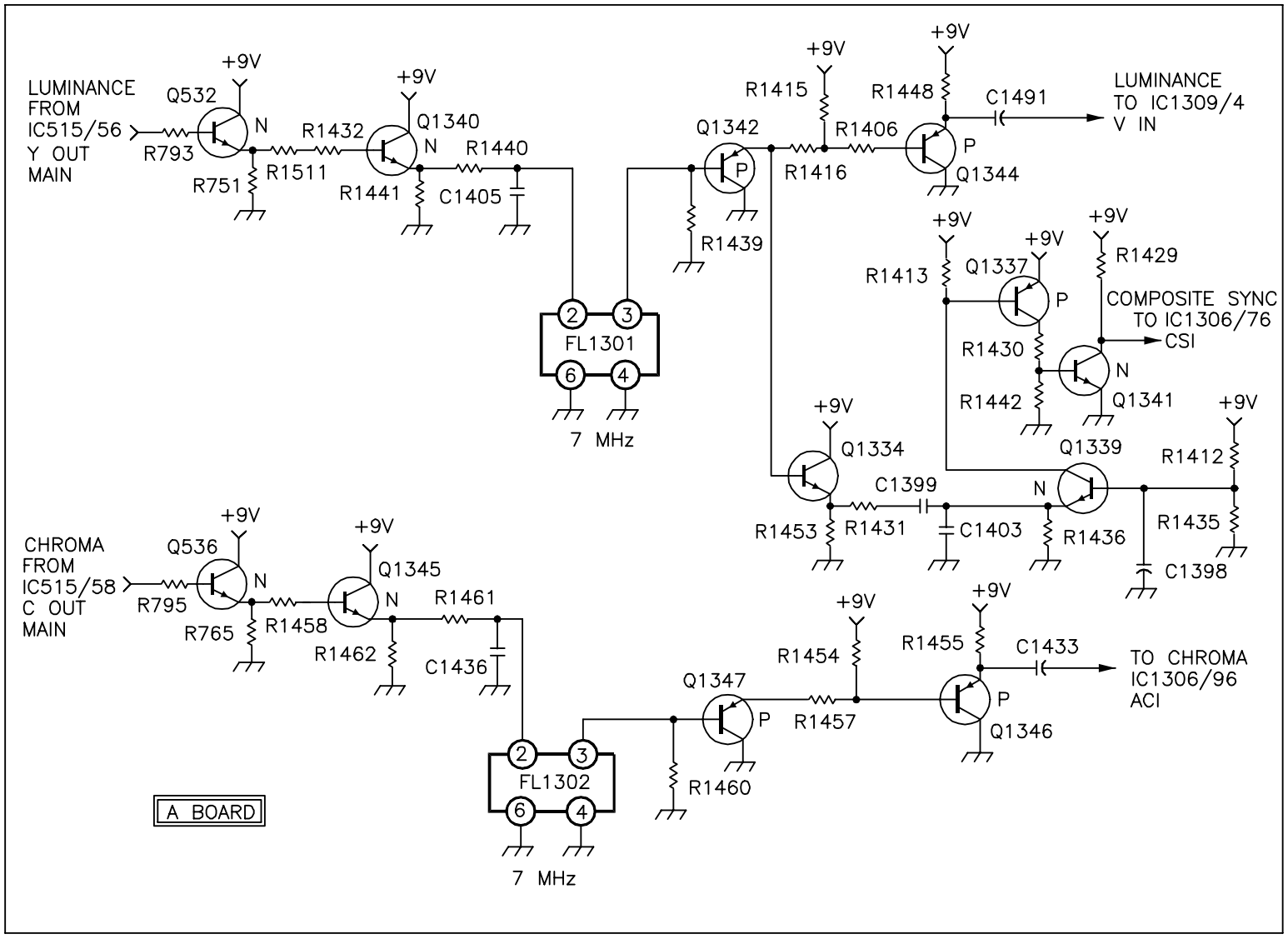
The Y or composite signal is passed through Q532, which is the output buffer for the input switching circuit. It then goes to Q1340, which provides further buffering for the signal before it enters FL1301. The signal enters FL1301/2 and exits FL1301/3. FL1301 filters out all unwanted signals above 7 MHz. After being filtered, the signal goes through another buffer, Q1342. The signal exits Q1342/E and is split to Q1344/B and Q1334/B. Q1344 provides additional buffering for the signal, which is then sent through C1491 and to IC1309 ADC. If you try to probe Q1344/B with a scope, you will load the signal and the picture will become distorted. Q1334 is the input to the sync separator circuit.

Sync Separator

Q1334 is the input to a differential amplifier that consists of Q1334 and Q1339 and their associated components. While Q1334/B has the Y or composite signal input to it, Q1339/B is set to a DC reference level of 3.9 volts. The result of these inputs, which is output at Q1339/C, is that only the sync signals are amplified since they are below the threshold. The signal leaving Q1339/C contains vertical and horizontal sync pulses. This signal is applied to Q1337, which acts as a buffer. Next, the signal is applied to Q1341, which amplifies and inverts the sync signals. Negative going vertical and horizontal sync signals are output from Q1341/C. This signal is then sent to IC1306 3D Comb Filter.

C Buffer

The C signal is only present when an S video input is used. The C signal is passed through Q536, which is the output buffer for the input switching circuit. It then goes to Q1345, which provides further buffering for the signal before it enters FL1302. The signal enters FL1302/2 and exits FL1302/3. FL1302 filters out all unwanted signals above 7 MHz. After being filtered, the signal goes through another buffer, Q1347. The signal exits Q1347/E and is split to Q1346/B and Q1336/B. Q1346 provides additional buffering for the signal, which is then sent through C1433 and sent to IC1306 3D Comb Filter.



MAIN Y/C BUFFERS

TVP08J24 996 12 17 98

3D Comb Filter

Overview

The 3D Comb Filter is used to separate the Y and C signals in a composite video signal. In this section we will discuss what a 3D Comb Filter is and why we need to use one. In addition we will discuss the comb filter circuit in the RA-4 chassis.

What is a 3D Comb Filter?

History

In order to produce a picture, we need to separate the Y and C signals from the composite video signal. This is necessary to extract the separate R, G and B signals that are needed by the CRT. In the early days of television through the late 70's, a trap filter was used to separate the Y and C signals. This method is now referred to as a 1D filter. This system functioned, but severely limited the resolution of the displayed signal. It also produced unwanted picture artifacts such as dot crawl, which are moving dots at the edge of a black and white transition.

A new filter was used in the late 70's. This filter was called a 2D-comb filter because it used the signal in the horizontal and vertical dimensions. It used delay lines to look at two consecutive horizontal lines and compared them. For example, if line 140 could be delayed and then compared to line 141, we could get a much better horizontal resolution and a reduction in dot crawl. However, these filters have trouble with diagonal lines and fine details. These problems result in a loss of vertical resolution.

Recently we have overcome these limitations through the use of the 3D-comb filter. This filter not only uses the horizontal and vertical dimensions, but adds a third dimension - time.

3D Comb Filter

As mentioned above, the third dimension in a 3D-comb filter is time. This means that not only do we compare the line above or below a horizontal line, but we also compare that line to the corresponding line in the frame before and after it. This means that if we were processing line 140 in frame 20, we would compare it not only to line 139 and 141 in frame 20, but also with line 140 in frames 19 and 21. This type of processing requires a great deal of memory since it must be capable of storing two full frames of video for the constant comparisons that are occurring.

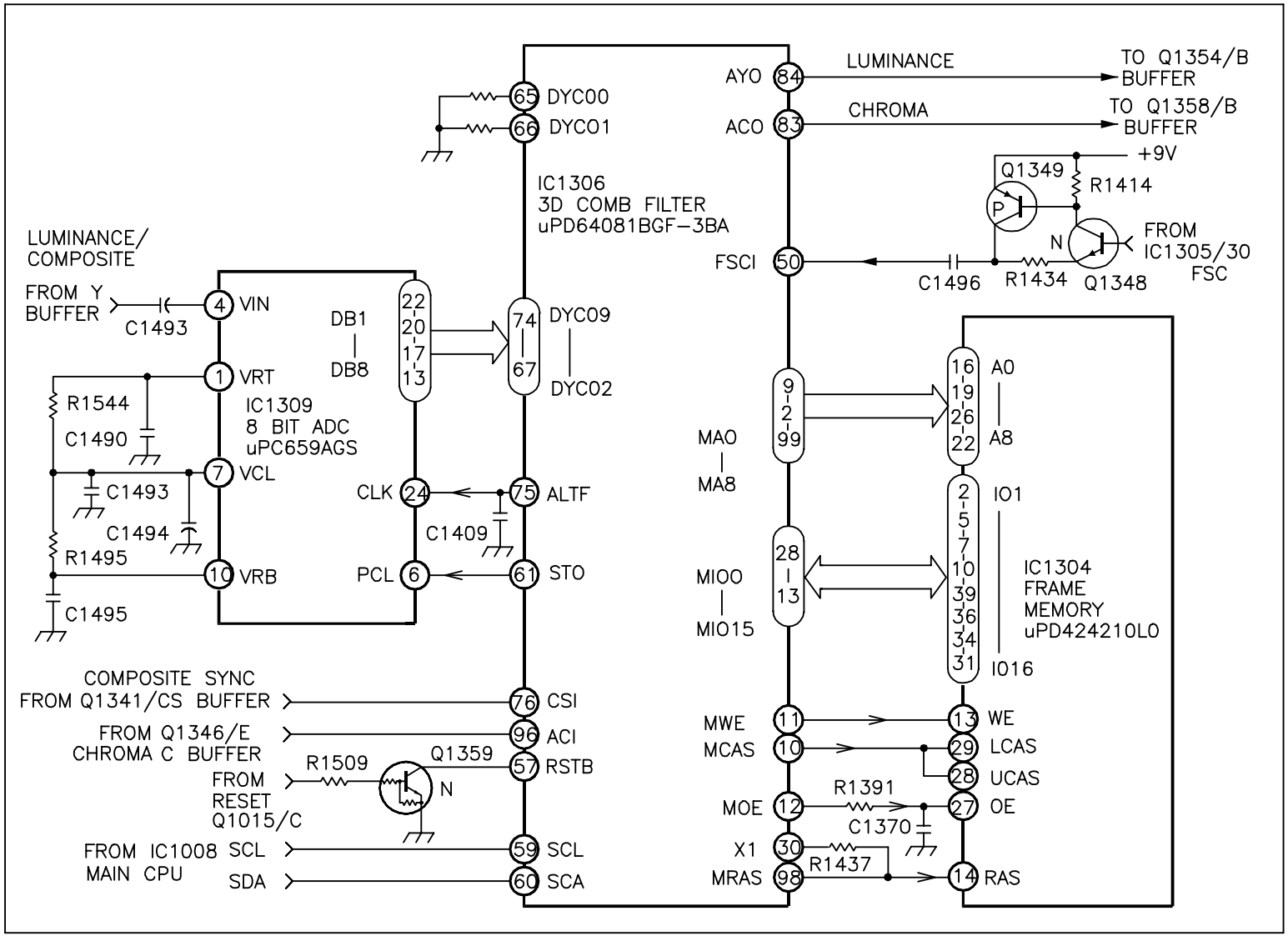
One problem with a full 3D-comb filter system is motion. Motion in the picture between frames can cause some unwanted artifacts. Therefore, the 3D comb filter senses motion in the frames. If no motion is detected, then the line is processed in the 3D process described above. This is referred to as interframe processing. When there is motion in the picture, then the 3D filter reverts back to a 2D filter which uses interline processing. Since many pictures contain both still and moving segments, the 3D-comb filter has the ability to switch back and forth between interframe and interline processing within a frame. The end result is a picture with higher vertical and horizontal resolution, minimized dot crawl and less noise in the video.

Circuit Description

When the set is first powered on, a pulse from Q1359/C resets IC1306 3D Comb Filter. Q1359 inverts the pulse sent by Q1015, the main reset transistor. This resets all the registers and clears memory so processing can begin. Next, using the I²C data from IC1008 Main CPU, IC1306 3D Comb Filter sets the levels of various adjustments. Examples of these adjustments are YNRL and CNRL. They may need to be adjusted as per Service Bulletin 378 located in the back of the book.

IC1309 8-Bit A/D Converter

Before the composite signal is input to IC1306 3D Comb Filter, IC1309 ADC first digitizes it. The composite video signal is input at IC1309/4 from the Y buffer circuit. In addition to the video signal input, IC1309 ADC needs a clock and clamp pulse input. The clock input is a 4fsc (14.28 MHz) sine wave signal, which is sent from IC1309/75 ALTF to IC1309/24 CLK. The clamp pulse is sent from IC1306/61 to IC1309/6 PCL. This signal is at the H rate. The RC network connected to IC1309/1, 7 and 10 is used to set the bias for the clamp circuit. If the DC voltages, other than those that appear below, appear at these pins, the result may be a loss of video. The digital output from IC1309 ADC is output from pins 13 – 17 and 20 – 22 to IC1306 3D Comb Filter.



3D COMB FILTER

TVP08J25 995 12 17 98

IC1306 3D Comb Filter

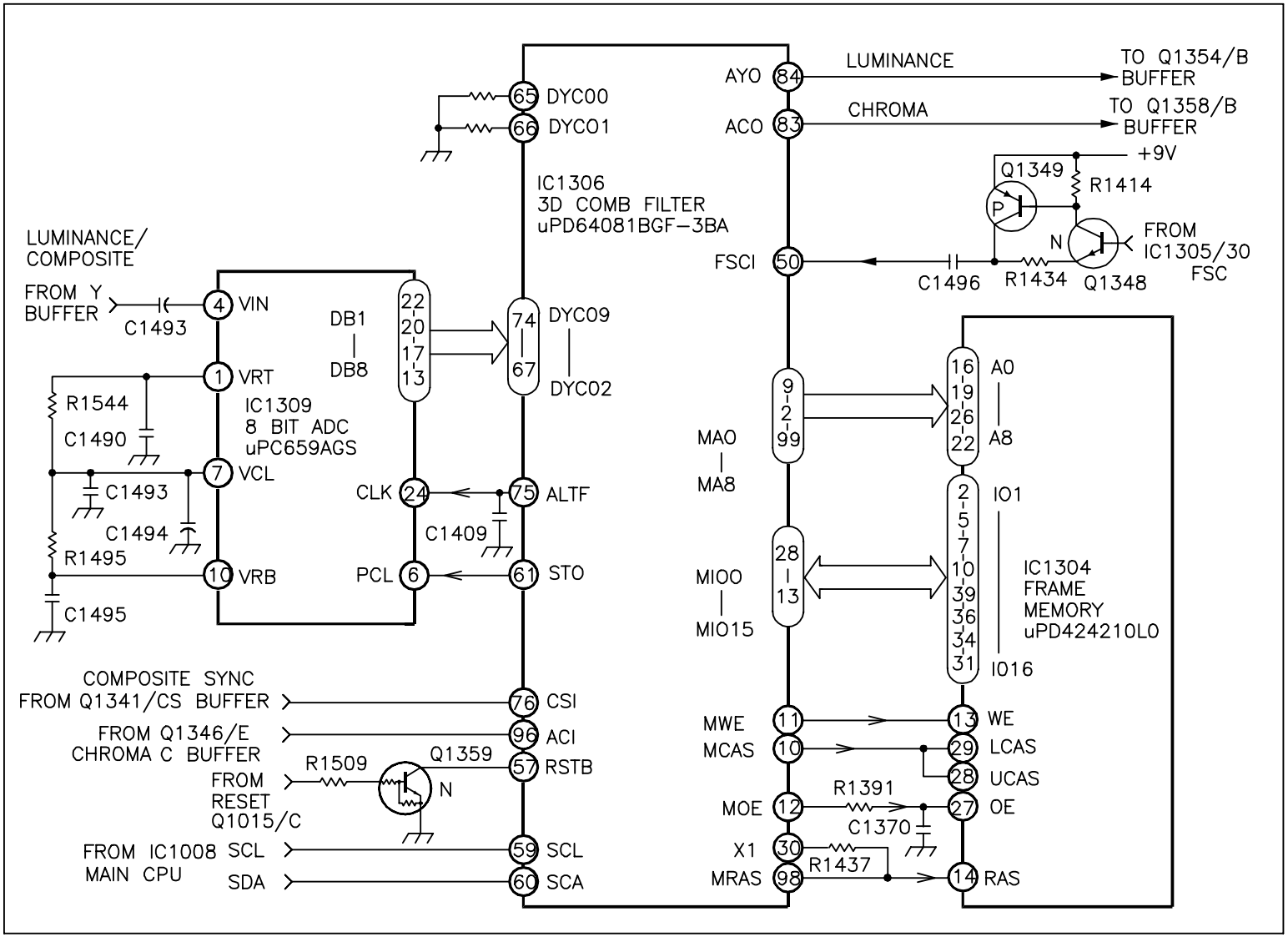
The data from IC1309 ADC is input to IC1306/67-74 DYC02 – DYC09. The DYC00 – 01 inputs are grounded through resistors. Timing is set up for these inputs by IC1306/76 CSI, the composite sync input, and also by IC1306/50 FSCI. The input at IC1306/76 is the composite sync input from the main Y buffer and it controls the timing generator inside of IC1306 3D Comb Filter. IC1306/50 FSCI receives a 3.58 MHz signal, which originates at IC1305/30. This signal controls the system clock internal to IC1306 3D Comb Filter.

Once the data from the digitized video signal is received by IC1306 3D Comb Filter, it is read into IC1306' internal EDO memory controller. The EDO control reads and writes data into and out of IC1304 Frame Memory and also controls the addressing, write enable and refreshing of the frame memory. Data is read in and out between IC1306/13-28 and IC1304/2-5, 7-10, 39-36 and 34-31. Addressing is done between IC1306/9-2 and 99 and IC1304/16-19 and 26-22. The write enable signal is sent from IC1306/1 MWE to IC1304/13 WE. This allows the memory controller inside IC1306 to write data to the locations addressed while WE is LOW. IC1306/12 MOE is the output enable line that allows IC1304 Frame Memory to have data read from it by IC1306 3D Comb Filter. This line is connected to IC1304/27 OE.

IC1304 Frame Memory is four Megs of EDO memory. Since IC1304 Frame Memory is EDO type memory, it needs to be refreshed constantly. This is done using the RAS (Row Address Strobe) and CAS (Column Address Strobe) lines. IC1306/10 MCAS outputs a CAS signal to IC1304/28 and 29 UCAS and LCAS. IC1306/98 MRAS is output to IC1304/14 RAS. These lines keep the memory constantly refreshed and are always active.

The comb filter uses the memory controller for three different purposes. The first is to feed signals that are line delayed by 1H and 2H into the line (2D) comb filter. The second is to feed signals that are line delayed by 1H and 526 H into the frame (3D) comb filter. The third section is the motion detector block that looks at all of the signals and determines if there is motion or not. This circuit is connected to a mixer that outputs either the output from the line comb filter if there is motion, or the output from the frame comb filter if no motion is detected.

After the filtering is complete, the separate Y and C components are input to noise reduction circuits. Noise is subtracted out of the signals and then they are ready to be output. Y is output from IC1306/84 AYO to Q1354/B, which is part of a buffer circuit. The C signal is output from IC1306/83 ACO to Q1358, which is part of a buffer.



TVP08J25 995 12 17 98

3D COMB FILTER

Main Chroma Decoder

Overview

The purpose of IC1305 Main Chroma Decoder is more than just to decode the C signal. It has four purposes: to process the C signal, process the Y signal, generate the H and V sync signals and produce a 3.58 MHz clock for the 3D comb filter and for YUV switching.

C Processing

When the C signal leaves IC1306/83 ACO, it enters a buffer and filter circuit identical to the one used prior to the 3D comb filter. This circuit consists of Q1358, FL1304, Q1356, Q1357 and Q1355. The signal is then sent to IC1305/32 C In. Once the signal enters IC1305 Main Chroma Decoder, it goes through an ACC circuit, chroma amplifier, and a demodulation circuit. The demodulation circuit converts the chroma signal into B-Y and R-Y color difference signals. These signals are then inverted and output from IC1305/19 and 20 as U and V Out. The U signal is buffered by Q1322 and output from its emitter to IC1307/2 Cb In. The V signal is buffered by Q1323 and output from its emitter to IC1307/3 Cr In.

Y Processing

When the Y signal leaves IC1306/84 AYO, it enters a buffer and filter circuit identical to the one that was used prior to the 3D-comb filter. This circuit consists of Q1334, FL1303, Q1350, Q1353 and Q1352. This signal is then sent through two more buffers, Q1367 and Q1366, before being input to IC1307/28 CV-Y. This signal is switched through IC1307 Main YUV Switch and the Y signal exits at IC1307/22 Sel Y. The input for this switching circuit is controlled by Q1343, which is part of the 3.58 MHz clock section. There will be more on this later in this section.

The signal from IC1307/22 Sel Y is split and sent to two buffers. One of these buffers, Q1328, is the Y buffer. The other buffer feeds the sync separator circuits. The Y signal enters IC1305/34 Y In for processing by IC1305 Main Chroma Decoder. Inside the IC the Y circuit goes through sub-contrast, sharpness, clamp and auto-pedestal circuits. These circuits are adjusted with data from the I²C circuit. The Y circuit is then output at IC1305/18 Y Out. The Y out signal is buffered by Q1321 and outputs its emitter to IC1307/1.

H and V Sync

When the Y signal leaves IC1307/22 Sel Y, it is sent to Q1330 to be buffered. This signal leaves Q1330/E to Q1331/B and Q1332/B. Q1331, along with C1381, passes the Y signal. It causes some roll off of the H sync pulse. This signal is then input to IC1305/38 V Sync. Q1332, along with C1389 and C1385, passes the Y signal and rolls off some of the V sync pulse. This signal is sent to IC1305/39 H Sync. These signals are used to sync the H and V oscillators to the incoming video.

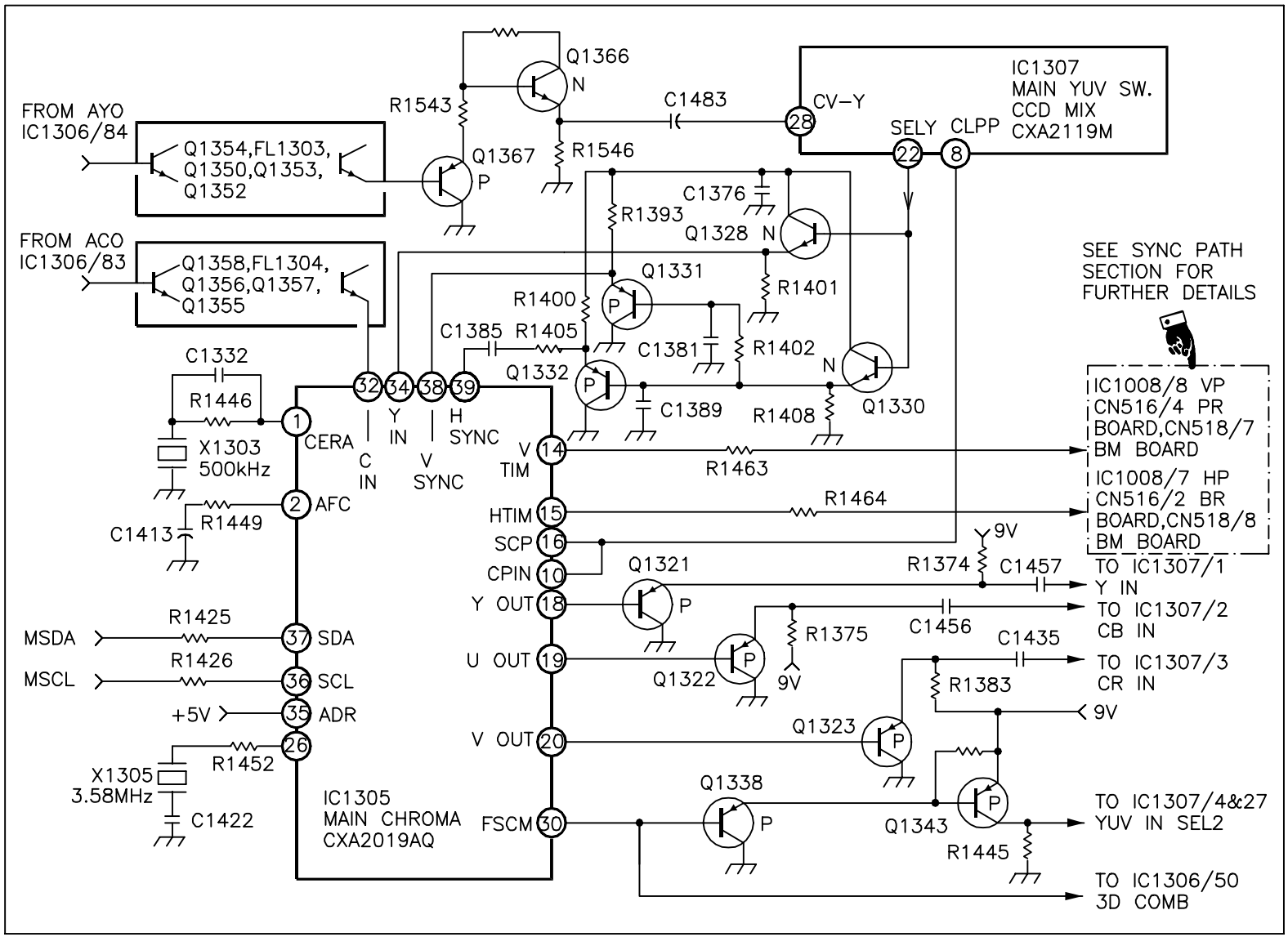
The Y signal that is input at IC1305/39 has the horizontal sync signal stripped off of it and applied to the internal phase detector. This signal is compared with a signal from X1303, which is input to IC1305/1. R1449 and C1413 filter the output of the phase detector. These components are connected to IC1305/2 AFC. The voltage at this pin keeps the oscillator phase locked to the sync signal. The internal divide by circuit is used to produce the Htim, which is output at IC1305/15.

The Y signal that is input at IC1305/38 has the vertical sync signal stripped off of it. This is done with the help of R1433 and C1400, which form a peak hold circuit and are connected to IC1305/40 V Hold. This signal is input to a countdown circuit to produce the Vtim signal, which outputs at IC1305/14.

The Vtim and Htim signals are combined and output at IC1305/16 SCP (Sand Castle Pulse). The clamp circuits in IC1305 Main Chroma Decoder and IC1307 YUV Switch use this signal.

3.58 MHz Clock

A 3.58 Mhz crystal is connected at IC1305/26 XNTSC. This input is used to create the chroma oscillator and will be output at IC1305/30 if a video signal is input. This output is used by the 3D-comb filter and also by Q1338 and Q1343. These transistors produce a HIGH output, which is used to select input 1 on IC1307 Main YUV Switch. When the Video 5 component input is used, this circuit produces a LOW and input 2 is selected at IC1307 Main YUV Switch. A LOW is output because there would be no video input to IC1305.



MAIN CHROMA

TVP8J26A 1004 12 2 98

Main YUV Switch

Overview

The purpose of IC1307 YUV Switch is to switch the appropriate YUV signal from IC1305 Main Chroma Decoder or the Video 5 component input. It is also used to matrix the Closed Caption Data (CCD) into the selected YUV signals. In addition there is a corresponding Y input that is switched to a Y output for Closed Captioning and main Y processing.

Inputs

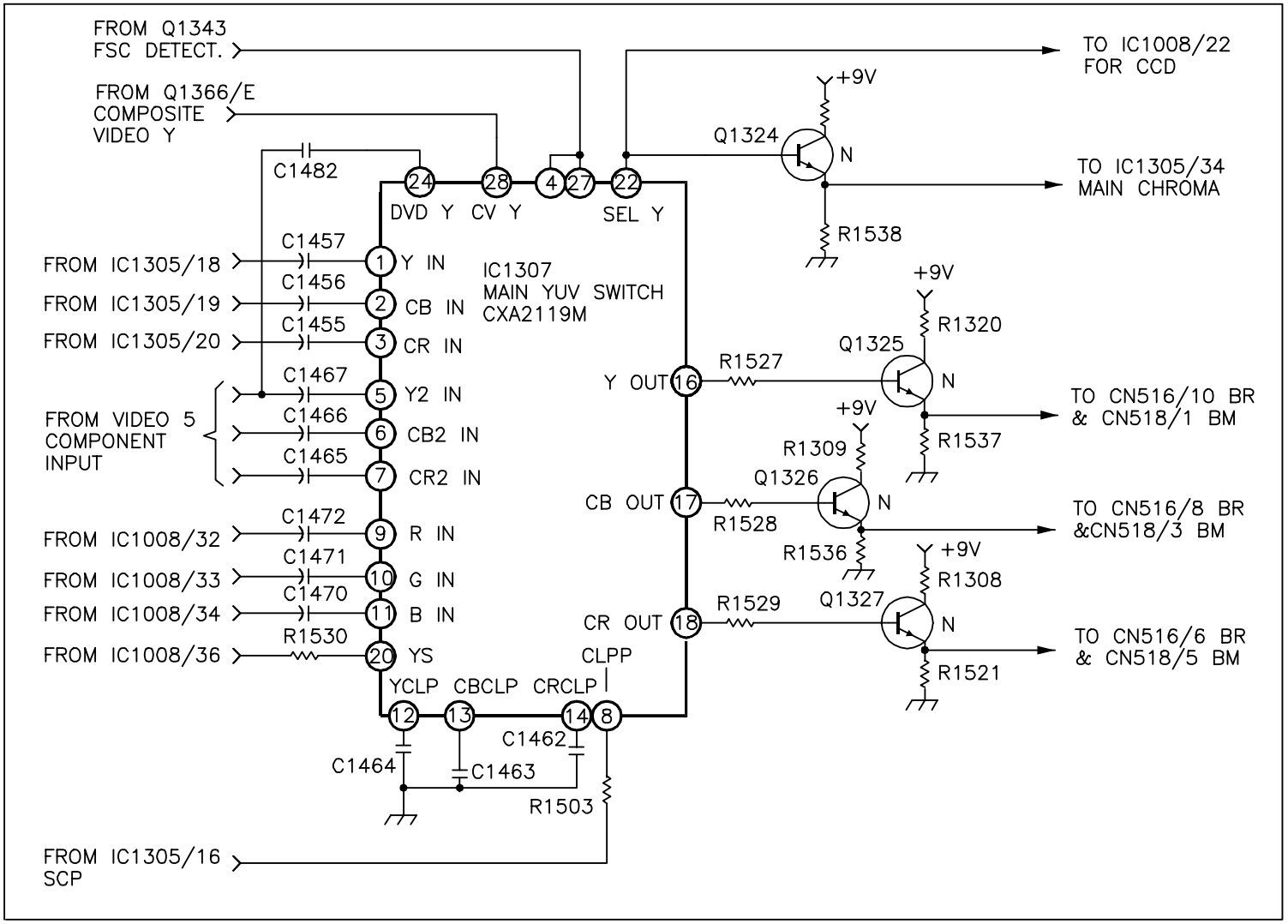
There are two main sets of inputs to IC1307 YUV Switch, along with inputs for the CCD information. The first set is comprised of the Y signal from the IC1306 3D Comb Filter which is input to IC1307/28 CV Y, and the Y, U and V signals from IC1305 Main Chroma Decoder which are input to IC1307/1, 2 and 3. The other set of inputs consist of the DVD Y signal which comes from the Video 5 component input and enters IC1307/24 DVD Y, and the Y, U and V component video from the Video 5 component input which enters IC1307/5, 6 and 7.

The CCD RGB and YM/YS signals are also input to IC1307/9, 10, 11 and 12. These signals will be matrixed onto whichever YUV signal is output. It will differ depending on which input is selected. Which inputs are switched to the outputs depends on the state of IC1307/4 and 27.

Output Selection

The select pins at IC1307/4 and 27 are tied together and receive their input from Q1343 which outputs a HIGH or a LOW depending on the state of the FSC signal from IC1305 Main Chroma Decoder. If any of the inputs except Video 5 component input are selected, IC1307/4 and 27 will be HIGH. This enables the first set of inputs to IC1307 YUV Switch and the CCD RGB that goes with it. The YUV signals are output from IC1307/16, 17 and 18. Q1325, Q1326 and Q1327 buffer these signals before they are sent to the BM and BR boards. It will also send the CV Y signal input at IC1307/28 out at IC1307/22 Sel Y for processing by IC1305 Chroma Decoder, and IC1008 Main CPU for CCD processing.

If the Video 5 component input is used, IC1307/4 and 27 will be LOW. This enables the second set of inputs, along with the CCD RGB that accompanies it. The YUV signals are output from IC1307/16, 17 and 18. Q1325, Q1326 and Q1327 buffer these signals before they are sent to the BM and BR boards. It will also send the DVD Y signal input at IC1307/24 out at IC1307/22 Sel Y for processing by IC1305 Chroma Decoder, and for CCD processing by IC1008 Main CPU.



MAIN YUV SWITCH AND CCD MIX

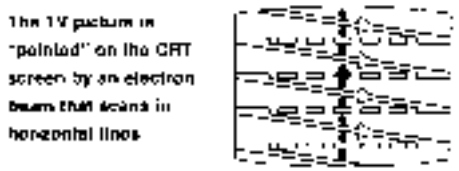
TVP08J27 1018 12 17 98

DRC - Digital Reality Creation

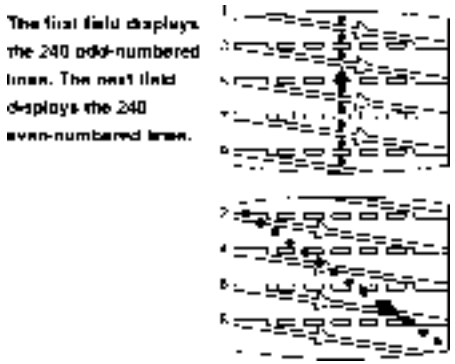
Another picture quality issue has been with us since the dawn of television. Deeply ingrained in our television system is the question of visible scanning lines.

All about scanning lines

A television picture is “painted” across the CRT screen by an electron beam that scans on a horizontal line from left to right. Once the beam reaches the ridge edge, it shuts off and returns to the left edge to start another line. All told, there are some 525 scanning lines in the American NTSC (National Television Standards Committee) television system, and they create a new television picture or “frame” some 30 times a second.



In reality, you don’t see the full 525 lines on the screen. Over 40 lines are consumed by the Vertical Blanking interval. This leaves roughly 480 lines for the actual picture. And you don’t even see the 480 lines all at once. Each video frame is divided into two “fields”, which last for 1/60th of a second. The first field is composed of all the odd-numbered lines (1, 3, 5 and so on). The second field “fills in” with the even-numbered lines. This technique of alternating odd and even fields is called “interlacing.” The NTSC system is often referred to as “525/60” (for 525 total scanning lines and 60 fields per second). It is also called “480I” (for 480 net scanning lines, interlaced).



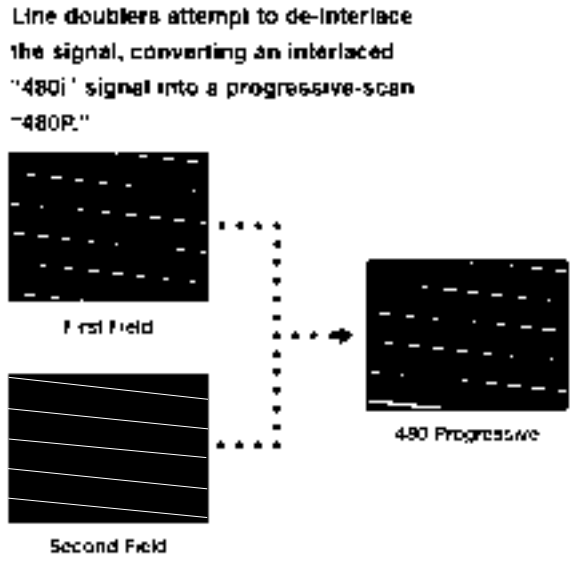
Over the years, the 480i system has worked remarkably well. But with only 240 lines on-screen at any one time, the scanning lines can become painfully obvious, particularly when you’re sitting close to a large-screen display.

Problem: Visual scanning lines

Originally, television engineers designed the NTSC system so that the picture would appear seamless when viewed from a distance of 8 times the picture height. This worked well in an era when the biggest commercially available screens were 12 inches diagonal. But in today’s big-screen era, viewers tend to set far closer to their televisions in order to get wrapped up in the action. Under these conditions, the scanning lines become blatantly visible.

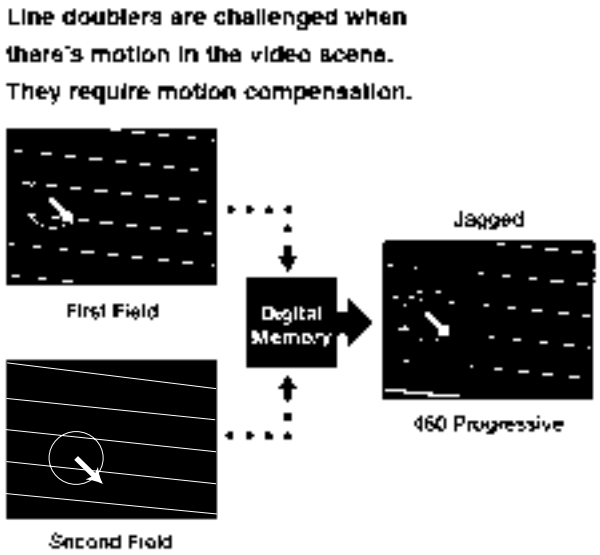
One solution: Line doublers

Demanding home theater enthusiasts, videophiles and video professionals have long sought a cure for this problem. One solution is to double the number of scanning lines with a circuit called a line doubler. Sony has been an active supplier of line doublers, particularly for professional video projectors.



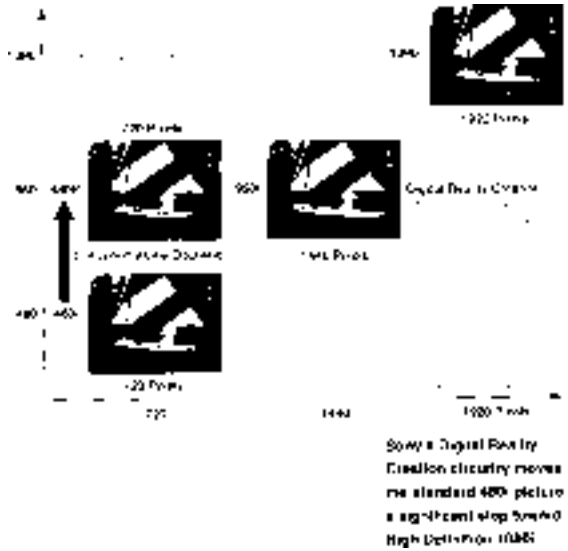
Many line doublers attempt to de-interlace the 480i NTSC signal, displaying both fields simultaneously in a 480-line “progressive” scan. Progressive scanning combines the separate fields of odd-numbered lines and even-numbered lines. Progressive scanning displays every line in a frame in numeric sequence – line 1, 2, 3, 4 and so on up to line 480. Progressive scan plays a central role in computer displays – where it helps to make text more legible. Line doublers turn interlaced 480i signals into a progressive 480P.

This concept works perfectly for still images, because the two fields match up completely. But on moving images, the even field is captured 1/60th second *later* than the odd field. So a car traveling on the screen has driven 1/60th second further down the street. And a baseball has slid 1/60th second closer to home plate. For this reason, line-doublers require elaborate motion-detection, motion-compensation and memory circuits. This can get expensive, with the better line doublers costing $2,500 or more.



A new solution: DRC

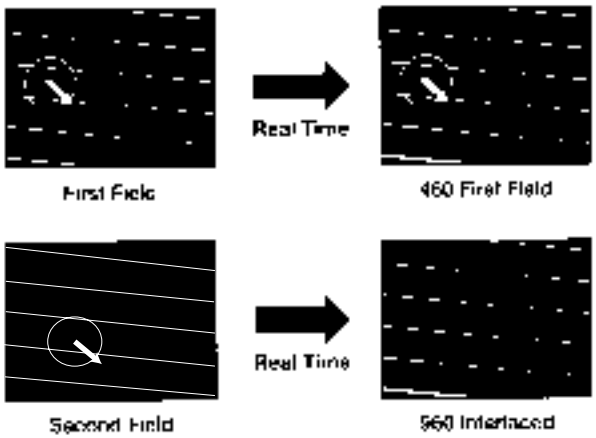
Sony’s new Digital Reality Creation (DRC) circuitry is an all-new approach to the problem of visible scanning lines. Not only does DRC create a clearer picture by doubling the number of active scanning lines – *it also doubles the number of pixels on each scanning line.* You get four times the picture density of standard 480i, making this a significant step toward the picture quality of true High Definition TV (HDTV).



How it works

The new DRC circuit is based upon a massive analysis of over tens of thousands of High Definition TV picture patterns. Because there is a fixed relationship between NTSC patterns and their HDTV equivalents, Sony’s exclusive microprocessor can simply *replace* the NTSC signal with its correct DRC counterpart. In operation, the DRC circuit accepts a digitally sampled 13.5 M H z input and generates a quadrupled 54.0 MHz digital output.

Moreover, with DRC, each field is processed separately, so there's never a need to compensate for motion between two fields. And while the doublers typically produce a scan of 480P, the DRC circuit produces a higher line rate, 960i, for even greater image density.

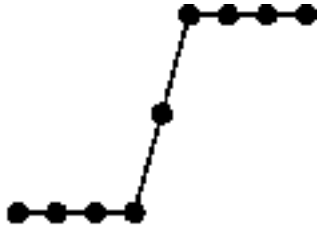


Line doubling (left) requires memory to avoid artifacts on moving objects. Digital Reality Creation circuitry (right) maintains the integrity of each video field.

What it all means

Digital Reality Creation circuitry greatly enhances the television viewing experience. Now you can sit up close to the screen, immersing yourself in the magic of home entertainment – and still not be bothered by visible scanning lines. Pictures appear denser and more seamless. And in the coming world of Digital TV (DTV) broadcasting, televisions with Digital Realty Creation circuitry will narrow the perceived gap among NTSC analog sources, standard definition digital and full High Definition digital video.

Line doubling improves vertical density



DRC doubles both vertical and horizontal density

NOTES

DRC Block

Overview

The DRC Block located on the BR board is a line doubling and pattern recognition system used to quadruple the number of pixels displayed on the screen. It changes the standard 480I signal to a 960I format. This means that our horizontal scan rate is now doubled to 31.5KHz.

Inputs

The BR board which contains all the DRC circuitry is a daughter board that plugs into the A board. All video to be displayed as the main picture is routed through BR board. This circuit cannot be disabled. The only time the video is not derived from the BR board is when a Twin-View feature such as Channel Index or Picture and Picture is used.

The BR board receives three component video signals. The M-Y, M-B-Y and M-R-Y signals enter the board at CN302/10, 8 and 6, respectively. These signals are also referred to as Y, U and V. Two other inputs are necessary; they are vertical and horizontal sync. They enter CN302/4 and 2 as M-VD and M-HD. The HD signal is used to phase sync a 13.5MHz clock using IC466 Sync Shift and IC303 13.5 MHz Clock. This signal is used to clock IC306 3 Channel 8-Bit ADC and IC305 TBC.

The component video signals are input to IC306 3 Channel 8-Bit ADC. This IC outputs 8 bits of Y and 8 bits of C information. These outputs are input to IC305 TBC. This IC is a Time Base Corrector that removes any jitter present in the signals. This IC outputs 8 bits of Y and 8 bits of C information. It also outputs a sync signal that is used to phase lock IC301 54 MHz Clock.

DRC Processing

The 8 bits of Y and 8 bits of C are applied to IC462 Up Converter. The Y signal is also applied to IC644 Memory. This IC transfers data between IC645 Memory and IC462 Up Converter. IC462 breaks the data into several data streams and outputs them into IC463 Up Converter. Two clocks, 13.5MHz and a 27 MHz, sync this IC. IC463 processes these data streams and outputs two sets of Y and C data. These data streams are input to IC304 Up Converter along with 54 and 27 MHz clocks. The processing done by IC462, IC463 and IC304 converts the video signals from normal NTSC to a near HDTV-like equivalent.

Outputs

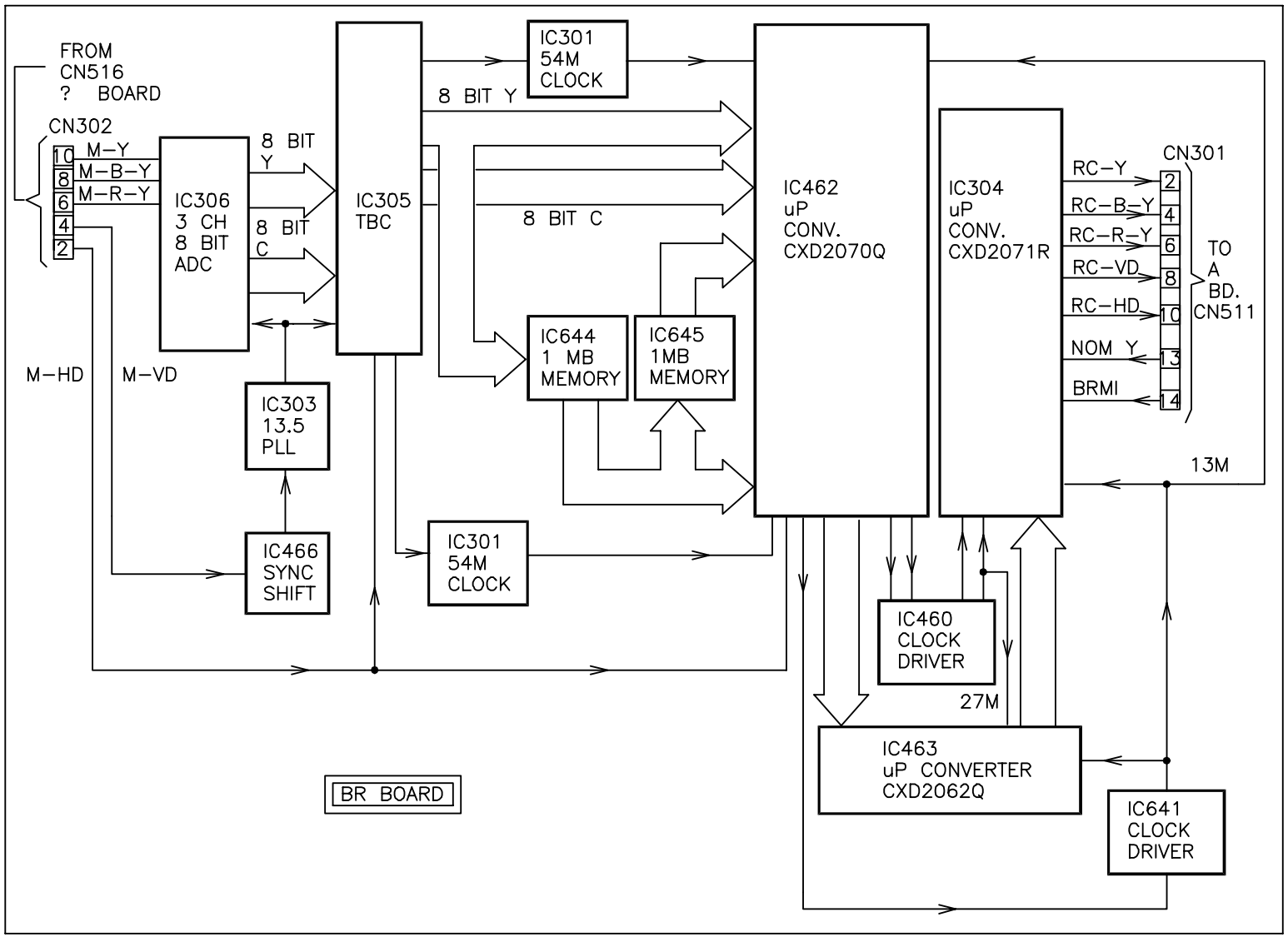
IC304 Up Converter outputs three component signals to CN301. These signals are output from CN301/2, 4 and 6 as RC-Y, RC-B-Y and RC-R-Y. This IC also outputs a RC-VD signal at CN301/8 and a RC-HD signal at CN301/10. The RC-HD signal is a 31.5KHz horizontal sync signal.

There are also two inputs at CN301/13 and 14 called NomY and BRMI. This signals are inputs that control the amount of vertical enhancement in the signal. This is controlled using the DRC Mode selections in the customer video menu. The table below shows the voltages at these pins for each DRC Mode.

DRC Mode	BRMI	NomY
High	0 Volts	0 Volts
Low	5 Volts	0 Volts
Game	5 Volts	5 Volts

Troubleshooting

At this time troubleshooting of the BR board should be limited to resoldering and board replacement. Troubleshooting is nearly impossible because of the lack of extender cables. DRC problems typically result in a solarized or blocky picture in the main picture. If your picture is distorted, switch the set to the Picture and Picture mode. If you problem clears up then you should replace the BR board.



DRC (DIGITAL REALITY CREATION)

TVP08J81 1041 12 21 98

MID - Multi Image Driver

The world of NTSC has been a simple world. The 480i video cameras give their signals to 480i video recorders, 480i production switchers, 480i broadcasting, 480i videocassettes, 480i videodiscs and ultimately 480i home television receivers. This world is comfortable and compatible, but it's already rapidly changing.

A blossoming range of image standards

Unlike entertainment-oriented television, computers have long used progressive scanning to maximize the legibility of on-screen text. For example, the popular VGA computer standard uses progressive scanning 640 h x 480 V pixels. In video terms, that's 480P.

Digital Television (DTV) broadcasting embraces both interlace scanning and progressive scanning. A convergence technology is needed to link the two previously separate worlds of entertainment and information.

Sony's solution

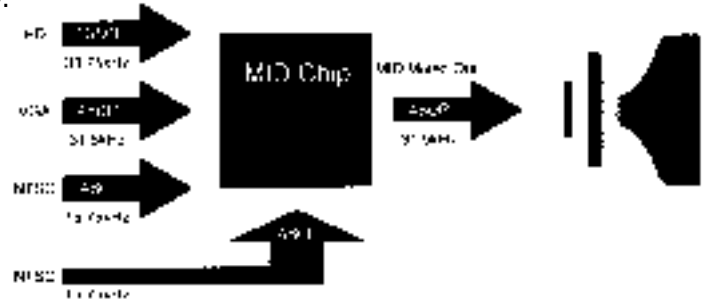
Sony's new Multi-Image Driver (MID) circuitry contains a special "Twin-View" function that can display either a High Definition or a Standard Definition video signal together with any VGA source. This is a proprietary integrated circuit based on company expertise in broadcast-quality Digital Multi Effects systems. Some (but not all) Sony televisions with MID will enable viewers to combine two different signal formats on the same screen.

MID works by converting both signals to VGA (480P) display. Supported signal combinations include:

- NTSC + NTSC
- NTSC + HD
- VGA + NTSC
- VGA + HD

MID circuitry can mix High Definition video with computer VGA images or HD and NTSC

In the digital future, the unique capabilities of the Multi-Image Driver circuitry will open up unprecedented applications. You'll use Picture-in-Picture with High Definition, standard definition and NTSC sources. You'll be able to watch a movie in High Definition, while you visit a website to learn more about how that movie was produced. And you'll be able to see both images with exceptional quality and highly advanced Picture-in-Picture functionality.



Sony's Multi-image Driver bridges the gap between computing and television. You can surf the net at VGA resolution while you watch High Definition TV on the same screen.

A new generation of PIP functionality

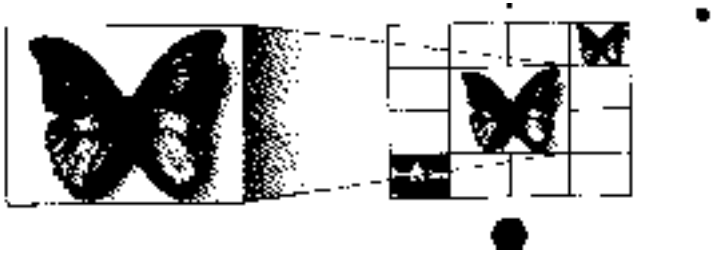
Multi-Image Driver circuitry also delivers powerful picture-in picture advantages, such as:

- **Flexible Twin-View™ Function.** Not only can you view two images side-by-side, but you can continuously expand either picture, up to two times its normal size.

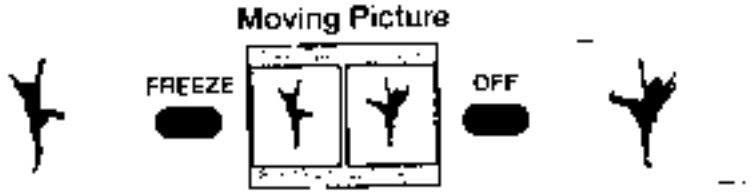
- **Free-layout Picture-in-Picture.** Instead of simply moving the PIP to pre-determined spots, you can use the remote joystick to manipulate it, placing it *anywhere* on the screen.

- **Advanced Channel Index.** MID also supports the ability to preview up to 13 channels simultaneously (12 inset still pictures plus one main picture in full motion).

- **New Favorite Channel.** Automatically shows your eight favorites or the last eight channels you've watched.



- **New Freeze Mode.** Lets you freeze a broadcast screen to write down a telephone number or website URL while the program continues as a side-by-side TwinView picture.



NOTES

MID Block

Overview

A MID (Multi-Image Driver) is used in the RA-4 chassis for PIP and Twin-View operations. This technology allows two images of any format to be displayed at the same time in a 480 P format in separate windows. All of the MID circuitry in this chassis is located on the BM board. Since there are no extender cables available at this time, repair of the MID circuit will consist of resoldering or replacing the BM board.

Mid Inputs

The BM board receives Y, U and V inputs from the main video and the sub video. These two sets of inputs are each applied to their own ADC. IC003 and IC014 are identical 8-bit three channel analog to digital converters. Their digital outputs are input to IC010 MID controller.

The BM board receives sync from the main and sub sync signals. These signals are main VS and HS and Sub VS and HS. The V signals are 60 Hz and the H signals are 15.734 KHz. The BM board also receives sync inputs from the VS and HS signals. VS and HS signals are output from IC511 Video Processor (not shown) and are used as the synchronizing signals for the deflection circuits. The VS signal is a 60 Hz signal, while the HS signal is a 31.5 Khz signal. These signals are needed to synchronize the input and output video signals.

MID Processing

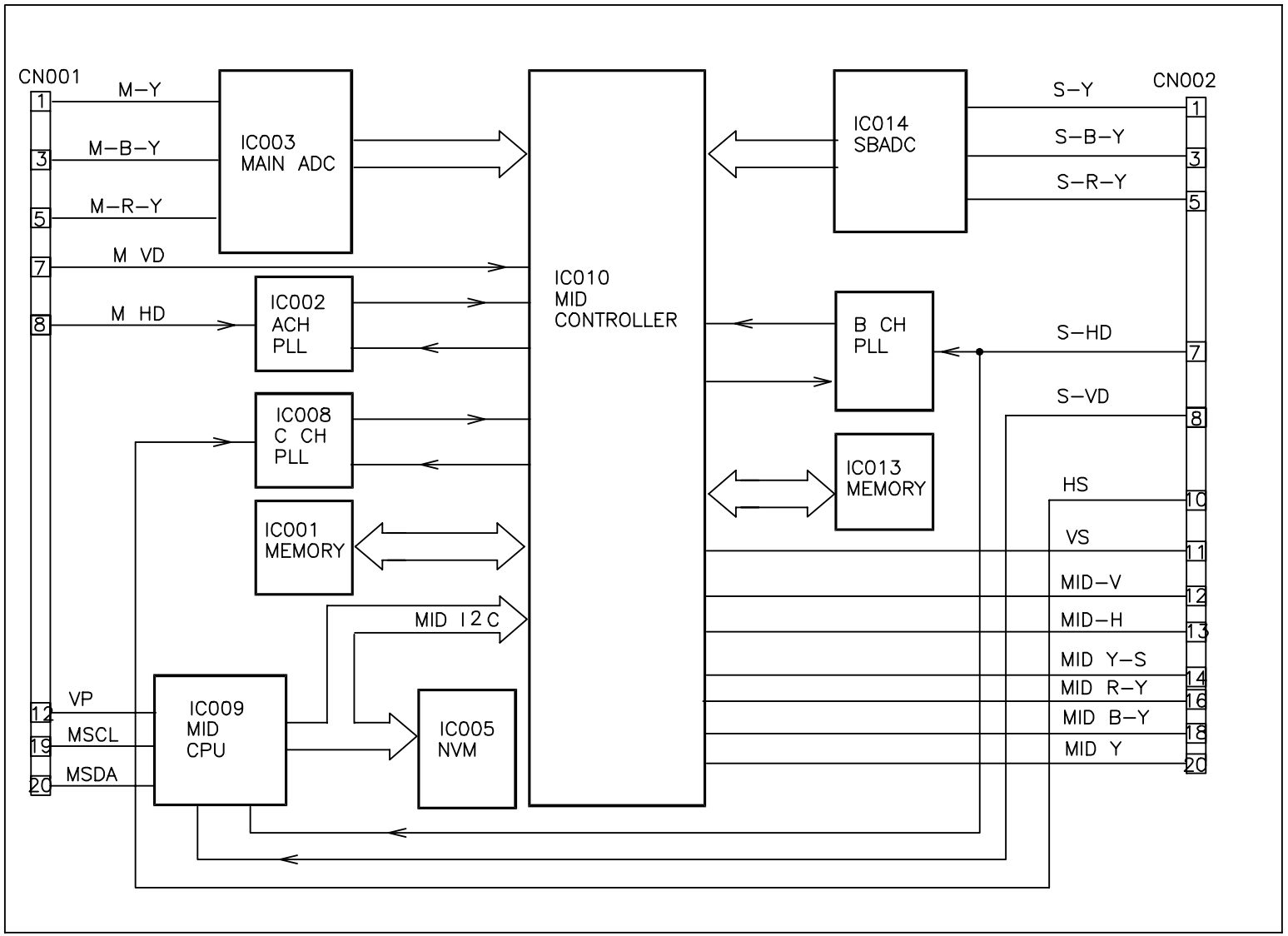
When the customer uses the remote to enable PIP or Twin View functions, data is sent over the I2C bus for the MID CPU. The MID CPU interprets these instructions and commands the MID Controller to produce the proper output. The video output uses the two memory ICs to manipulate the signals to produce the desired outputs. The MID CPU also uses the NVM to store the settings of its parameters. These includes picture modes, size of pictures, number of pictures, etc.

MID Outputs

Once the processing of the signal is complete, Y, U and V signals are output from the MID processor along with a MID YS signal. This signal is used for positioning of the MID video signals into the picture. MID VS and HS signals are also output from the MID Controller. These signals are used as sync signals for the MID video. The VS signal is a 60 Hz signal and the HS signal is 31.5 KHz.

MID Troubleshooting

MID malfunction will only cause problems with the PIP or Twin-View functions. Some symptoms could be loss of PIP window or distorted PIP picture. If the BM board is not producing vertical sync and a Twin-View function is activated, the set will shut down and indicate a vertical failure or produce a cycling power relay. If an antenna or video source is being input, the symptom would be a cycling power relay (relay turning ON and OFF every few seconds). If no antenna or video source were input, then the Self-Diagnostics would indicate a video failure. At the present time any MID failure requires the BM board to be replaced.



MID BLOCK

TVP08J37 1031 12 16 98

Video Processor

Overview

The purpose of IC511 Video Processor is to combine all of the signals that need to be displayed and output them to the C boards as R, G and B signals. In addition, it outputs the sync signals for the deflection circuits, outputs the Velocity Modulation signal and controls the Automatic Cathode Bias, which is responsible for IK blanking.

Video Processing

Video Inputs

Four different sets of video signals are input to IC511 Video Processor. Two that can be used for the main video are the Y, U and V signals output from the DRC and MID boards. The MID signals are output from MID board to CN513/20, 19 and 18 into IC511/64, 63 and 62. The DRC signals are output from the DRC board to CN511/2, 4 and 6 into IC511/69, 68 and 67. In addition to these signals a YM/YS signal is output from the MID board to CN513/15, and then input to an OR circuit consisting of Q530 and Q546. The other input to the OR circuit comes from IC1008/61 O Sync Sel. The output from this OR circuit is input to IC511/61 TCACR SW. The signal that enters this pin determines how much of the MID or DRC signals will be used for the main picture. When a normal picture is being shown, then all of the picture will come from the DRC signal. When PIP is displayed, the main picture will be supplied by DRC and the child picture will be the MID signal. When features such as Channel Index and Twin View are used, then the entire picture will be from the MID signal.

The other two inputs are from the Auto Registration's OSD circuit (BD board) and IC1004 OSD Processor. The BD board outputs signals to CN522/6, 7, 8 and 9 which are input to IC511/45, 46, 47 and 48. These signals are YM/YS and RGB type signals and are used when the customer uses the Auto-Focus button on the front panel. They are also used in the service mode to output the OSD for the PJED section and the dot or crosshatch patterns used for adjusting. The other signals are output from IC1004 OSD to four buffers. These buffers are Q1012, Q1002, Q1001 and Q1003. The outputs are taken from their emitters and input to IC511/49, 50, 51 and 52. These signals are the YM/YS and RGB signals for the OSD.

Video Outputs

The video signals that are input are combined to form a picture that is output as R, G and B signals from IC511/35, 37 and 39. These signals are sent through buffers to CN701, which is connected to the CR board. They are then sent to their respective C boards where they are amplified and applied to the cathode of the picture tubes.

IC511/59 VM Out outputs a velocity modulation signal that is applied to the Z boards for each color. This signal is used to speed up and slow down the CRT beams as they scan horizontally across the face of the tubes. This enhances the transitions between light and dark images, consequently increasing the resolution of the picture.

IK

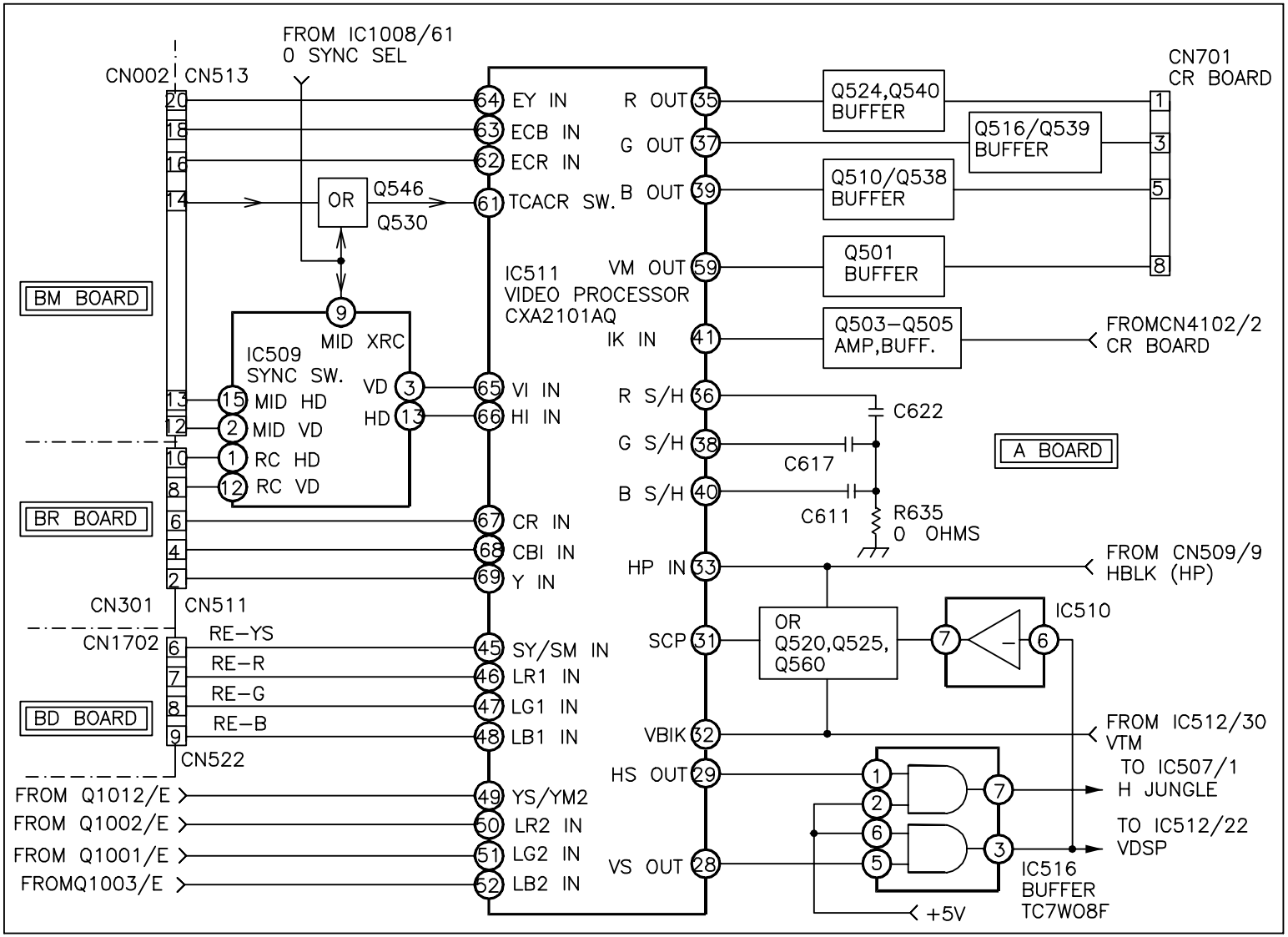
IK pulses are output along with the video signals from the R, G and B outputs. These pulses are returned from the C boards and input to IC511/41 IK In. A window comparator inside IC511 Video Processor monitors these pulses. This window comparator has a sample and hold circuit for each color. The sample and hold voltage can be monitored at IC511/36 for red, IC511/38 for green and IC511/40 for blue. If the voltage for any of these three falls outside of a certain window, the picture will be blanked and the Timer LED will flash five times as part of the self-diagnostic function.

Sync Processing

There are separate sync signals output by the MID and DRC circuits that are input to IC509 Sync Switch. The MID HD signal is input to IC509/15 and the MID VD signal is input to IC509/2. The DRC HD signals are input to IC509/1 and the DRC VD is input to IC509/12. These signals are switched by the signal at IC509/9. The VD signal is output at IC509/3 and input to IC511/65. The HD signal is output from IC509/13 and input to IC511/66.

These signals are output from IC511 Video Processor as HS Out and VS Out at pins 29 and 28 respectively. They are sent to IC516 Sync Buffer before being sent to their respective deflection circuits.

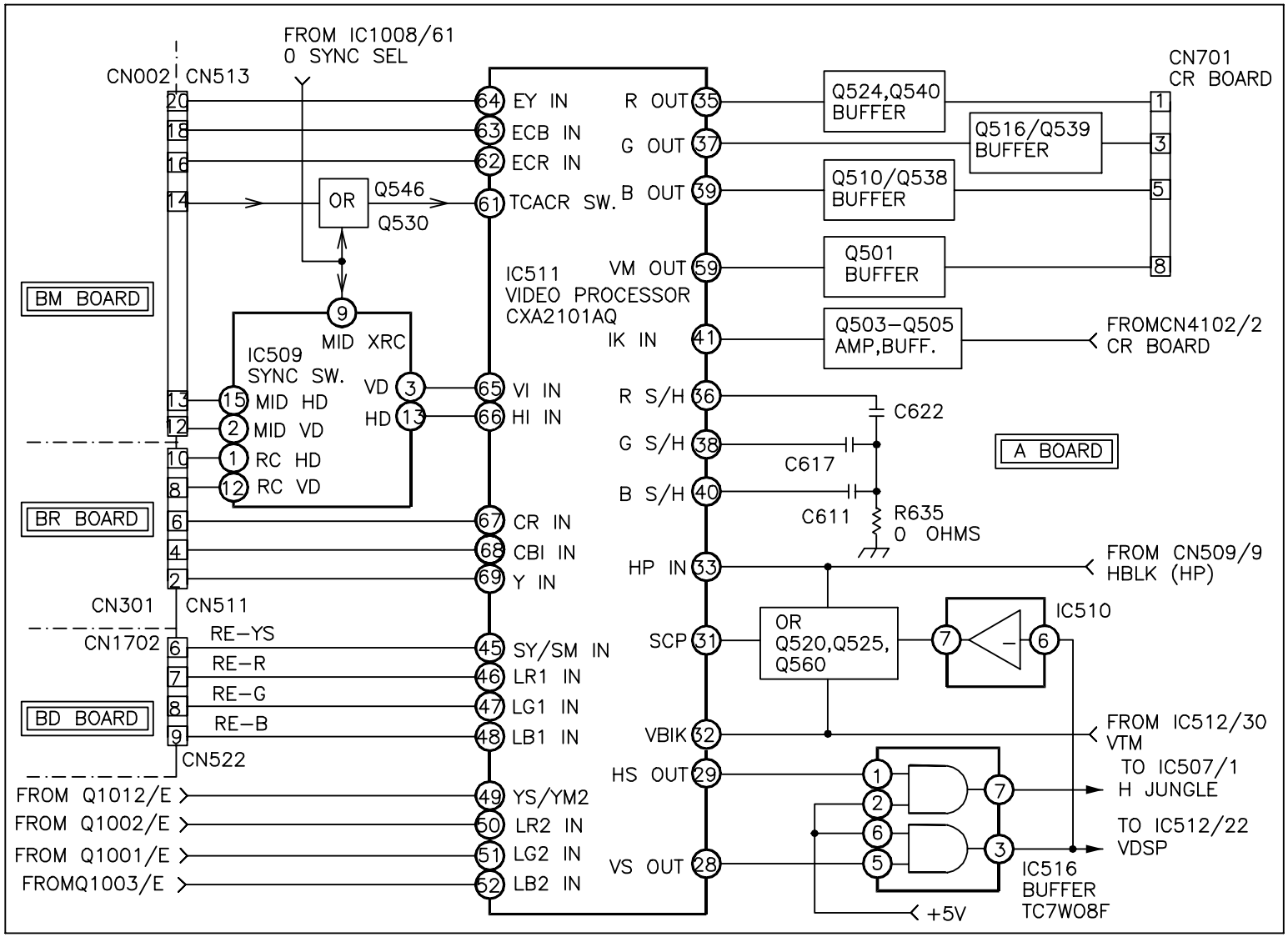
The return signals from the deflection circuits, HBLK and VBLK, are input



VIDEO PROCESSOR

TVP08J45 1029 12 18 98

to IC511/33 HP In and IC511/32 VBLK. These signals are used to phase lock the sync of the deflection circuits output to the output of the sync signals from IC511 Video Processor. In addition to this, the HBLK signal is applied to an OR circuit, along with the VBLK and HS Out signals to the SCP pulse. The SCP is called the sand castle pulse because of its shape. The SCP pulse input to IC511/31 is used to time the clamping of the video signal.



VIDEO PROCESSOR

TVP08J45 1029 12 18 98

IK/AKB

Overview

When troubleshooting a blanking problem, you must first understand the video drive and IK blanking circuit and how they interrelate. Second, by applying the troubleshooting techniques in this book you can determine if blanking is caused by the video drive circuit or the IK.

Video Drive

The RGB video signals exit IC511 Video Processor at pins 35, 37 and 39. The RGB signals pass through buffers and enter the CR board at CN7101. The G and B signals are sent to their respective C boards. Each of these signals are input to their respective Video Out IC, then amplified and output to the cathode of their tube.

IK

The purpose of the AKB or IK circuit is to keep the picture's white balance correct by controlling the bias or input level at the picture tubes cathode.

When serial data is present at the IC511 Video Processor, the IK circuit begins operation. Three pulses are output during vertical blanking, one at each of the RGB outputs. These pulses turn the tubes fully on. The beam current is sensed at pin 5 of each Video Out and applied to the IK buffer. This signal is sent to IC511/41 IK In, which is the reference return for the loop. The RGB output voltage levels are determined by this input.

If the voltages of the pulses returned are not within a certain window, the video signal will be blanked. Internally these three pulses are applied to their own sample and hold circuit. They all contain an external capacitor, which is connected to pins 36, 38 and 40 respectively. The voltage at these pins corresponds to the efficiency of each cathode. The more current drawn, the **lower the voltage output at the sample and hold capacitors. This differs from previous models.**

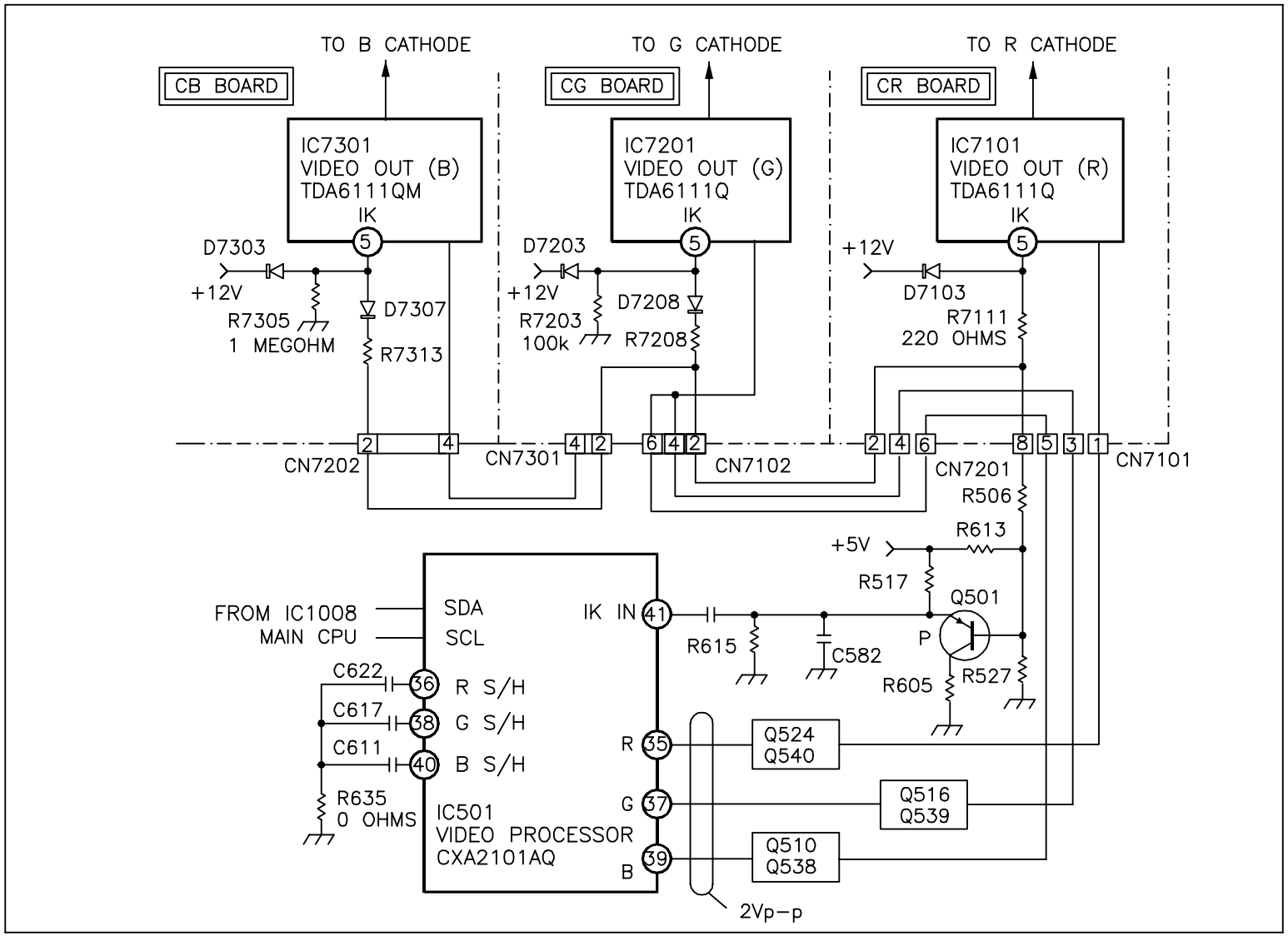
When a normally working set is first turned ON, the Timer LED blinks for approximately 8 to 10 seconds. This is because IC511 Video Processor is holding the data bus in a busy state. When the voltages at IC511/36, 38 and 40 are between 2.5 and 6 volts, the IC511 Video Processor will signal the micro that it is no longer in a busy state and unblank the set. When IC511 unblanks the video, it outputs RGB of approximately 2 Vp-p from pins 35, 37 and 39. If there is a problem, the Timer LED will flash five times in accordance with the Self-Diagnostic function. As an example, if the red tube were drawing no current, IC7101/5 would fall to about 2 volts. This would cause the voltage at IC511/36 to rise to around 6.5 volts. These voltages are indications that the red tube is not drawing enough current.

Troubleshooting

The first thing that must be determined is if the problem is with the video drive or the IK return. There are several ways to determine if the IK pulse is driving the tube. The quickest way is to take a mirror and place it at about a 45-degree angle above and behind the tube and look for a bright horizontal line at the bottom of the tube (this would be at the top of the mirror). Remember the IK pulse is done during vertical blanking, so although it cannot be seen on the screen, it can be seen in the tube. If one of the lines is missing or is significantly dimmer than the other two, that color has the problem. Check the color's output from the Video Processor to decide if it or the video drive circuit is at fault. If the video drive circuit is at fault, the IK pulse can be followed to signal trace the circuit.

If all three lines can be seen, then you can check the sample and hold voltages at IC301/19, 21 and 23 to see if the IK pulses are being returned. These voltages are normally around 4 Vdc, but any voltage between 2.5 and 6 volts should not cause blanking. If all three lines are seen and the S/H voltages are correct, suspect the IC511 Video Processor. However, when one of the S/H voltages is incorrect, there are a few possibilities:

The screen control could be mis-adjusted. Simply turn the screen adjustment up or down. If this is the problem, the set should unblank before the adjustment brings the tube to retrace. If the voltage at Q501/B is not within the levels mentioned above, there could be a problem with that picture tube or its biasing. The voltage at Q501/B depends on the voltages output by each pin 5 on the video drive IC's.



IK/AKB

TVP08J47 1030 12 17 98

Sync Paths

Overview

The purpose of this slide is to show you the various sync signals and the names for these signals. The RA-4 sync paths are more complicated than normal due to the complexity of its operation.

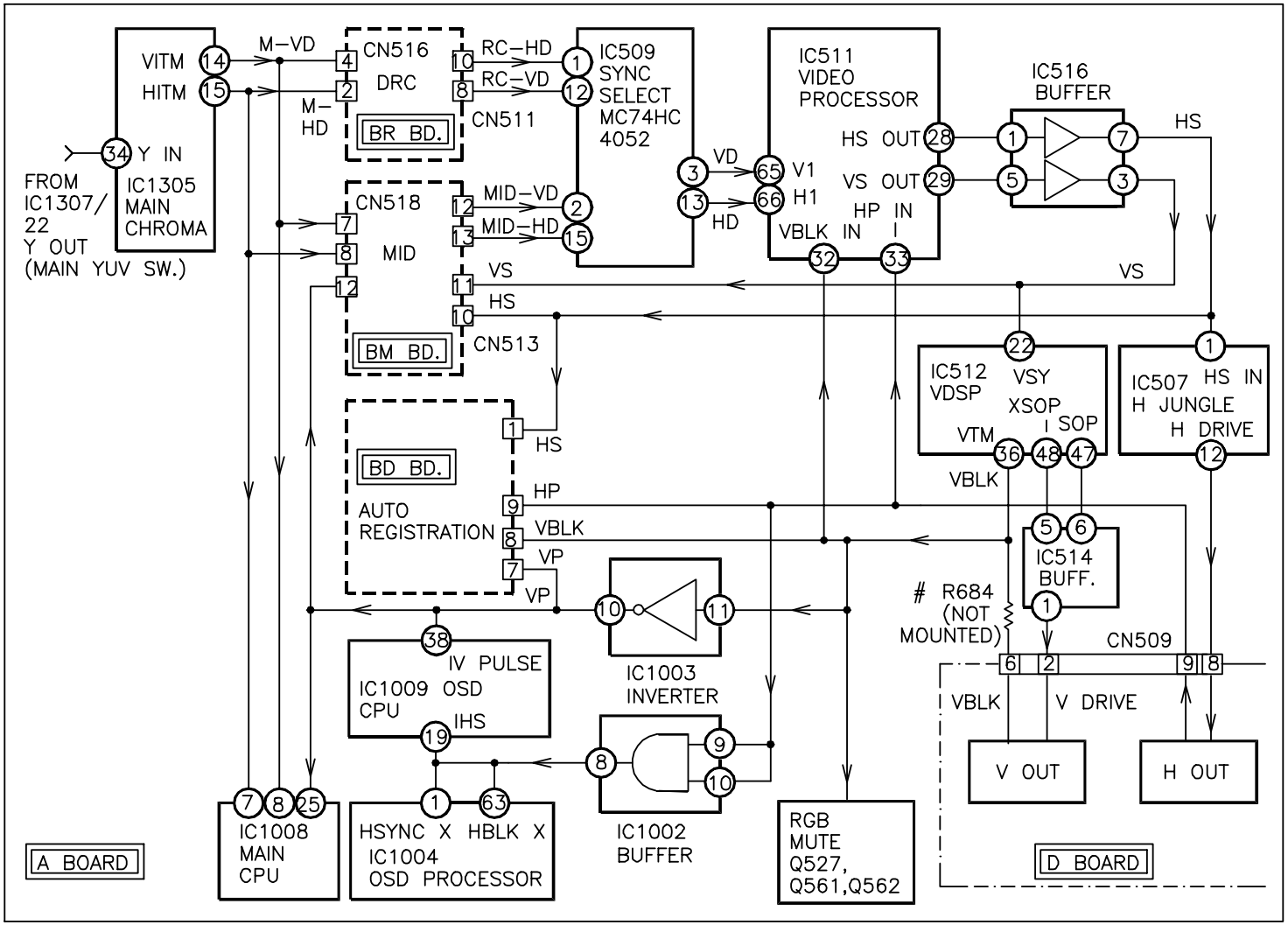
Sync Paths

The Y signal is input to IC1305 Main Chroma Decoder. The main sync signals are extracted from this signal and output at IC1305/14 VITM and IC1305/15 HITM. The VITM signal is a 60 Hz signal called M-VD. The HITM signal is a 15.734 KHz called M-HD. If the M-VD pulse is missing, there will be no vertical sync. If the M-HD pulse is missing, there will be no horizontal sync.

The M-VD and M-HD signals are input to the BM and BR boards. Each of these boards outputs its own individual vertical and horizontal sync signals. These sync signals are input to IC509 Sync Select, which selects the proper signals to be input to IC511 Video Processor. IC511 Video Processor outputs the HS and VS signals, which will be used for syncing the drive signals of the vertical and horizontal deflection circuits.

The VS signal is input to the BM board and IC512 VDSP. This IC creates the vertical drive signal, which is output to the Vertical Output IC on the D board. Normally the vertical blanking signal would be created using the vertical boost pulse. Although this circuitry exists, it is not used since R684 is not mounted. This is indicated by the # symbol. The VBLK signal is created by IC512 VDSP instead. The BD board, IC511 Video Processor and the RGB Mute circuit use the VBLK signal. The VBLK signal is also inverted by IC1003 and then called VP. The VP signal is used by the CPUs in the set to time the I2C data. If this signal is missing and video is applied to the set, a failure will occur that causes the power relay to cycle.

The HS signal is input to the BM board and IC507 H Jungle. The H Jungle uses this signal to create the H drive pulse. The H Drive pulse is input to the H Out. The H Out circuit creates a signal called HP. This HP signal is used by IC507 to phase lock the H Drive and H Out signals. The BD board and IC511 Video Processor also use it. The HP signal is sent through IC1002 Buffer to be used by IC1009 OSD CPU and IC1004 OSD Processor.



SYNC PATHS

TVP0819A 1019 12 17 98

Deflection Block

Overview

This block shows the basic deflection circuits and how they are interconnected. There are four basic circuits. They are Vertical, Horizontal, High Voltage (HV) and Convergence or Sub-Deflection.

Vertical

The vertical circuit develops the vertical sync circuit and outputs vertical drive to the three yokes. It also manufactures the Pin E/W signal and AFC signals which are used by the Horizontal section. The vertical circuit receives a ½ H signal derived from the HS signal, which is used by the countdown circuit in the DSP. The vertical block is made up of the VDSP, HBLK Delay, the ½ H and Odd/Even and Vertical Output circuits.

Horizontal

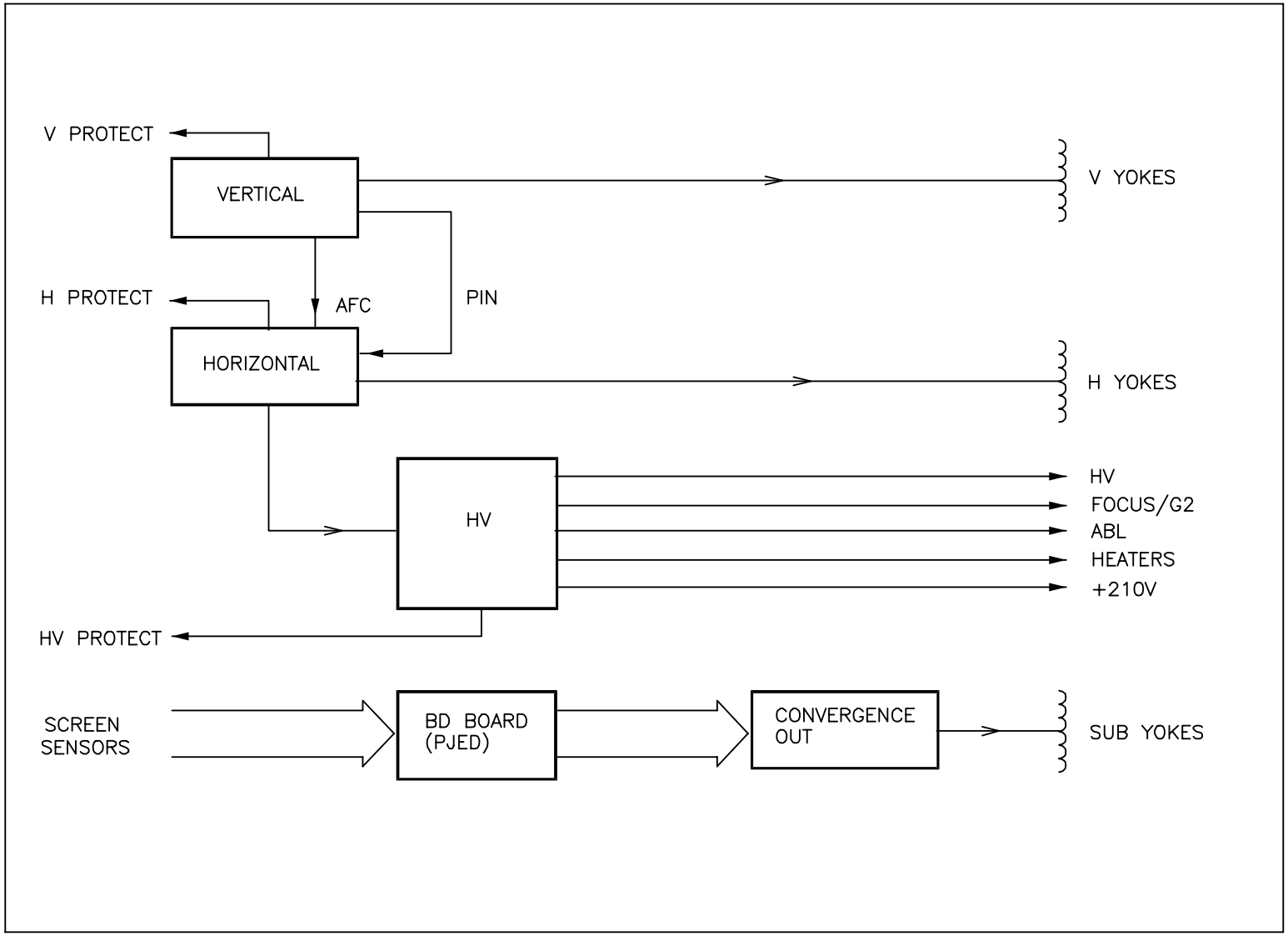
The horizontal circuit develops the horizontal drive signal used by the by the horizontal output to supply current to the H yokes. The High Voltage circuit to develop the outputs of the High Voltage circuit also uses this signal. In addition, the Horizontal circuit uses the AFC and Pin signals from the vertical section to create the proper picture on the screen. The horizontal block consists of the Horizontal Jungle, Horizontal Drive and Output, Pin Amp and HP/H protect circuits.

High Voltage

This set does not use the H Output to produce High Voltage. It has its own output stage that amplifies the H Drive signal and applies that output to the FBT. The FBT creates High Voltage, Focus Voltage, ABL, Heater Voltages and +210 Volts. The High Voltage is regulated to keep the picture from changing size when brightness levels change. The High Voltage section consists of HV Drive, HV Output, HV Regulation PWM, HV Regulation Control and HV Stop 1 and 2.

Convergence

The convergence circuit is used to overlay the output from the three tubes on top of each other. It uses inputs from the sensors around the screen to adjust centering and skew when the Auto Focus button is pushed. It also uses data input at the factory to produce the correct waveform needed to overlay each tubes picture on top of each other. These signals are amplified by the convergence outputs and applied to the sub yokes for each tube. The Convergence circuit consists of the sensors, BD board and Convergence amplifiers.



DEFLECTION BLOCK

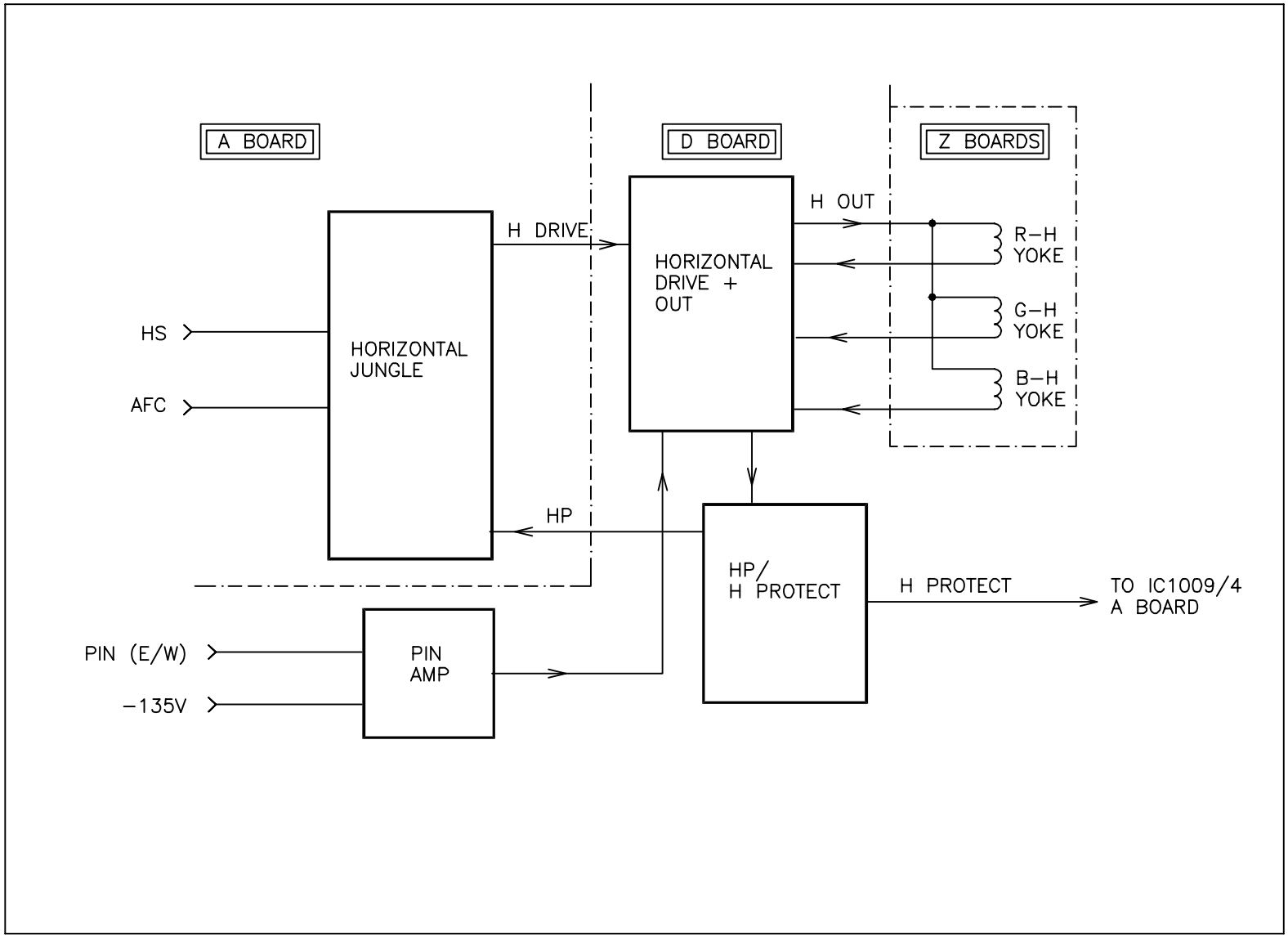
TVP08J12 993 12 17 9

Horizontal Deflection Block

Overview

The Horizontal Jungle uses an oscillator synced by the HS and AFC signals to produce the H Drive signal. The Horizontal drive signal is used as input to produce the horizontal output. The Pin amplifier is used to vary the amount of current supplied to the horizontal yokes so that more current is delivered when the beam is sweeping the middle of the tubes.

A sample of the horizontal output signal is used by the HP/H Protect to produce the HP signal. The HP signal is fed back to the Horizontal Jungle to phase lock the Horizontal Drive and Horizontal Output. The H Protect circuit uses the HP signal to detect proper operation of the horizontal circuits. If a failure occurs, the protect circuit will shut down the set and inform IC1009 OSD Processor if a failure has occurred.



HORIZONTAL DEFLECTION BLOCK

TVP08J28 1032 12 3 98

Horizontal Jungle

Overview

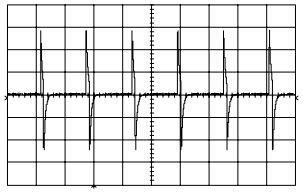
IC507 Horizontal Jungle uses an internal oscillator to generate an H Drive signal that is used to produce the horizontal output for the yokes and the High Voltage. IC507 H Jungle also receives AFC and HP inputs that are used to phase synchronize the H Drive output with the Horizontal Output and Vertical circuits.

H Drive

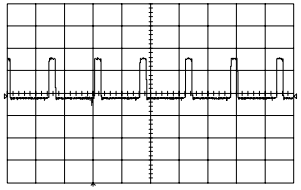
The internal oscillator of IC507 H Jungle has its rough frequency set by C521, C522 and R549, which are connected to IC507/8 and 9. IC507/7 AFC Output controls the fine adjustment of this frequency by phase shifting the oscillator output. This is performed by using the inputs at IC507/1 HS In, IC507/4 HP Input and IC507/2 AFC Input. IC507/5 Filter 1 uses C546 and C548 to create a sawtooth signal, which is used to generate the AFC output. IC507/2 AFC Input is a signal created by filtering the AFC signal with C526, R534 and C525. IC507/3 uses R550 and C550 to generate the pulse width of the phase shifting circuit inside of IC507.

IC507/6 Filter 2 uses C543 to generate the comparison voltage, which is compared to the sawtooth signal created by IC507/5 to create the output voltage at IC507/7 AFC Output.

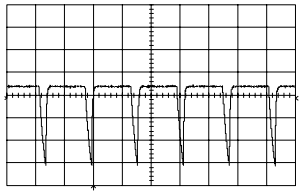
The output of this circuit is the H Drive signal, which exits at IC507/12. This signal passes through an internal circuit that uses the voltage at IC507/11 HD Duty. This circuit sets the duty cycle to 50% since the voltage there is half of the 12-volt supply. The H Drive output is sent through Q514 Buffer and then output from the A board to the D board via CN5004/8 which is where the Horizontal Drive and Output circuits are located.



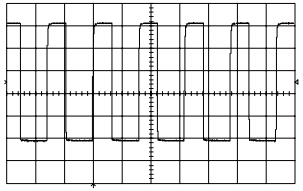
IC507/1
HS
1V 20 us



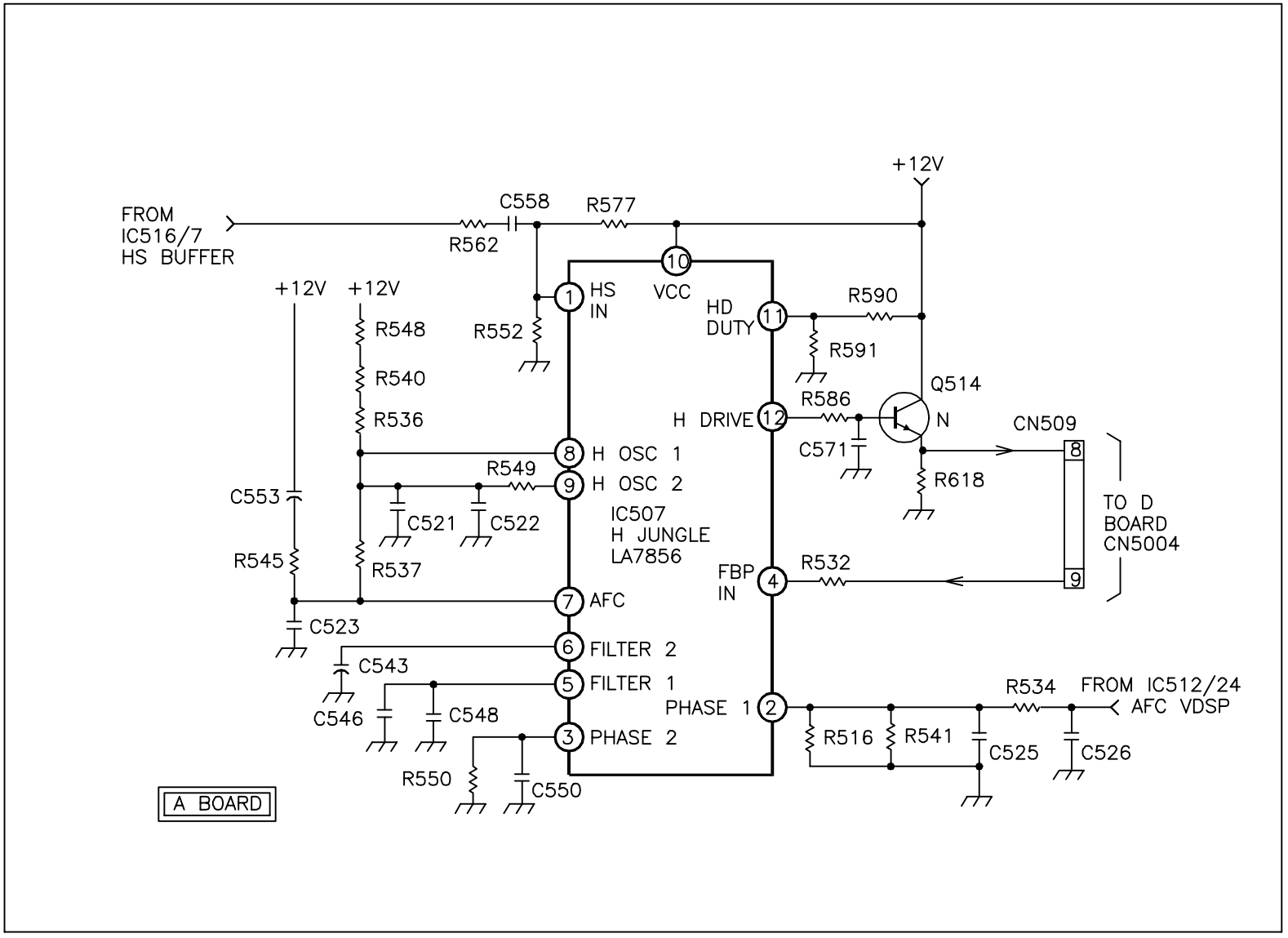
IC507/4
FPB IN
1V 20 us



IC507/2
Phase 1
1V 20us



IC507/12
H Drive
2V 20us



HORIZONTAL JUNGLE

tvp08j18 999 12 17 98

H Out

Overview

The H out circuit is used to amplify the H Drive signal and deliver a current signal, which will be applied to the Horizontal yokes. The signal applied to the yokes will be a current sawtooth that pulls the CRT beams across the screen at the Horizontal rate of 31.5 Khz. This circuit also uses T5002 to create a DC offset voltage necessary to correct the tube angles where the red and blue tubes are placed.

H Drive

The H Drive signal is input at CN5004/8 and applied to the base of Q5002. Q5002 is a buffer signal that passes the H Drive signal to C5005. C5005 is a filter used to remove any DC component in the H Drive signal. The H Drive signal is applied to the base of Q5008/B. This creates a signal at Q5008/C, which is applied to T5001 HDT.

R5031 and C5019 is a snubber filter that is used to reduce any spikes on the amplified HD signal. If there is a problem with these components, it could cause the Q5013 H Out to heat up and fail. R5032 and R5026 are fusible resistors designed to optimize the gain of Q5008 Horizontal Drive Transistor. The signal developed across T5001 HDT primary windings is coupled to its secondary, which feeds the H Out circuit.

H Out

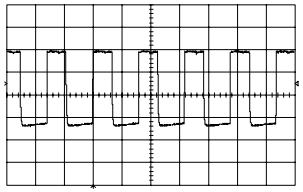
When the H Drive pulse reaches Q5013/B, it causes current to flow in the H yokes through the C-E junction of Q5013. This causes the CRTs beams to go from the middle of the tube to the right hand side. When the pulse goes LOW, D5009 Speed Up causes Q5013 H Out to shut off immediately. When Q5013 H Out shuts off, the magnetic field in the yokes collapses and induces a voltage that will cause C5039 to charge. This causes the beams to go from the right to the left side of the CRTs. When C5039 is fully charged, the magnetic field in the yokes will be dissipated, causing C5039 to discharge through the yokes. The remaining current required will flow through D5013 Damper. This will cause the beam to move to its original position and the whole process begins again with the next H Drive pulse.

The pin amp has an effect on the width of the picture since more current is required to move the beam at the center of the tubes. The pin signal modulates a vertical parabola signal onto the H Out signal. This causes more current to flow through the yokes when the beam is towards the center of the tube.

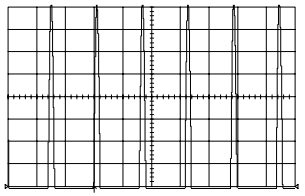
C5043, C5042 and C5041 form an AC Voltage Divider that is used to reduce the level of the H out signal. The pulses created across C5038 are sent to the H pulse shaper circuit and used for the creation of the HP pulse and to detect proper operation of the H Output by the H Protect.

Horizontal Centering

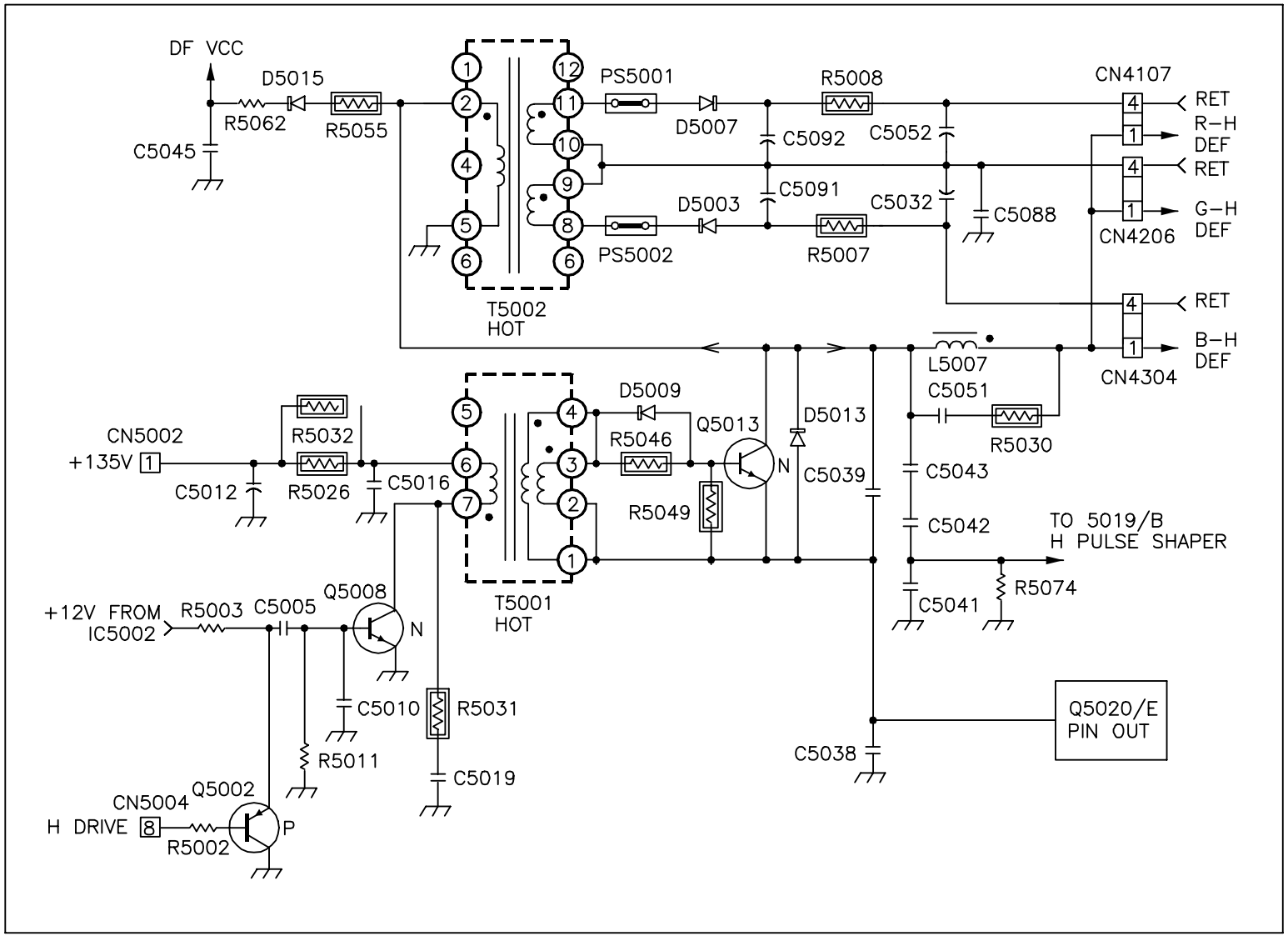
Since the red and blue tubes are not at 90-degree angles to the screen like the green tube, we need to create an offset voltage. This is done by applying the pulses from Q5013 H Out to T5002 HOT and rectifying these pulses on the secondary side. The center tap of T5002 secondary is connected to the return of the green yoke. One winding is connected through PS5001, D5007 and R5008 to the return of the blue yoke. The other winding is connected through PS5002, D5003 and R5007 to the return of the red yoke. This configuration causes a positive offset voltage across the red yoke relative to the green yoke, and a negative offset voltage across the blue yoke relative to green. This roughly centers the red and blue tubes pictures with green.



Q5008/C
2V 20us



Q50013/C
100V 20us



H OUT

TVP08J13 990 12 17 98

Pin Amp

Overview

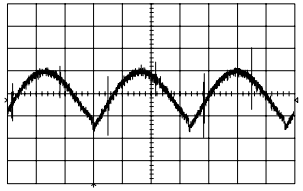
Since it requires more current to move the CRT beam in the center of the screen to the screen's horizontal edges, a Pincushion correction or Pin Amp is necessary. The Pin Amp is used to deliver additional current to the horizontal yokes as the beam gets closer to the center of the tube and less current as the beam nears the top and bottom of the screen.

Pin Amp

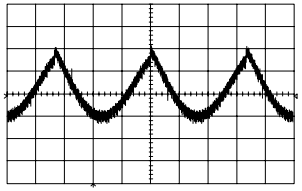
The Pin (E/W) signal from the VDSP is input to Q5003/B. This signal is a .5 Vpp 60 HZ parabola waveform and is inverted by Q5003 and applied to Q5007/E. Q5007 is a common base amplifier whose input goes into its emitter and out of its collector. Q5007/C sends signals to Q5011/B. Q5011 is a buffer and the waveform is output from Q5011/E.

This signal is applied to Q5012/B, which is the input to a differential amplifier consisting of Q5012 and Q5017. When the negative going signal is applied to Q5012/B, it causes more current to flow through its C-E junction. This in turn causes less current to flow through Q5017 C-E junction, which causes the signal at Q5017/C to become more negative. After the parabola has reached its negative peak, it will begin to be more positive. When this occurs, less current flows through Q5012 C-E and more flows through Q5017 C-E. This causes the signal at Q5017/C to become more positive. This signal is applied to Q5018/B. When the signal becomes more negative, it causes current to flow through Q5020 E-B junction and Q5018 E-B junction. When current flows through Q5020 E-B, it causes current to flow through Q5020 C-E. This circuit is connected to horizontal output circuit and causes more current to flow through the horizontal yokes. This increase in current flow allows the picture to be uniform in size throughout the whole screen.

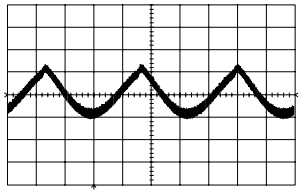
D5018 is in place to act as temperature compensation for this circuit. D5012 is also used for this, but has been replaced by a jumper in most sets. It does this by increasing the current flow though Q5017 when Q5020 conducts. This in turn makes the signal at Q5018/B more positive, thereby decreasing the current through Q5020. This keeps the circuit thermally stable. If D5018 were to open, Q5020 would go into thermal runaway and eventually fail.



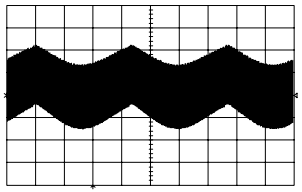
Q5003/B
5V 5ms



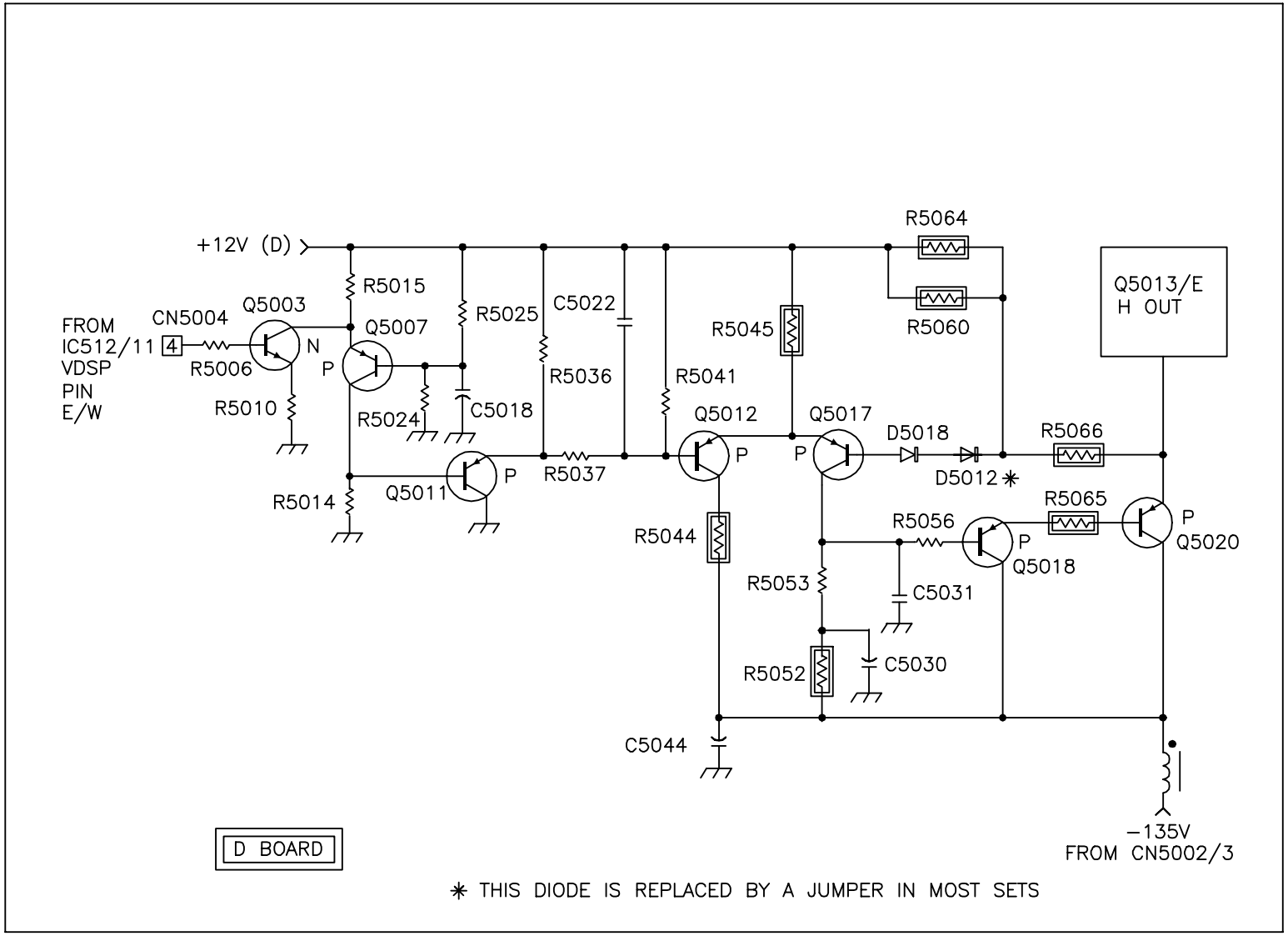
Q50011/B
5V 5ms



Q5018/B
5V 5ms



Q5020/E
10V 5ms



PIN AMP

TVP08J14 992 12 17 98

H Protect/HP

Overview

The H Protect/HP circuit has two purposes. The first is to use a sample from the Horizontal output to create the HP pulse, which is used to control the phase of the H Drive pulse. The second is to create a HIGH output on the H Protect line if there is a loss of the HP pulse. This HIGH is used to trigger the latch circuit and shut down the set.

HP

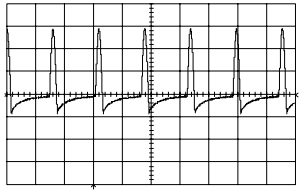
Pulses from the horizontal output circuit are input to Q5019/B. This signal cuts off the bottom of these spikes and these modified spikes are output Q5019/E. This signal is input to Q5016/E. Q5016 is a common base amplifier whose input is the emitter and output is the collector. This amplifier squares off the tops of these spikes. This signal is the HP or HBLK pulse and is used to control the phase of the H Drive signal, as well as the H Protect circuit.

H Protect

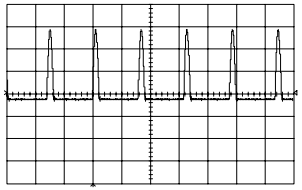
The HP signal is applied to Q5014/B. Since it is a positive going pulse, it is blocked by D5014 from Q5015/B. When the positive going pulse is input to Q5014, it turns the transistor OFF causing 6Vpp pulses to be present at Q5014/E. This voltage comes from the +12 volt line through R5058 and Q5015 B-E junction. This pulse is applied to a peak detect circuit consisting of C5026, R5039, D5008 and C5020. As long as pulses continue to be applied to this peak detect circuit, C5020 will hold a charge. The voltage from this charge is enough to keep Q5006 ON since it applies .6 volts to Q5006/B. This keeps Q5006/C LOW whenever the HP signal is present. If the pulses should disappear, the DC present would be stopped by C5026 and C5020 would not charge, turning Q5006 OFF and causing a HIGH output from Q5006/C.

H Protect Delay

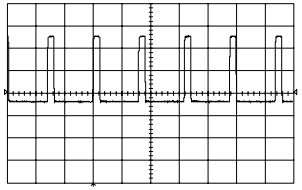
Q5009 is the H Protect Delay and delays the operation of the H Protect circuit until C5011 charges. When the set is turned ON, current flows to ground through Q5009 B-E junction and C5011. This allows for .6 volts to be present at Q5006/B until C5011 charges. The HP pulse should be present at this time. If not, the H Protect line will go HIGH and the set will shut down.



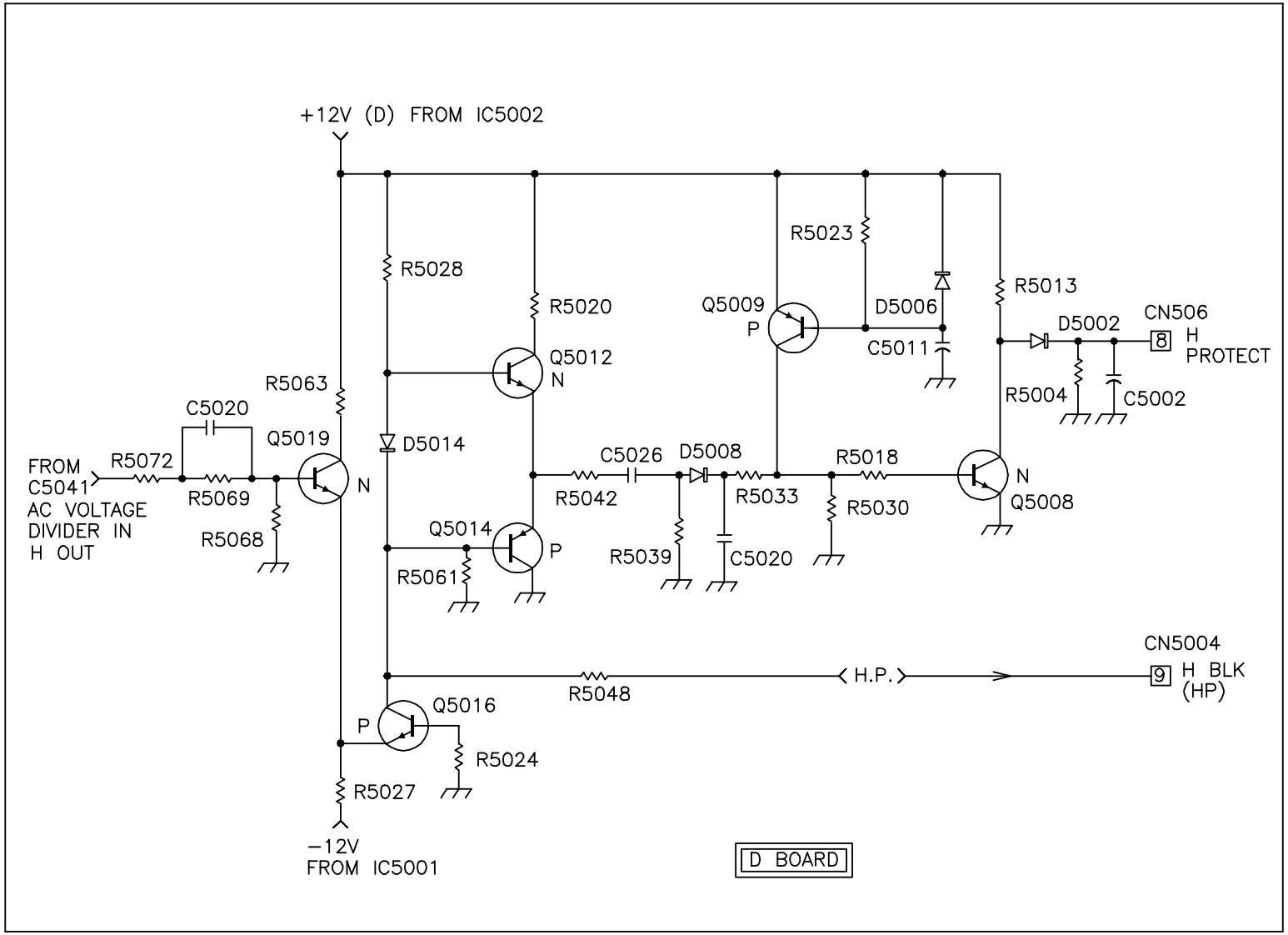
Q5019/B
2V 20us



Q5019/E
2V 20us



Q5016/C
2V 20us



H PROTECT/HP

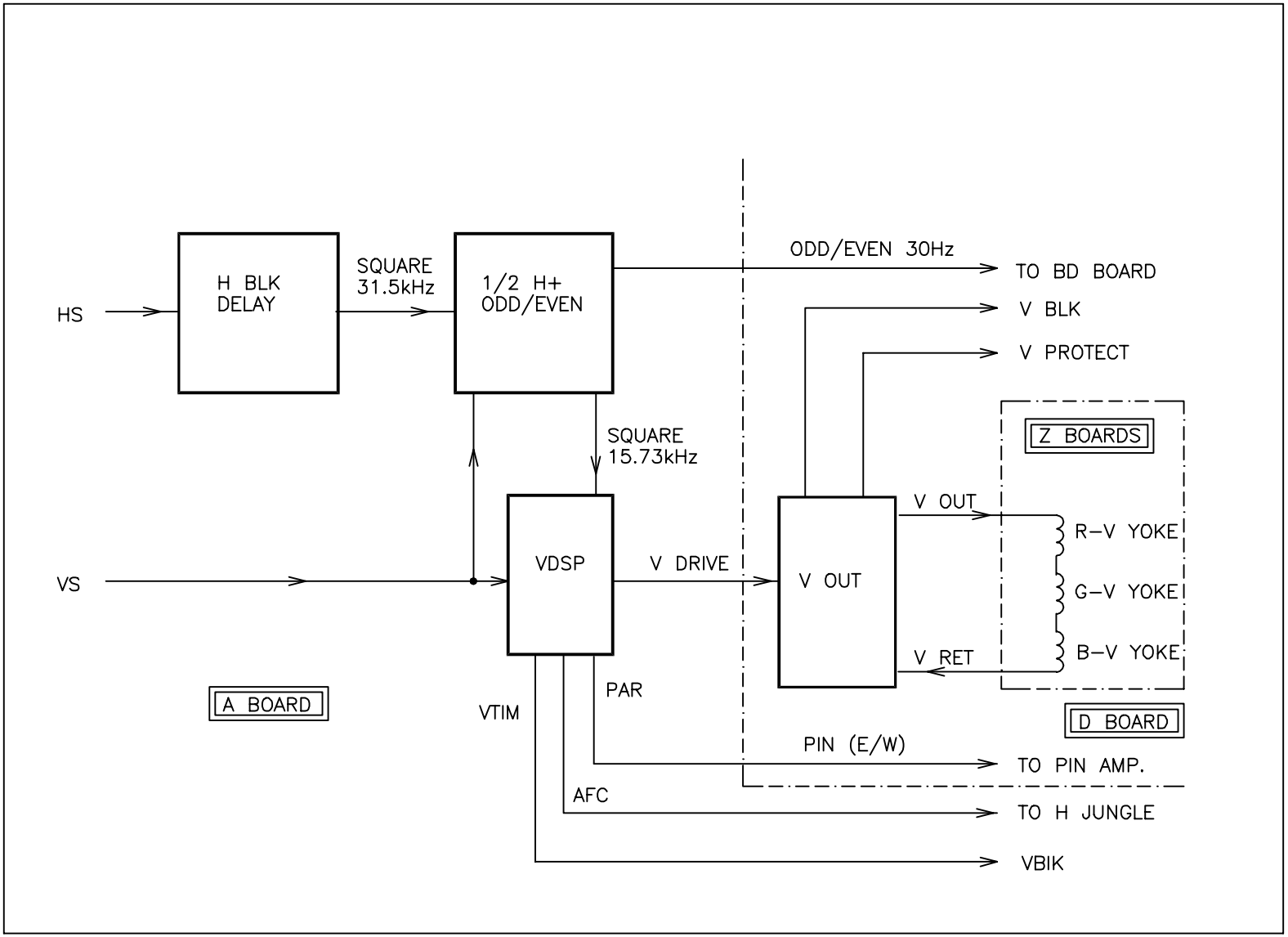
TVP08J15 991 12 17 98

Vertical Deflection Block

Overview

The Vertical Deflection circuit uses the HS and VS signals to produce the vertical drive, VTIM, Par or Pin and AFC signals. The HS signal is necessary because the VDSP circuit works by counting down this frequency to produce its 60Hz outputs. The HS signal goes through the H BLK Delay circuit, which stretches the HS pulse so that it is a square wave. This signal is then applied to the ½ H and Odd/Even circuit along with the VS signal. This circuit produces two outputs. The first is the ½ H signal that is a 15.734 kHz square wave. The second output is the Odd/Even pulse. This signal is a 30Hz signal, which is used by the OSD Processor and the BD board.

The VDSP circuit uses the VS and the ½ H signal to produce four outputs. The V Drive output is a sawtooth wave that is applied to the V Out circuit and then applied to the vertical yokes. The VTIM output is the vertical timing pulse. It is also called VBLK and is used to mute the video drive during vertical blanking. It is also inverted, called VP and is as a timing pulse by the various CPUs in the set. This pulse is used to synchronize the data. The Par output is a 60 Hz parabola signal that is used by the Pin amplifier in the Horizontal circuit. The AFC output is used by the H jungle to synchronize the H Drive signal with the Vertical drive.



VERTICAL DEFLECTION BLOCK

TVP08J29 1033 12 21 98

H BLK Delay and ½ H + Odd/Even

Overview

The VDSP IC requires a 15.734 KHz square wave input for its countdown circuit. The HS signal goes through the H BLK Delay circuit, which stretches the HS pulse so that it becomes a square wave. This signal is then applied to the ½ H and Odd/Even circuit along with the VS signal. This circuit produces two outputs. The first is the ½ H signal that is a 15.734 KHz square wave. The second output is the Odd/Even pulse. This signal is a 30Hz square wave, which is used by the OSD Processor and the BD board.

H BLK Delay

The VDSP requires a horizontal frequency square wave to operate its countdown circuit. Since the HS pulse is not a square wave, we need to stretch it so that a pulse is created that starts at the same rising edge but has a 50/50-duty cycle. This is done using IC517 H BLK Delay, which uses two identical delay circuits to lengthen the width of the HS pulse.

IC217 H BLK Delay contains two identical circuits which contain a two input OR gate with one input bubbled, and a pulse delay circuit with Q and NOT Q outputs.

The HS signal is input to IC517/12 HS. IC517/11 B2 is tied to the Def 5 volts. Since an OR gate produces a HIGH output any time one of its inputs is HIGH, the gate inside IC517 will be HIGH whenever the HS pulse is HIGH. This pulse is input into the delay circuit. The output's HIGH to LOW transition is delayed by the time constant of R661 and C576, which are to IC517/14 C2/R2. The delayed signal is output at IC517/10 Q2.

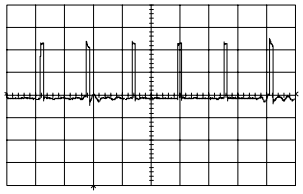
IC517/10 Q2 is then sent through R663 to IC517/5 HS1. Since this is a bubbled input to the OR gate and IC517/4 A1, the other input, is connected to ground, the output is of the OR gate will be HIGH whenever the input of pin 5 is LOW. This signal is delayed by the time constant of R670 and C580, which are connected to IC517/2 C1/R1. This delayed signal is output at IC517/6 Q1.

½ H and Odd/Even

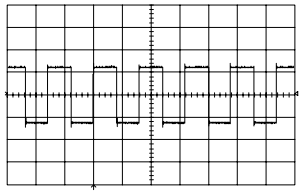
The output from IC517/6 is input to two pins on IC508 ½ H and Odd/Even. They are IC508/3 1Clk and IC508/12 2D. Each of these inputs is for one of the two D flip-flops inside IC508.

In flip-flop 1, the signal from IC517/6 is input to the clock input. The data input at IC508/2 is tied to IC508/6 NOT Q. When the data input of a D flip-flop is tied to its NOT Q output, the circuit will output a signal that is the Clk signal divided by 2. This means that the output at IC508/5 1Q will be half the input frequency of the input at IC508/3 1Clk. This signal is called ½ H and is output to IC512/16.

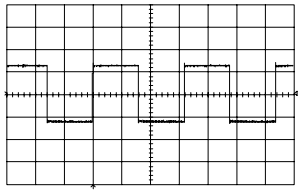
In flip-flop 2, the signal from IC517/6 is input into the data input. The clock input has the VITM signal input to it. The VITM pulse from IC512/22 is also called VBLK and is a short pulse timed at the vertical blanking interval. Each of these pulses represent a field of video. The flip-flops output can only change state when the clock pulse is on its positive edge and the two inputs are timed so that the data input is HIGH or LOW for every other clock pulse. The result is a HIGH signal being output from Q on the first clock pulse and a LOW being output on the second clock pulse. Since the output of this circuit is taken at IC508/8 NOT 2Q instead of 2Q, our result would be opposite. The end result is a 30 HZ square wave output at IC508/8. The LOW periods of this signal represent the odd fields and the HIGH outputs represent the even fields. The BD board and IC1009 OSD CPU use this signal.



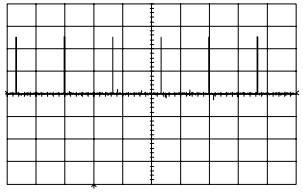
IC517/12
2V20us



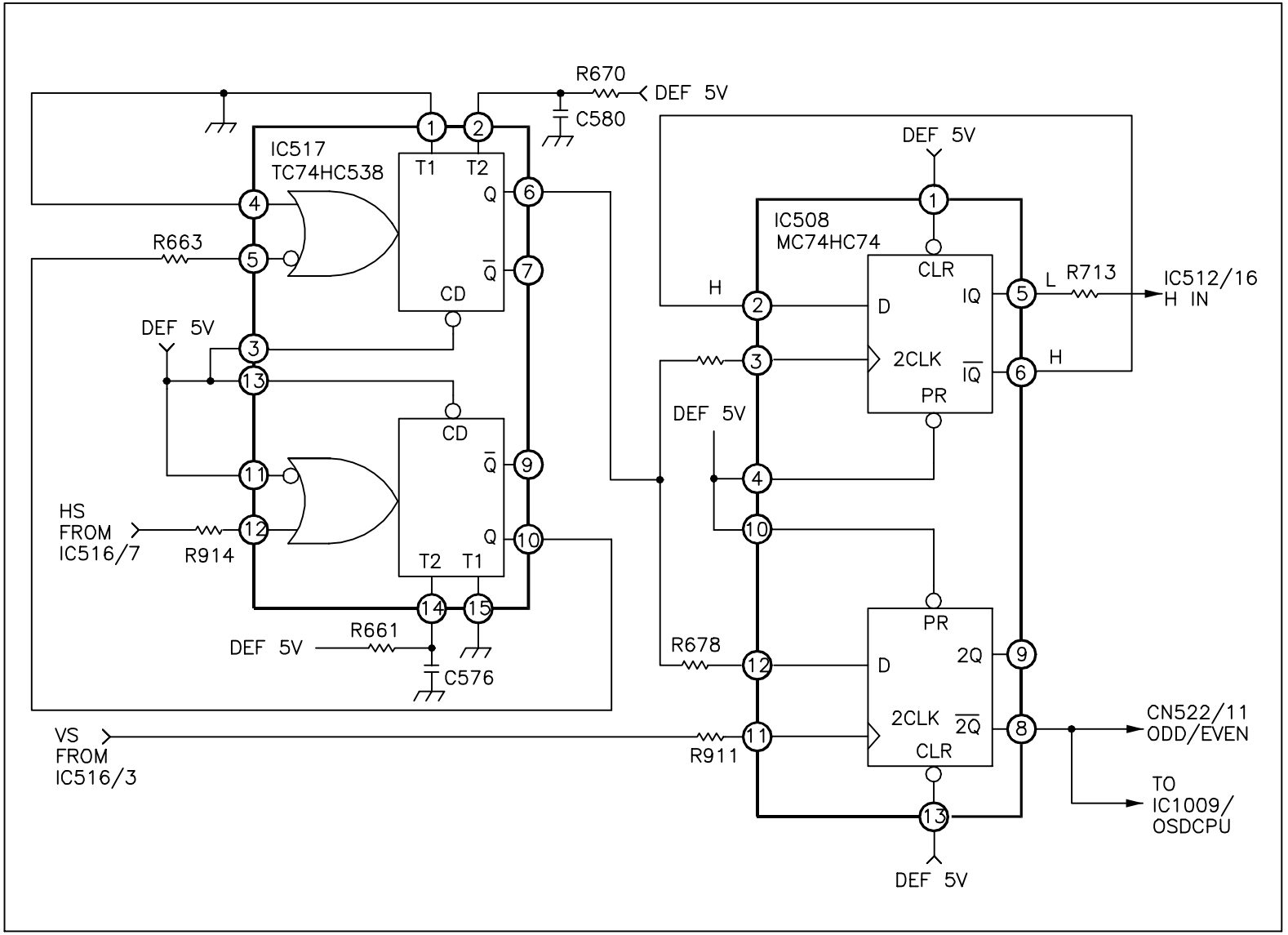
IC517/6
2V 20us



IC508/5
2V 20us



IC508/11
2V 10ms



H BLK DELAY AND 1/2 H +ODD/EVEN

TVP08J21 1002 12 18 98

VDSP

Overview

IC512 is the VDSP or Vertical Digital Signal Processor. This IC outputs the V Drive, Pin, AFC and VTIM signals. It receives data over the I²C bus to manipulate these waveforms. Changing these waveforms varies many of the picture adjustments, including VSIZE, HSIZE, VPOS, UPIN and LPIN, as well as others. This IC consists of four basic parts - they are the VCO, Countdown Processor (CDP), Digital Signal Processor (DSP) and DAC.

VCO

The VCO is needed by the CDP and DSP to provide a stable clock. An internal VCO uses C678, which is connected to IC512/5 VC1, to create a VCO. This VCO is synchronized with the ½ H signal that is input at IC512/16 H In. The two signals are phase compared internally and the output of the phase comparator exits IC512/18 PHA. An op amp internal to IC508 VDSP filters this output using C675 and R757, which are connected to pins 8 and 7. The voltage created by this circuit is used internally to control the frequency of the VCO.

CDP

The countdown processor consists of an ALU, RAM and ROM and operates on an internal program stored in its ROM. The CDP determines which type of system is being used, 50 or 60 Hz, and outputs various counts according to its program. It also receives an input at IC512/22 VSY from the VS signal. This syncs the counting with the vertical sync from the incoming video. This circuit outputs the VTM signal at IC512/36 VTM. This signal will be used as VBLK and inverted and used as VP. Notice that R645 is listed in the service manual with a # symbol next to it. If you see # next to a component in a manual, this means that this component is not mounted on the board. The other outputs from the CDP are input to the DSP section of IC512.

DSP

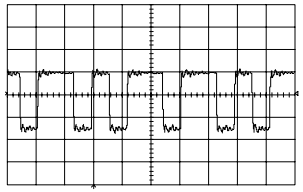
The DSP consists of an ALU, multiplier, RAM and ROM. It uses the count information it receives from the CDP and its own internal program to generate the vertical deflection sawtooth, the Pin or parabolic signal and the AFC compensation signal. This section also receives data to manipulate these waveforms for the picture adjustments stated earlier. These outputs are then applied internally to three 1-bit D/A converters.

DAC

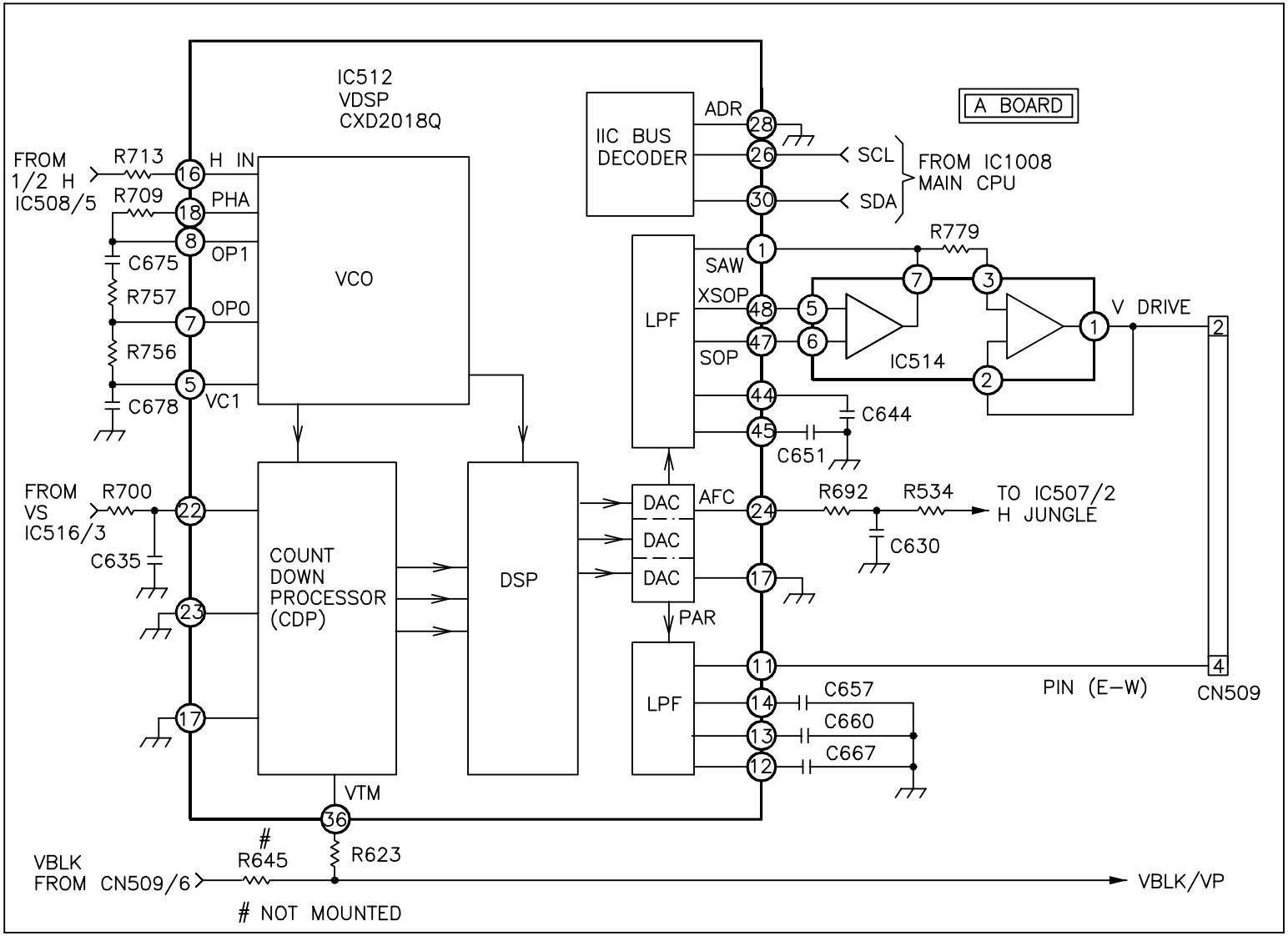
IC512 VDSP contains three D/A converters, two with low pass filters and one without. The DAC without the low pass filter outputs the AFC waveform. Since this is a 1-bit DAC and its output is not being passed through an LPF, the signal at IC512/24 is a high frequency signal resembling a square wave. This signal is output to the H Jungle circuit, which contains the LPF.

The vertical deflection sawtooth is output from a DAC into a LPF. This LPF uses C644 and C651, which are connected at IC512/44 and 45. This LPF outputs complimentary signals from IC512/47 and 48 into IC514/6 and 5. The output from IC512/1 Saw is the sawtooth signal and is input along with the output from IC514/7 into IC514/3. IC514/1 is the buffered output called V Drive that will be used to drive the vertical output circuit.

The parabola or pincushion signal is output from a DAC into a LPF. This LPF uses C667, C660 and C657, which are connected to IC512/12, 13 and 14. IC512/11 Par produces an analog output that is used as the input to the Pincushion correction circuit.



IC512/24
AFC Out
2V 400ns



VDSP

TVP08J22 998 12 18 98

V Out

Overview

The main purpose of the V Out circuit is to amplify the V Drive signal and apply it to the yoke. There is also a V protect circuit that senses the loss of V Output operation and sends a HIGH to the IC1009 and the latch circuit to alert the Self-Diagnostics circuit and shut down the set.

V Out

The V Drive signal is sent from the VDSP on the A board to the D board through CN5004/2. This goes through R5021 and R5043, and enters IC5004/1 Inverting Input. IC5004/7 Non-Inverting Input has a DC reference voltage of 1.25 Vdc input to it. This DC voltage effects the vertical centering position. IC5004 V Out amplifies the input signal and outputs at pin 5. The signal output is approximately 55 Vpp. This is possible even though the difference in supply voltage is only 30 volts because of the voltage boost circuit inside IC5004. This circuit outputs a pulse that boosts the positive supply voltage by increasing the charge of C5037 during retrace. The time at which this occurs is evident by looking at the output waveform.

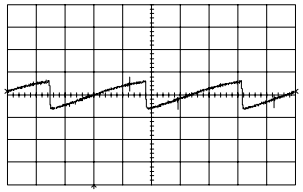
IC5004/5 outputs a signal that is applied to the vertical yokes, which are in series through L5009 and R5076. C5048, C5047 and R5077 act as a damper circuit. C5089, C5040 and R5059 are used for protection purposes. R5047 is the main feedback component. R5071, R5067 and TH5001 also have an effect on the gain of the amplifier. TH5001 is used for temperature compensation. As the circuit operates, the vertical yokes become hot and their resistance increases. When this occurs, R5067 and R5071 become hotter. When they heat up, the resistance of TH5001 is lowered because it is located in close proximity to these resistors. This allows more current for the yokes so that the picture is not effected. C5028 is there to prevent oscillation.

V Protect

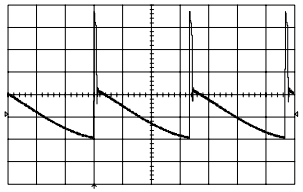
The voltage boost pulse from IC5004/3 is applied to a peak detect circuit consisting of C5034, D5010, R5040 and C5023. As long as these pulses are present, they cause C5023 to hold a charge. This charge causes .6 volts to be present at Q5005/B. This voltage keeps Q5005/C to be LOW. If the pulses should disappear, C5023 would not charge due to the blocking action of C5034. This would cause Q5005 to turn OFF and allow 5 volts to be present at Q5005/C. This would activate the protect latch and also inform IC1009 that a failure has occurred.

V Protect Delay

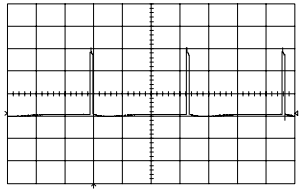
Q5010 is the V Protect Delay and delays the operation of the V Protect circuit until C5013 charges. When the set is turned ON, current flows to ground through Q5010 B-E junction and C5013. This allows for .6 volts to be present at Q5005/B until C5013 charges. The voltage boost pulse should be present at this time. If it is not, the V Protect line will go HIGH and the set will shutdown.



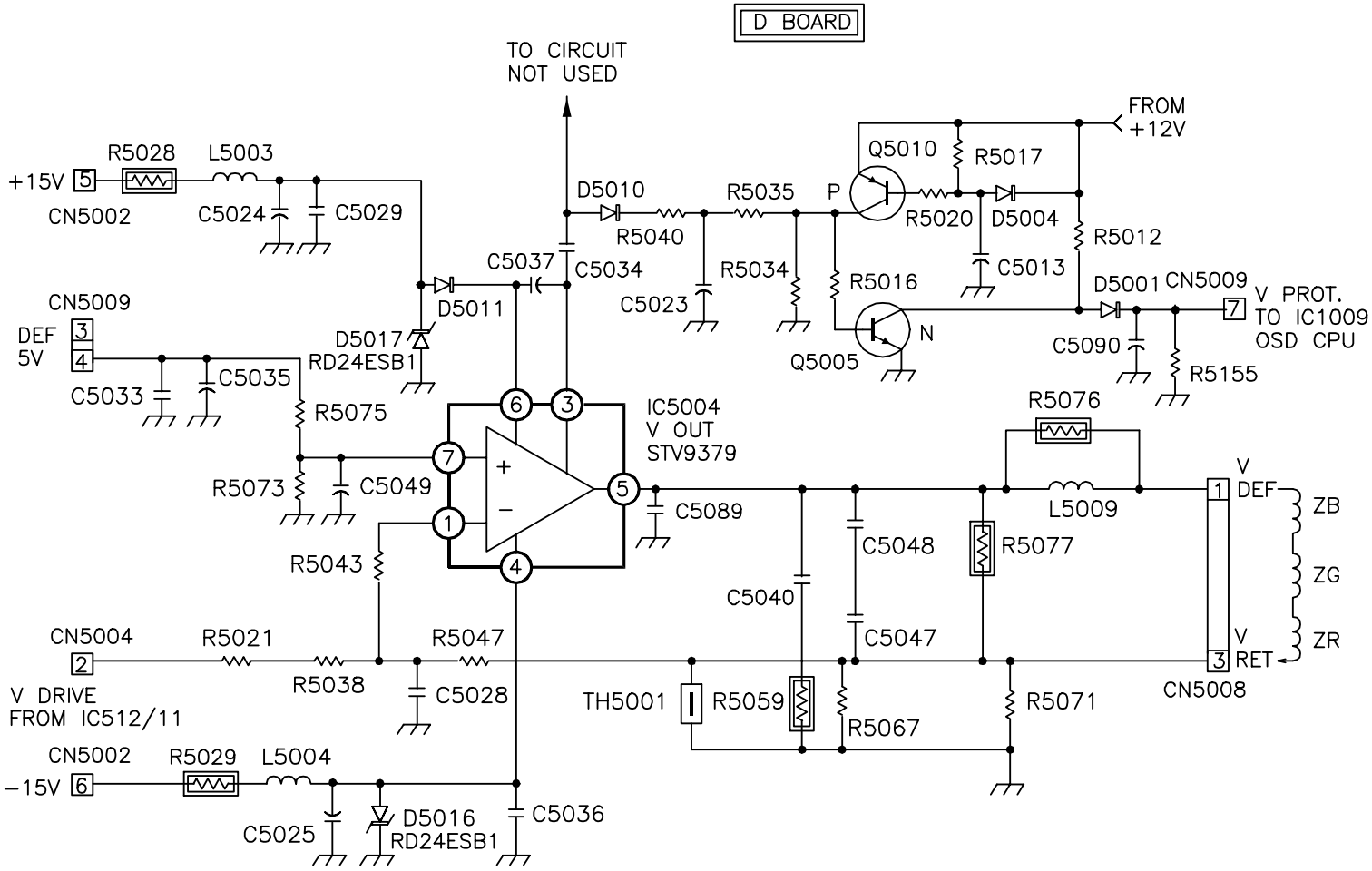
CN5004/2
V Drive
2V 5ms



IC5004/5
V Out
10V 5ms



IC5004/3
Boost Pulse
10V 5ms



V OUT

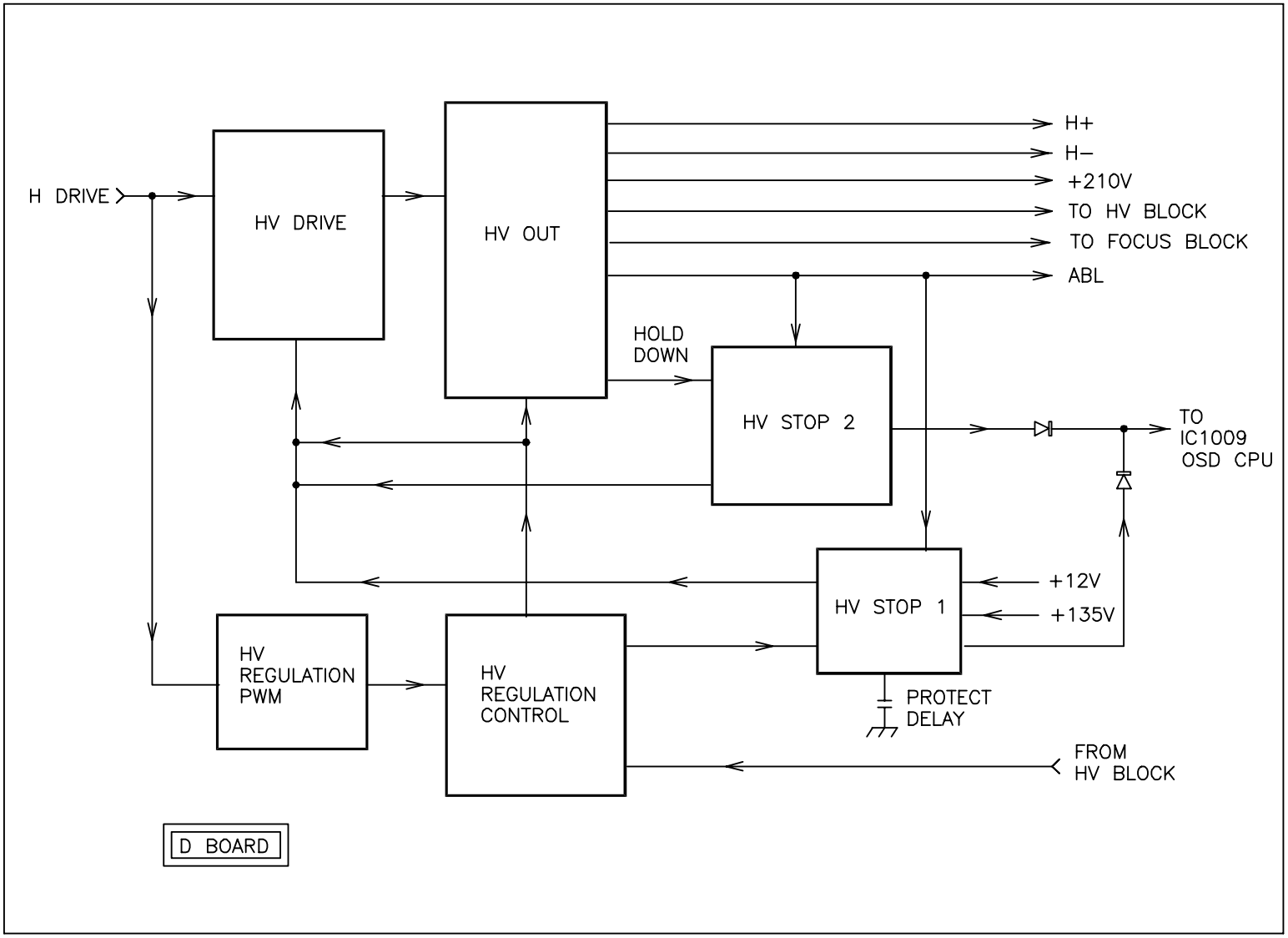
TVP08J17 987 11 23 98

High Voltage Block

Overview

The High Voltage circuit uses the H Drive signal to produce the heater, +210, High Voltage, Focus Voltage and ABL output. This block also uses the H Drive signal to produce a PWM signal. This signal is compared to a voltage tapped off of the High Voltage Block to create a HV Regulation signal. The High Voltage is regulated to keep brightness changes from causing changes in the size of the picture.

There are also two HV Stop circuits, one that monitors the +12, +135 and the tap from the High Voltage Block, and another that monitors a tap from the FBT and the ABL signal. Both of these circuits mute the H Drive circuit and alert IC1009 OSD Processor of a failure. If there is a High Voltage Protect problem, the set will not shut down since there is no connection between the High Voltage Protect circuit and the latch circuit.



HIGH VOLTAGE BLOCK

TVP08J30 1034 12 18 98

HV Drive

Overview

The HV drive circuit amplifies the H Drive signal and applies it to the HV Output. It also uses the signal from the HV Regulation circuit to control the peak drive to the HV Output.

HV Drive

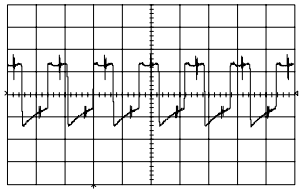
The H Drive signal is input through CN8003/1 and looped through to CN8003/2. If this connector is removed, the High Voltage section will not operate. The signal is then input to Q8005/B through R8010 and R8011. Notice that there is an input from the HV Stop 1 and 2 circuits here. In the event of a protect scenario, this line would be pulled to ground and HV Drive would be disabled. Q8005 is a buffer and the drive signal is output from its emitter.

The signal is then wave shaped by R8008, R8015, C8007, C8006, R8003 and C8004. This signal is input to Q8003/B amplified and output Q8003/C. This signal is coupled through T8001 HDT to the HV Out transistor.

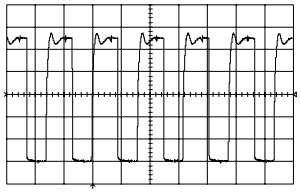
Peak Drive

The peak drive of the HV Drive signal, which was output, from Q8003/C is controlled by a signal from the HV Regulation circuit. The HV Regulation circuit inputs a PWM signal to R8024. R8024 and C8010 integrate this signal into a triangle wave. This triangle wave is input to Q8001/B. Q8001/C outputs a smoothed triangle riding on a DC level. This signal is used to control the conduction of Q8002.

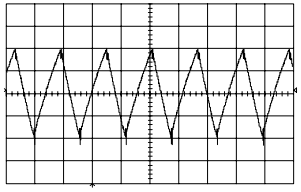
Normally using +135 through the resistance of R8005 and R8007 would develop the HV DRIVE signal. When Q8002 conducts it causes the HV Drive signal to be developed through R8004 and Q8002 C-E junction. This resistance is lower than that between R8004 and R8002, therefore a larger peak signal can be output at Q8003/C.



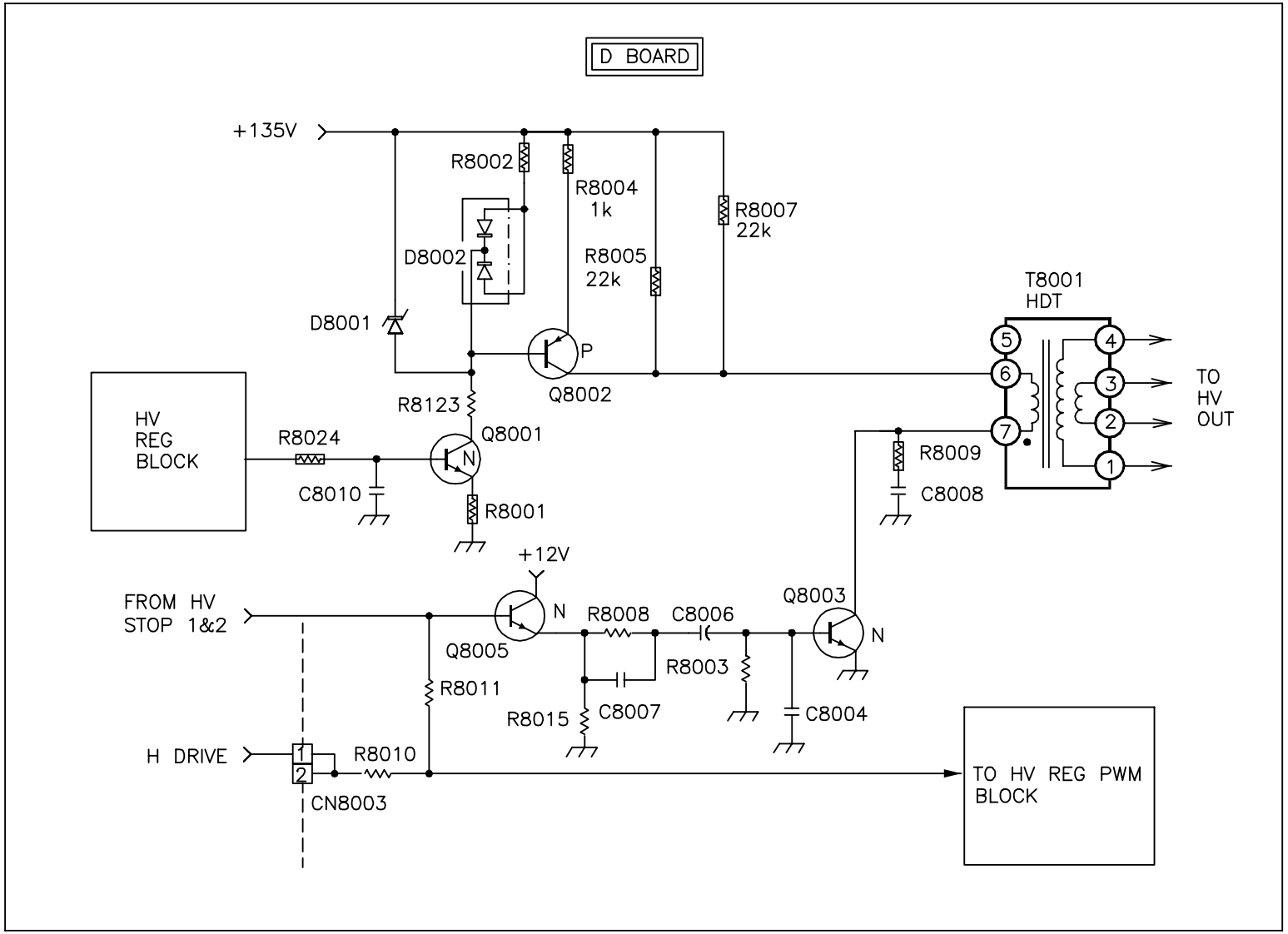
Q8003/B
2V 20us



Q8003/C
20V 20us



Q8001/B
1V 20us



HV DRIVE

TVP08J31A 1038 12 17 98

HV Out

Overview

The High Voltage Out circuit uses the H Drive signal to produce the heater, +210 V, High Voltage, Focus Voltage and ABL output. This circuit is regulated by Q8008 whose conduction is controlled by a PWM signal from the HV Regulation circuit.

HV Out

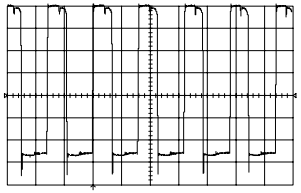
The horizontal drive signal is coupled to Q8007 HV Out through T8001 HDT. As the H Drive signal is applied to Q8007/B, it turns on and allows current to flow through its C-E junction. This is from the snubber filter network consisting of C8003, C8009, D8003, R8012, R8016 and R8020 to the +135 volt line through T8003 FBT and T8002 LOT. When the H Drive signal goes low, the magnetic fields developed by T8003 FBT and T8002 LOT collapse and charge C8018. When the magnetic field is dissipated, C8018 discharges through T8003 FBT and T8002 LOT. The remainder of the current flows through D8007 and D8011 damper diodes until the H Drive signal goes high again.

The voltages developed across the primary windings of T8003 FBT and T8002 LOT are used to create different voltages on their secondary. T8002 Low Output Transformer uses the winding across pins 15 and 17 to develop the Heater voltages used by the picture tube filaments. The pin 15 side of the winding is fused using circuit protector PS8001. This line also contains two current limiting resistors, R8038 and R8039. The winding between pins 11 and 15 are used to develop +210 volts for the video drive ICs. The voltage at T8002/11 is rectified by D8014, filtered by C8025 and through R8183.

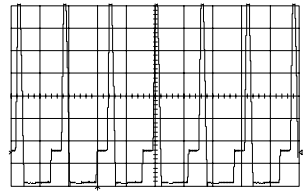
The secondary voltages from T8003 FBT are high voltages delivered to the High Voltage Block and Focus Block. The amount of current being drawn by the High Voltage is monitored using the ABL line at T8003/11. ABL is used in a number of places including the HV Stop circuits. The voltage output by T8003/6 is representative of the level of the High Voltage. It is used by the Hold Down circuit in the HV Stop 2 section.

High Voltage Regulation

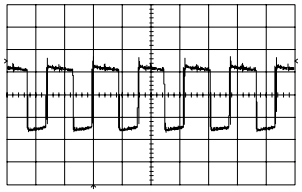
The High Voltage is regulated using a signal developed by the HV Regulation PWM signal discussed later. This signal is applied to Q8008/G. This input waveform causes current to flow through Q8008. This is used to control the width of the pedestal at the bottom of the Q8007/C waveform showed below.



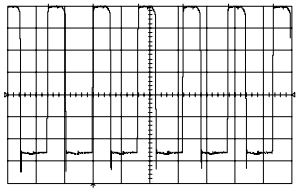
Q8007/B



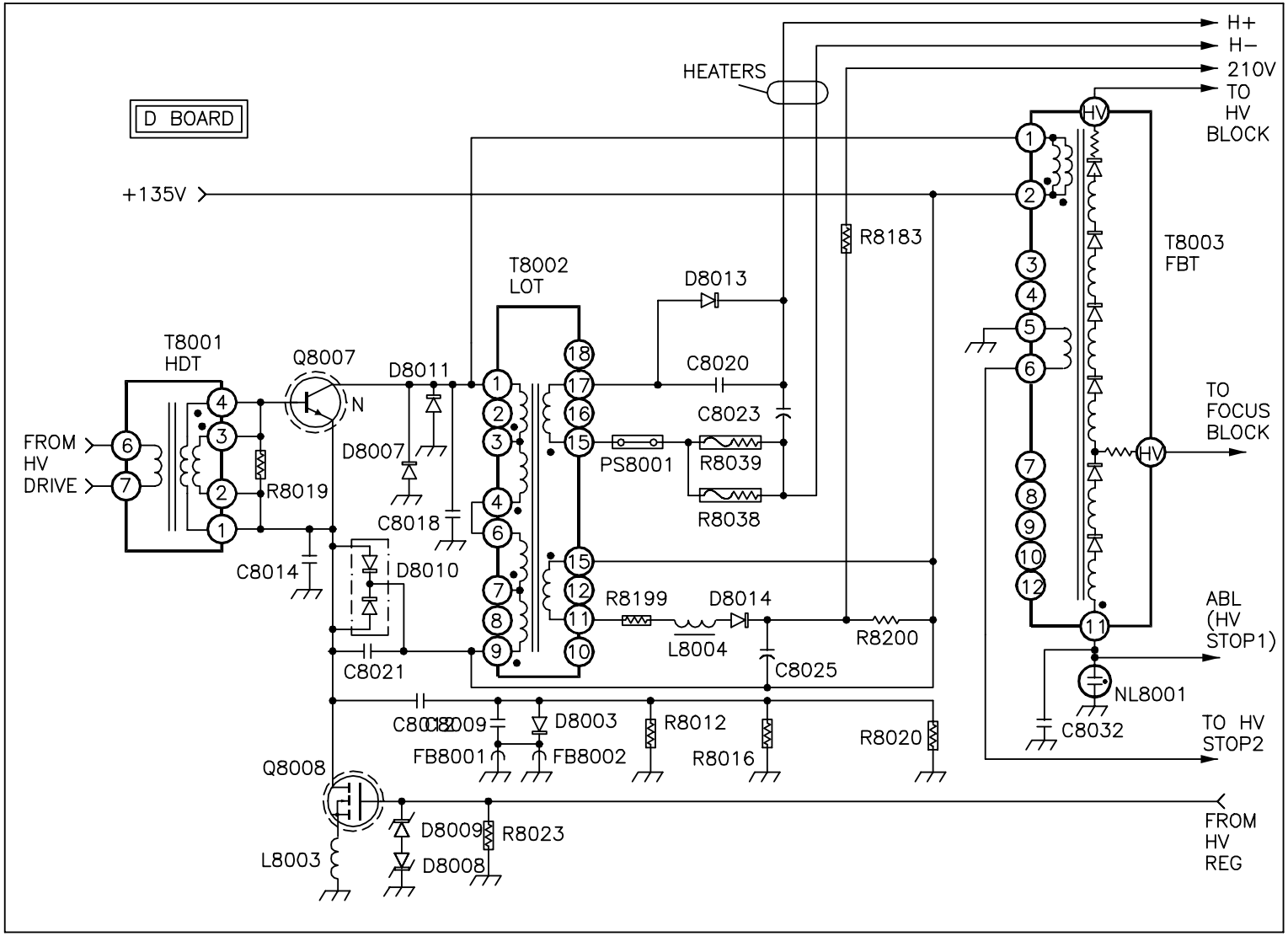
Q8007/C



Q8008/G



Q8008/D



HV OUT

TVP08J31 1003 12 21 98

HV Regulation Control

Overview

The HV regulation control circuit uses a tap from the HV Block to keep the High Voltage at a consistent level. It does this by setting up a reference voltage and comparing that to the voltage from the HV Block tap. This circuit also contains a +12 volt LVP that will lower the High Voltage if the +12 volt line should lower.

Regulation Control

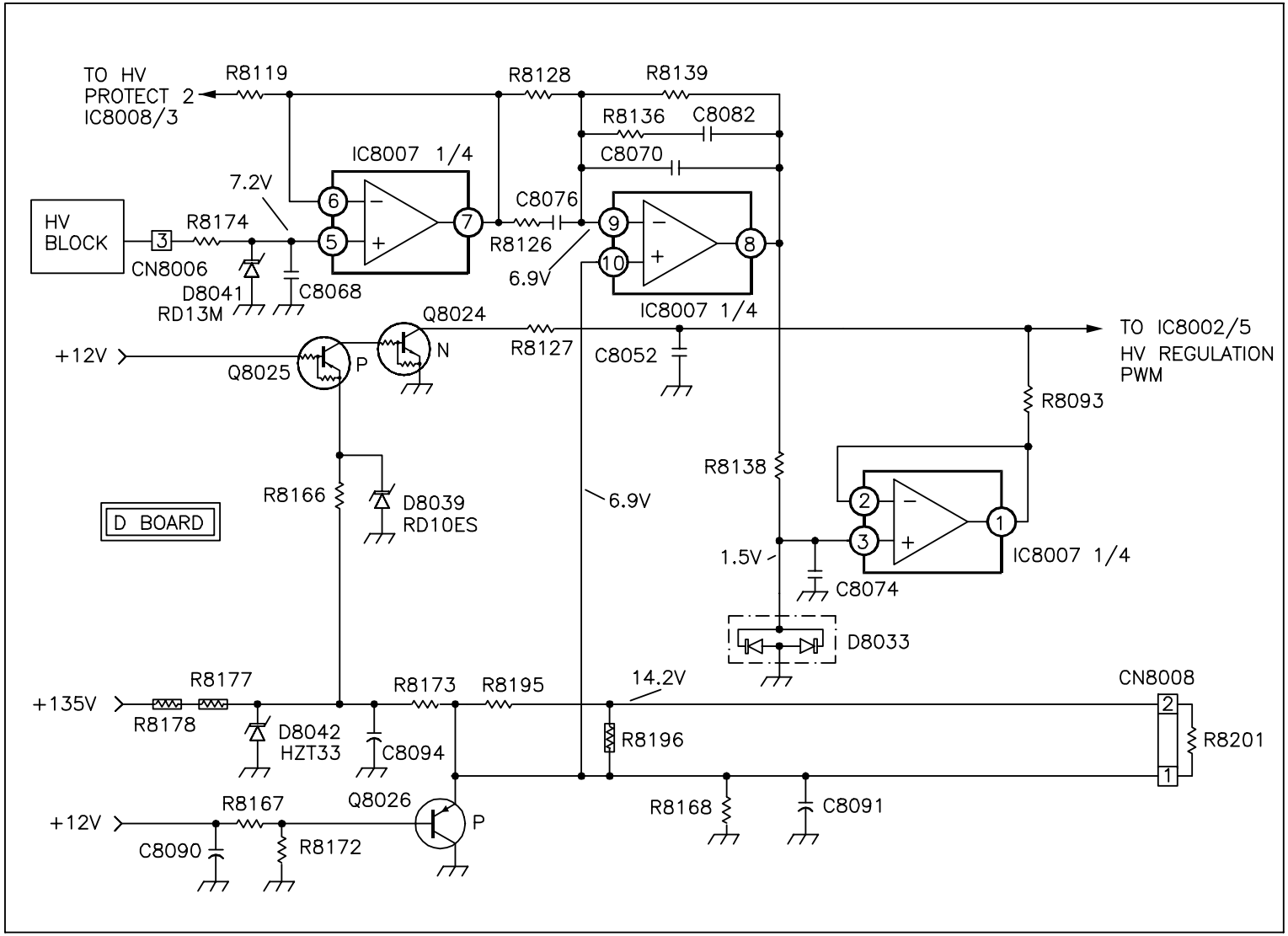
The HV Block has an output that is representative of the High Voltage and rises and falls with the level of High Voltage. The tap from this block is input to the D board at CN8006/3. This voltage, typically around 7.2 volts, passes through R8174 to IC8007/5 Inverting Input. This portion of IC8007 is used as a buffer. Whatever voltage is input at IC8007/5 is output from IC8007/7. This voltage is output to the HV Protect circuit and coupled through R8128 to IC8007/9.

IC8007/10 Non-Inverting Input is a reference voltage that has been set at the factory. It uses the +12 and +135 volt lines to set up a bias across the B-E junction of Q8026. The conduction of the transistor, along with the value of R8196 and R8201, set up the voltage to IC8007/10. R8201 may or may not be present in the set. If it is, it will be mounted on the post of CN8008. The High Voltage is adjusted for 31 KV at the factory. It should be checked and adjusted according to page 57 of the service manual if parts are changed in the High Voltage circuit.

The voltages at IC8007/9 and 10 are used to determine the High Voltage. They should be nearly identical in value when the circuit is acting normally. This portion of IC8007 and its associated components are used as a filter and gain control circuit. Its purpose is to reduce the input voltage and filter the HV Block signal so that the set's response to changes in High Voltage are not too fast or too slow. Typically 6.9 volts is input and 1.5 volts is output. This voltage is sent to IC8007/3, which is a buffer, and then output IC8007/1. It will then be used to vary the HV Regulation PWM signal.

+12 High Voltage LVP

Q8025/B is connected to the +12 volt line. Q8025/E has 10 volts present on it because D8039 holds this voltage. This keeps Q8025 OFF, which keeps Q8024 OFF. If there should be a problem on the +12 volt line, this would cause Q8025 to turn ON. If Q8025 turns ON, then Q8024 would turn ON and cause the High Voltage to be lowered by placing 0 volts on IC8002/3.



HV REGULATION CONTROL

TVP08J33 1005 12 18 98

HV Regulation PWM

Overview

The purpose of the HV Regulation PWM is to create a sawtooth waveform using the H Drive pulses. This sawtooth will be used to create a PWM waveform by comparing it to the output of the HV Regulation Control circuit. This PWM signal will be used to control Q8008 PWM HV Regulator.

Sawtooth Generator

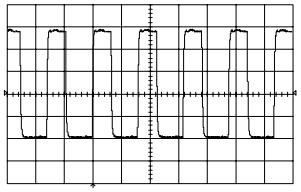
The H Drive signal is input to Q8009/B. Q8009 is a buffer whose output is from the emitter. The signal is next input to Q8010/B, which inverts the signal and outputs it from the collector. R8044, C8026 and C8029 also integrate the signal at this time.

This signal is then compared to a reference voltage by IC8002. IC8002/2 is a reference voltage of 9 volts. The result of this comparison is output at IC8002/1. The signal is then integrated again by C8045 and input to Q8018/B. This signal is inverted and shaped by Q8018 and output from its collector as the following pulse:

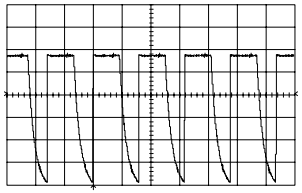
This pulse is input to Q8022/B. When the signal is LOW, Q8022 is OFF, thus allowing IC8008 to act as an integrator. This causes the output at IC8008/7 to rise gradually because C8066 is in the feedback path of IC8008. The output rises like a sawtooth and is applied to IC8002/6 through R8096. The output continues to rise until the pulse at Q8022/B becomes HIGH. When this occurs, C8066 is short-circuited by the C-E junction of Q8022, causing IC8008 to become a buffer. This causes the peak signal of the signal to be passed through D8023 directly to IC8002/6. This places a pulse on the end of the sawtooth during Horizontal retrace time. This cycle continues with the input of the pulses to Q8022/B

PWM

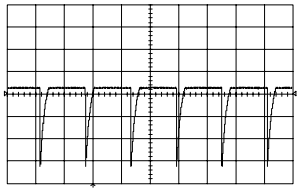
IC8002 PWM creates a PWM signal by comparing the sawtooth signal with the output from the HV Regulator Control circuit whose output comes from IC8007/1. When the Sawtooth signal input at IC8007/6 is greater than the input at IC8002/5, it will cause IC8002/7 to output a LOW. When the sawtooth is less than the regulator input, IC8002/7 will output a HIGH. This PWM causes +/-12 volts to be output at the emitters of Q8015 and Q8016. This signal will be output Q8008 to regulate the High Voltage.



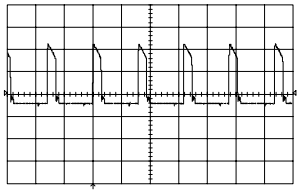
Q8009/B
2V 20us



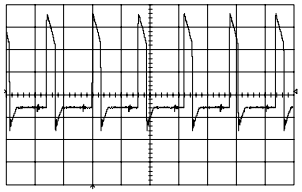
Q8010/C
2V 20us



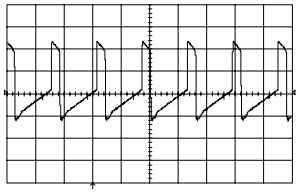
Q8018/B
5V 20us



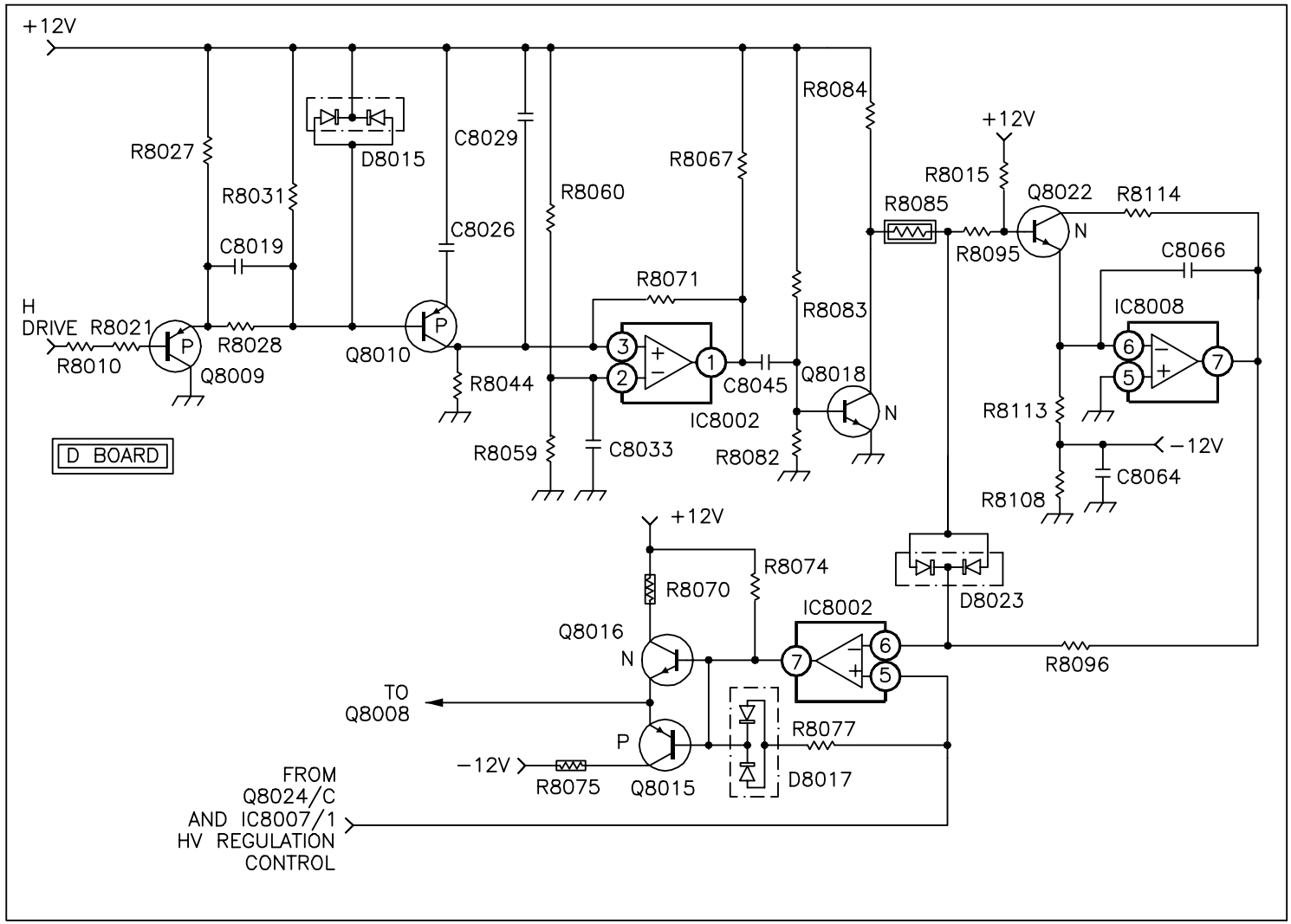
Q8022/B
2V 20us



IC8008/6
1V 20us



IC8002/6
2V 20us



HV REGULATION PWM

TVP08J32 1017 12 177 98

HV Stop 2

Overview

The purpose of the HV Stop 2 circuit is to shut down the High Voltage if the ABL voltage should become too low or if a Hold Down condition exists.

ABL

The purpose of the ABL winding of T8003 FBT is to output a voltage relative to the amount of current being drawn from the FBT. The ABL voltage gets lower as more current is drawn by the FBT. The winding at T8003/11 goes through CN8003. CN8003 has pins 5 and 6, and 3 and 4 shorted together on the plug. CN8003/4 and 5 are shorted on the board. The High Voltage circuit will not operate if this plug is removed from its connector. The ABL voltage exits CN8003/3 and goes through R8161 and R8162 before being input to Q8028.

The ABL voltage is input to Q8028/B. This voltage is normally sufficient to keep Q8028 ON, which keeps its collector voltage at 0 volts. This 0 volts is applied to IC8006 where it is compared to a 4.8 volts reference set up by the voltage divider that consists of R8110 and R8109. Since the 0 volts input at IC8006/5 is less than the 4.8 volts at IC8006/6, the output will be 0 volts at IC8006/1. This output is sent to D8026 and Q8021/B.

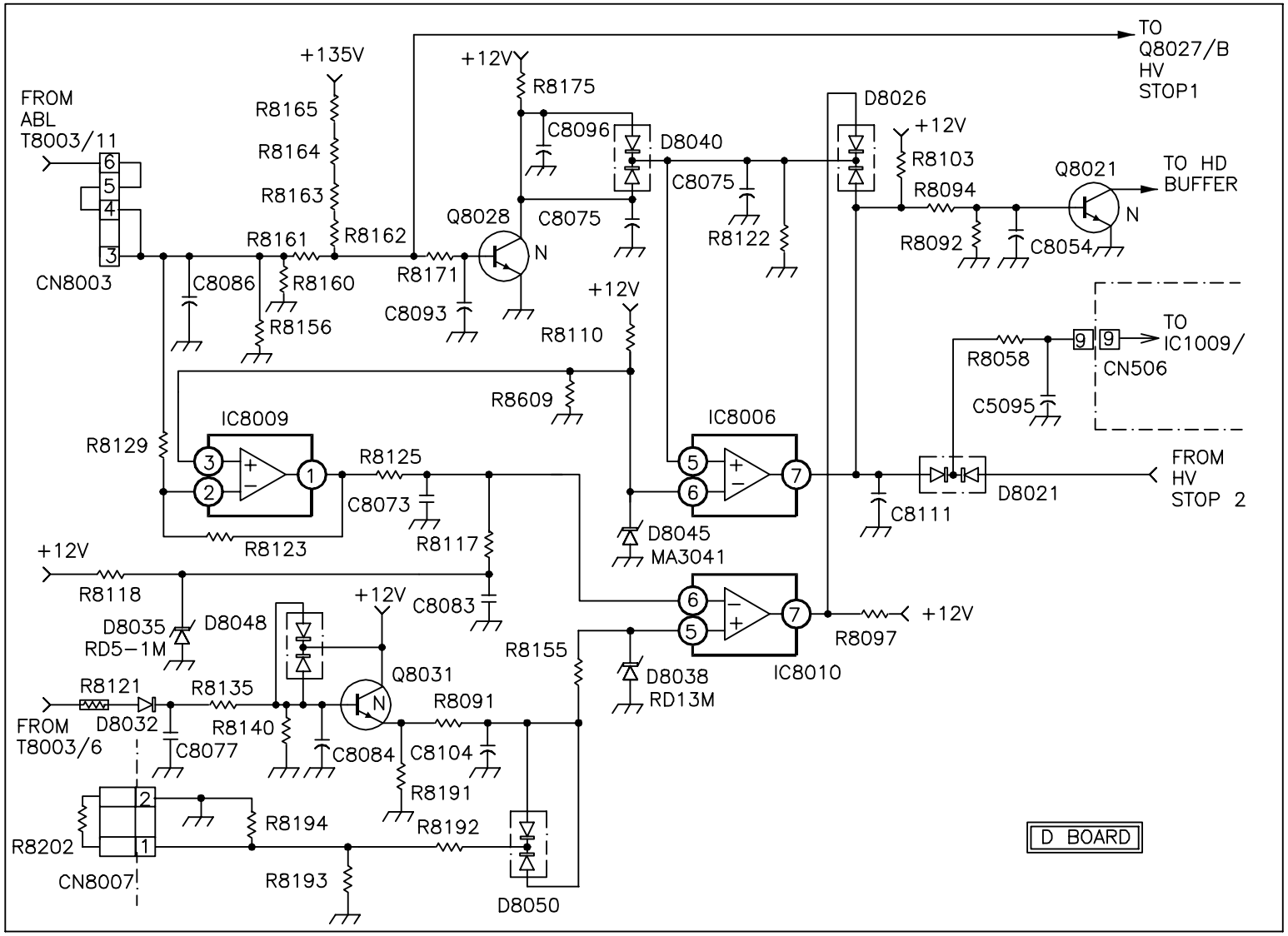
When the current draw on the FBT is too great, it will cause the voltage at Q8028/B to become low enough to turn it OFF. This causes Q8028/C to become 12 volts and this is applied to IC8006 where it is compared to a 4.8 volts reference set up by the voltage divider that consists of R8110 and R8109. Since the 12 volts input at IC8006/5 is more than the 5.9 volts at IC8006/6, the output will be 12 volts at IC8006/7. This output is input to D8026 Or Gate. When D8026 conducts, it outputs 12 volts to IC8006/5, which causes the output at IC8006/7 to become 12 volts. This acts as a latch to keep the HV Stop2 line at 12 volts once shutdown has occurred. The output is also sent to D8021 and Q8021/B. D8021 is connected to IC1009 and alerts the IC that a High Voltage failure has occurred. This causes the Timer LED to flash seven times in accordance with the self-diagnostics. When Q8021 is turned ON, it shuts down the H Drive connected to the HV Drive circuit. This shuts down the High Voltage.

Hold Down

Hold Down means that the High Voltage is shut down when the it exceeds a certain level. That level is 34 KV in this set. This is done by inputting the output of T8003/6 to a peak hold circuit consisting of D8032 and C8077. C8077 charges to hold the peak voltage present at D8032/C. This voltage passes through a voltage divider consisting of R8135 and R8140 before being buffered by Q8031. This voltage then is input to a voltage divider consisting of R8191, and the resistor network consisting of R8192, 8193, R8194 and R8202. R8202 is installed at the factory onto CN8007. It may or may not be present in the set. This resistance is set at the factory and its value is such that the set will shut down at 34 KV. The voltage created by this setup provides around 4.9 volts to IC8010/5.

The voltage input at IC8010/5 is compared to a reference voltage at IC8010/6. This reference voltage will vary between 5.1 and 6.2 volts since it is derived from the ABL signal. The ABL signal is used as a reference because the voltage from T8003/6 will vary if more current is drawn fromT8003 FBT. Since the ABL voltage also varies with current draw, it creates an acceptable reference for Hold Down. In order to create this reference, the ABL signal is input to IC8009. IC8009 is an inverting amplifier that outputs the largest signal when the most current is being drawn, which is when the ABL voltage is lowest.

If the voltage at IC8010/5 should become greater than the voltage at IC8010/6, then the output at IC8010/7 will become 12 volts. This output is input to D8026 Or Gate. When D8026 conducts, it outputs 12 volts to IC8006/5, which causes the output at IC8006/7 to become 12 volts. This acts as a latch to keep the HV Stop2 line 12 volts once shutdown has occurred. The output is also sent to D8021 and Q8021/B. D8021 is connected to IC1009 and alerts the IC that a High Voltage failure has occurred. This causes the Timer LED to flash seven times in accordance with the self-diagnostics. When Q8021 is turned ON, it shuts down the H Drive connected to the HV Drive circuit. This shuts down the High Voltage.



HV STOP 2

TVP08J35 1006 12 17 98

HV Stop 1

Overview

The purpose of the HV Stop 1 circuit is to shut down the High Voltage if the ABL voltage should become too low, if the output from the High Voltage Block regulation tap is too high, or if the +135 volt line should rise above +148 volts. The ABL circuit is identical to the one in the HV Stop 2 circuit, as it is a DHHS regulation to have two of this type in a TV.

ABL

The purpose of the ABL winding of the FBT is to output a voltage relative to the amount of current being drawn from the FBT. The ABL voltage gets lower as more current is drawn by the FBT. This voltage is input to Q8027/B. This voltage is normally sufficient enough to keep Q8027 ON, which keeps its collector voltage at 0 volts. This 0 volts is applied to IC8010 where it is compared to a 5.9 volts reference set up by the voltage divider that consists of R8106 and R8115. Since the 0 volts input at IC8010/3 is less than the 5.9 volts at IC8010/2, the output will be 0 volts at IC8010/1. This output is sent to D8021 and Q8019/B.

When the current draw on the FBT is too great it will cause the voltage at Q8027/B to become low enough to turn it OFF. This causes Q8027/C to become 12 volts. This 12 volts is applied to IC8010 where it is compared to a 5.9 volts reference set up by the voltage divider that consist of R8106 and R8115. Since the 12 volts input at IC8010/3 is more than the 5.9 volts at IC8010/2, the output will be 12 volts at IC8010/1. This output is input to D8027 Or Gate. When D8027 conducts, it outputs 12 volts to IC8010/3, which causes the output at IC8010/1 to become 12 volts. This acts as a latch to keep the HV Stop line 12 volts once shutdown has occurred. The output is also sent to D8021 and Q8019/B. D8021 is connected to IC1009 (not shown) and alerts the IC that a High Voltage failure has occurred. This causes the Timer LED to flash seven times in accordance with the self-diagnostics. When Q8019 is turned ON, it shuts down the H Drive connected to the HV Drive circuit. This shuts down the High Voltage.

High Voltage Block Tap

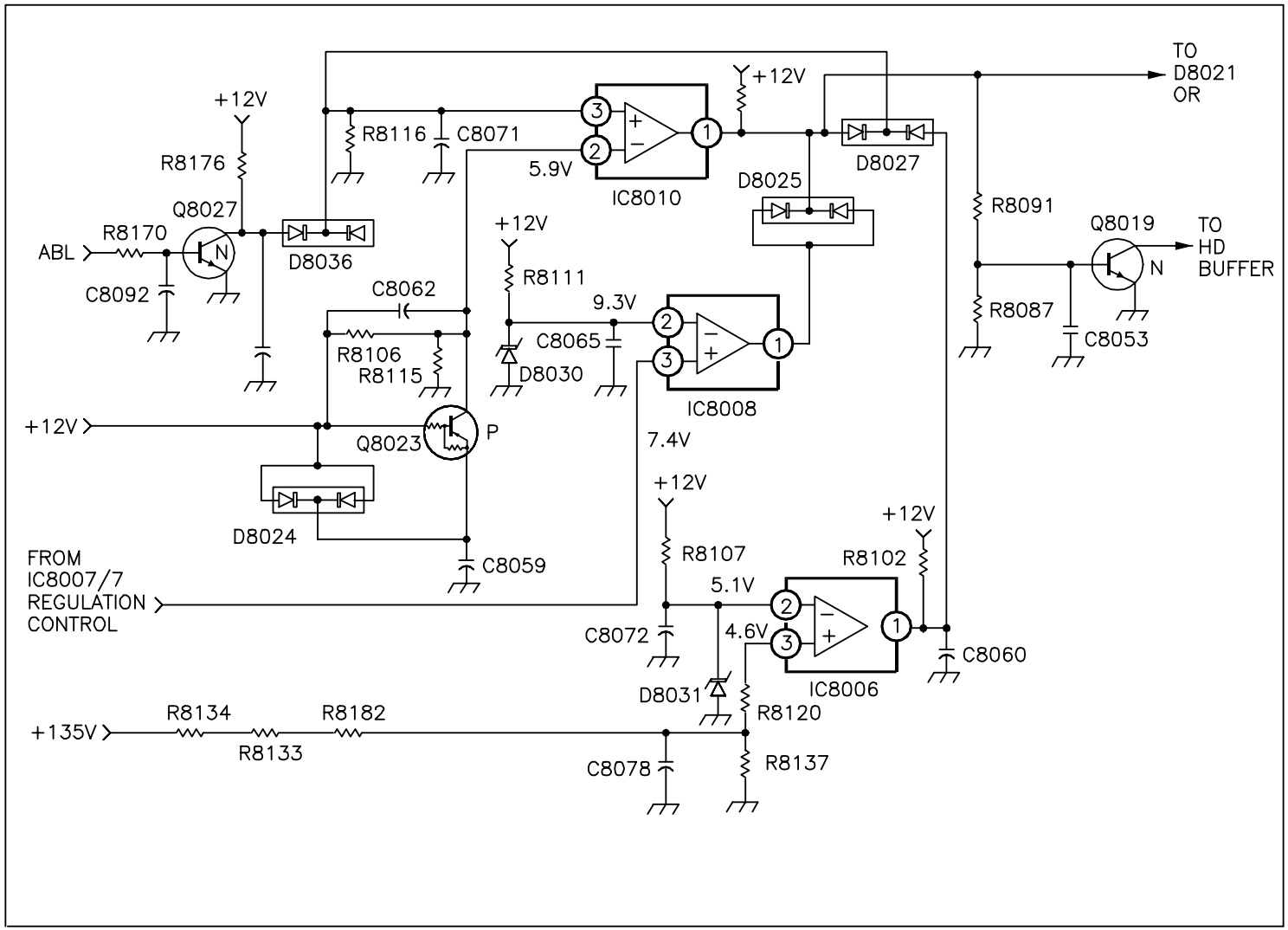
IC8008/3 receives input IC8007/1 which is the buffer for the High Voltage Block tap. It has the same voltage as the tap. This voltage is compared to a reference of 9.3 volts input at IC8007/2 and produces an output of –12 volts at IC8008/1.

If the voltage at IC8008/3 rises above 9.3 volts, the output at IC8008/1 would become +12 volts. This output is input to D8027 Or Gate. When D8027 conducts, it outputs 12 volts to IC8010/3, which causes the output at IC8010/1 to become 12 volts. This acts as a latch to keep the HV Stop line 12 volts once shutdown has occurred. The output is also sent to D8021 and Q8019/B. D8021 is connected to IC1009 (not shown) and alerts the IC that a High Voltage failure has occurred. This causes the Timer LED to flash seven times in accordance with the self-diagnostics. When Q8019 is turned ON, it shuts down the H Drive connected to the HV Drive circuit. This shuts down the High Voltage.

+135 Volt OVP

The +135 volt line goes through a voltage divider consisting of R8134, R8133, R8132 and R8137. This voltage is input through R8120 to IC8006/3 and is normally 4.6 volts. This voltage is compared to IC8006/2, which has a reference voltage of 5.1 volts input to it. Since the input at IC8006/3 is lower than the voltage at IC8006/3, the output at IC8006/1 is 0 volts.

If the +135 volt line rises above +148 volts, the voltage at IC8006/3 will become greater than 5.1 volts. This will cause IC8006/1 to output 12 volts. This output is input to D8027 Or Gate. When D8027 conducts, it outputs 12 volts to IC8010/3, which causes the output at IC8010/1 to become 12 volts. This acts as a latch to keep the HV Stop line 12 volts once shutdown has occurred. The output is also sent to D8021 and Q8019/B. D8021 is connected to IC1009 (not shown) and alerts the IC that a High Voltage failure has occurred. This causes the Timer LED to flash seven times in accordance with the self-diagnostics. When Q8019 is turned ON, it shuts down the H Drive connected to the HV Drive circuit. This shuts down the High Voltage.



HV STOP 1

TVP08J34 1016 12 17 98

Convergence Block

Overview

The convergence circuits are used to adjust all three colors so that they are all “laid on top of each other”. This is performed by sending signals to sub deflection coils that are located on each of the three yokes. This is done in the RA-4 chassis using Sony’s new digital convergence circuit. To accomplish this, this circuit uses what is called the PJED (Projection Engine Digital). The PJED performs two functions. It allows the factory or servicer to converge the set, and also allows the customer to Auto Focus the set. The Auto Focus button optimally adjusts the center and skew controls.

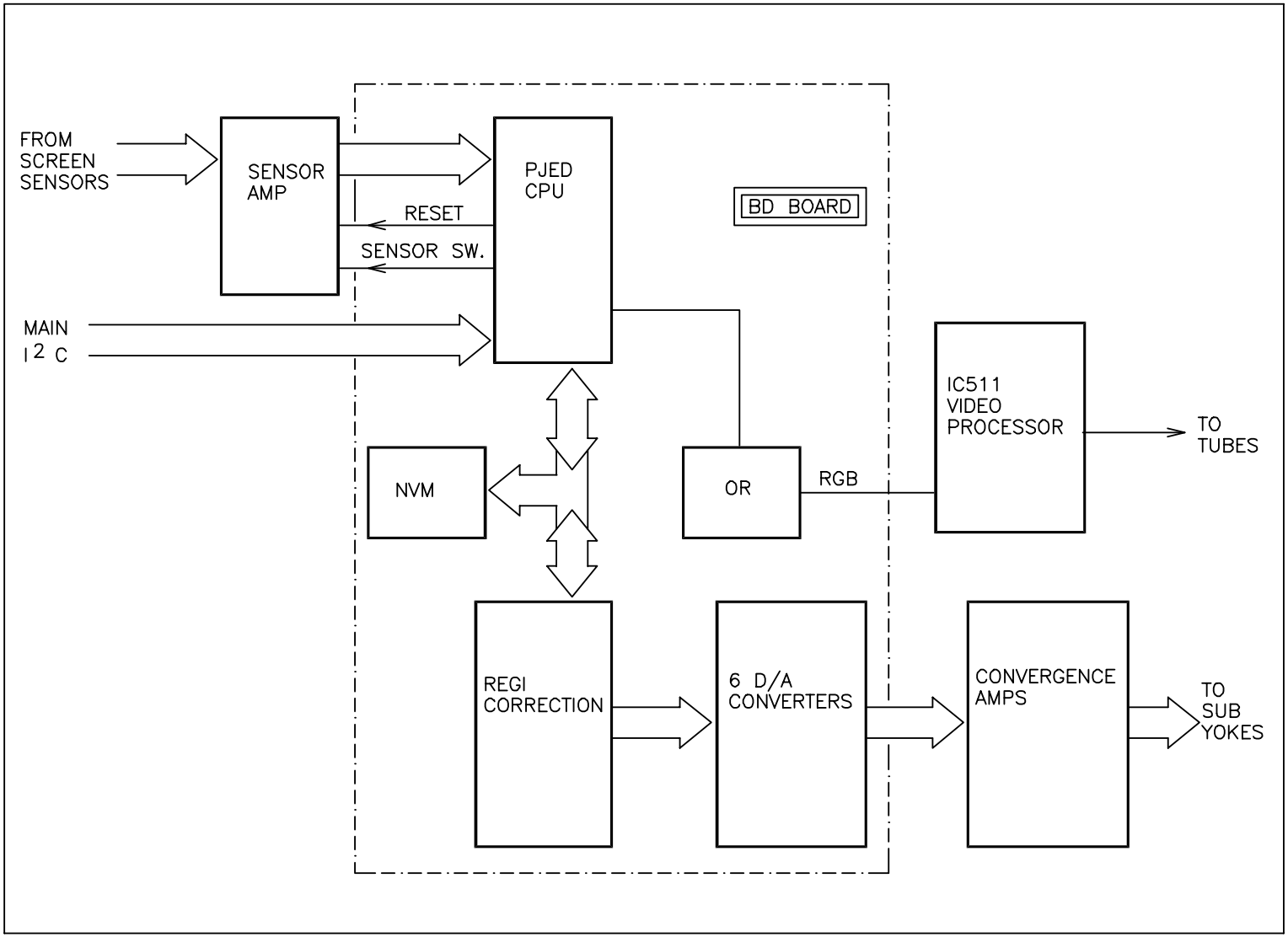
Convergence

Convergence in this set is much different than in previous chassis. It is a digital system that uses a coarse mode to “rough” in the picture, and then a fine mode to allow 81 different points to be adjusted for each color without affecting the rest of the picture. You will find this system to be much simpler and intuitive than the previous system.

This system operates by allowing the servicer to interface with the PJED using the remote. Remote commands are received by the Main CPU and sent to the PJED over the main I^2C bus. Once the CPU of the PJED receives these commands, it sends data through its own I^2C bus, referred to as the P Bus, to an IC which outputs the correct waveforms. These waveforms are output to the Sub Deflection amplifiers and applied to the sub yokes.

Auto Focus (Auto Registration)

The Auto Focus button on the front of the set allows the customer to adjust the skew and centering of the three colors at the touch of a button. When Auto Focus is selected, the PJED OSD sends out signals, which are sent through a level compensation circuit to the video processor to be displayed on the screen. The patterns displayed on the screen are received by a number of sensors located around the outside of the screen. These sensors output a current proportional to the amount of light received. The level compensation circuit was used earlier because the sensors are not equally sensitive to different colors of light. The output from the sensors is input to a current to voltage converter. The signal from the I/V Converter is input to a peak detect circuit whose output is sent to an A/D converter in the PJED. While this process is going on, the PJED is changing the waveforms to the sub deflection circuit. This varies the intensity of the light that strikes the sensors. The CPU will determine when the output from the sensors equals the stored values of the optimum picture. This means that it does not optimize the picture by itself, but looks in memory for the stored value. This value is set at the factory or by a servicer who presses the Auto Focus button in the service mode.



CONVERGENCE BLOCK

TVP08J83 1042 12 21 98

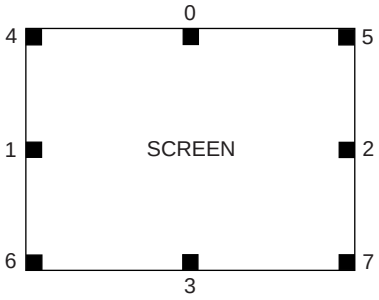
Sensor Amp

Overview

The sensor amplifier is used when the customer or servicer presses the Auto Focus button. It amplifies the signal from the sensors and outputs the signal to the D/A converter on the BD board.

Auto Focus

The Auto Focus system works by adjusting centering and skew convergence data to receive a memorized optimum level. The servicer can set this level by performing the Auto Focus function in the Service Mode. This means that the system does not pick a new optimum value when the customer uses it but rather changes centering and skew adjustment data to get an optimum sensor reading. The drawing below shows the position of the sensors around the screen.

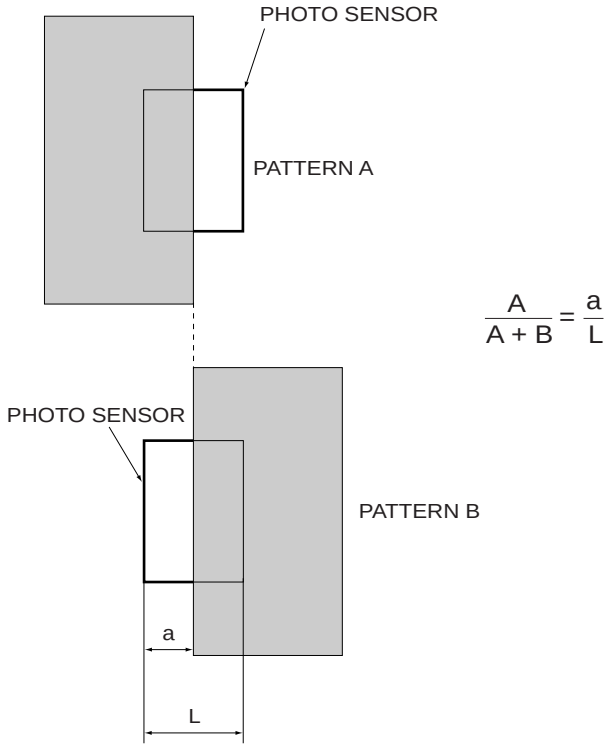


0 : UPPER SENSOR
1 : LEFT SENSOR
2 : RIGHT SENSOR
3 : LOWER SENSOR
4 : UL SENSOR
5 : UR SENSOR
6 : LL SENSOR
7 : LR SENSOR

When Auto Focus button is pressed Pattern A and B are output in succession over top of the sensors. Pattern A is offset to the left of the sensor and Pattern B is output to the right of the sensor.

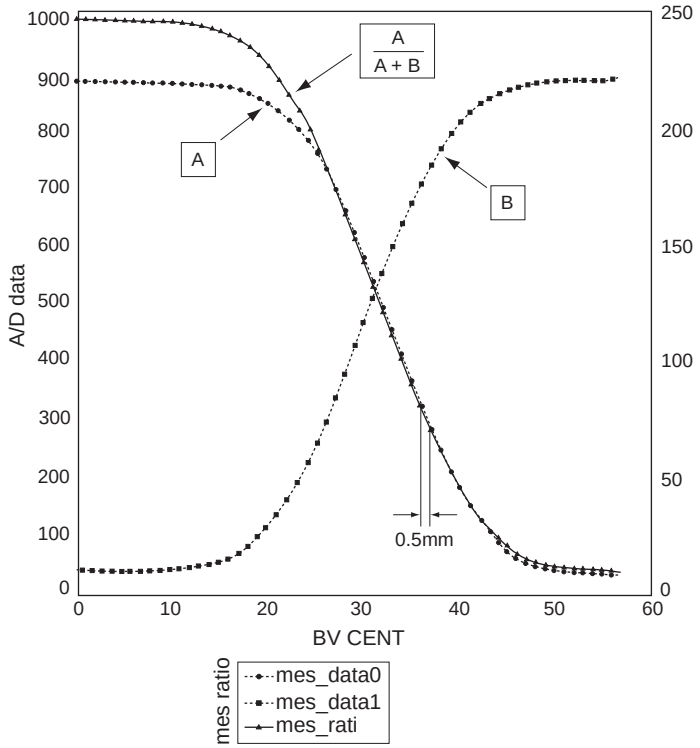
[OVER VIEW]

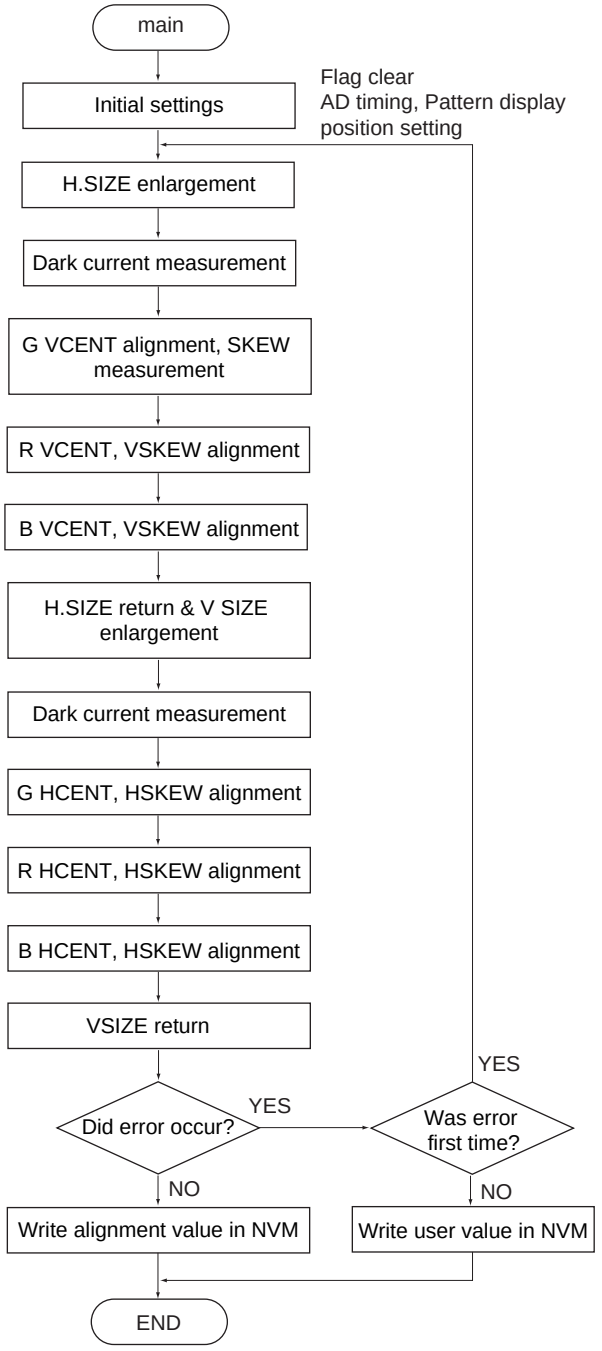
1. MEASUREMENT PRINCIPAL



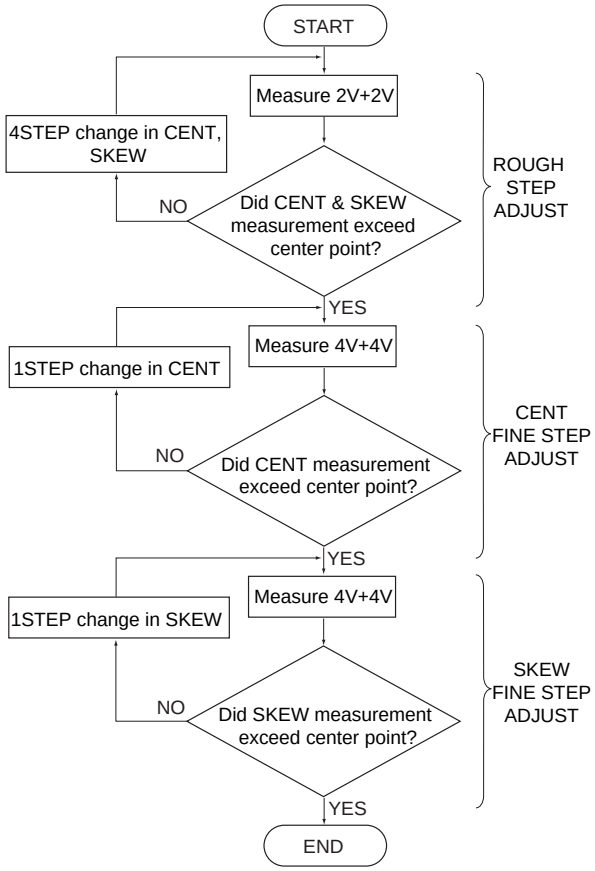
$$\frac{A}{A+B} = \frac{a}{L}$$

Varying the input to the convergence amplifiers changes the pattern. The table below shows that the A and B patterns are output while the convergence data is changed. The changing of this data changes the convergence amplifiers input. The X axis shows the changing of the convergence data and the Y axis shows the value of the data output by the sensor amplifier. The optimum value of the data is shown where the curves cross. This data is memorized if the Auto Focus button is pressed in the Service Mode. When the customer uses the Auto Focus button the system will change the convergence data to receive the optimum value at the A/D converter.



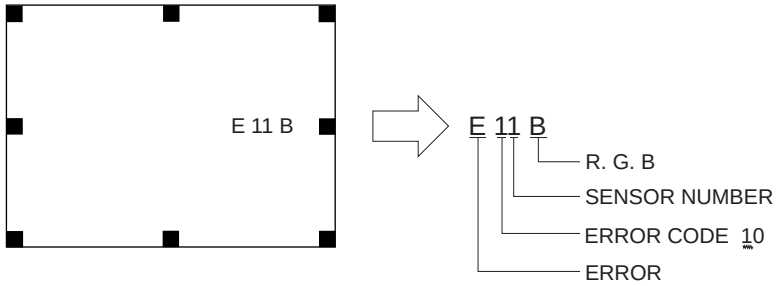


The flowchart on the previous page shows the sequence of operations for the Auto Focus operation. The first operation is to set the initial settings. Then the H size is changed. This is done because the sensors are outside of the screen. After the H size is enlarged, a dark current measurement is performed. This means that a reading of the sensors is taken with output from the tube in order to establish a room brightness offset. This measurement is subtracted from the readings taken later. After the V centering and skew adjustments are performed for each color, the H size is returned to normal and the V size is enlarged. A dark current measurement is taken again and then H centering and skew adjustments are done. When these adjustments are complete, V size is returned to normal. If an error occurred, the process will be repeated. If the error is returned a second time then an error code is given.



The flowchart below left shows the steps taken during the adjustment portion of the previous flowchart. As these adjustments are performed, the convergence data values for centering and skew are changed for each color. This data is measured until the data center point or optimum value is measured. When this point is reached the system moves on to the next step. If an error occurs the cycle repeats. If an error occurs the second time then it puts an error code on the screen.

The error system works slightly differently in the Service Mode. If an error occurs while running Auto Focus in the Service Mode, an error will be displayed immediately instead of repeating the adjustment and displaying the error when completely finished. An error like the one below shows the type of error that would occur if the sensor 1 received a low output level for blue.



* Error code will be displayed on center of screen for 3 seconds.

The following table shows the errors that may occur. You should note here that if the green tube is replaced it is very important that the green yoke be placed so there is no tilt. If it is not placed correctly, a repetitive “80” can occur.

[ERROR CODE LIST]

ERROR CODE	DISCRIPTION	NOTE
00	No Error	
10	Sensor Output Level Low	* Check wiring, beam position, sensor.
20	Sensor Output Level High	* Check OP-amp circuit.
30	Adjustment Loop Counter Overflow	0 : “ CENT V ” 1 : “ CENT H ” 2 : “ SKEW V ” 3 : “ SKEW H ”
40	Regi Data Overflow	Same as Loop Counter Overflow
50	Regi Data Overflow	Same as Loop Counter Overflow
60	Offset Overflow	Same as Loop Counter Overflow * Check beam position. If need, adjust “ PWM2 ” for H error, “ V CENT (main) for V error. * “ PWM2 ” is usually 34 or 36.
70	Offset Overdrow	Same as Counter Overflow * Check beam position. If need, adjust “ PWM2 ” for H error, “ V CENT (main) for V error.
80	Green “ V SKEW ” too tilt	* Adjust Green beam righ or left sensopr, or Green DY tilt.

* 60, 70 or 80 appears only in Service Mode.
* In case of multiple error, last error is displayed.

(EXAMPLE)

11B : Left sensor Blue level low. (Left sensor circuit may be faulty.)

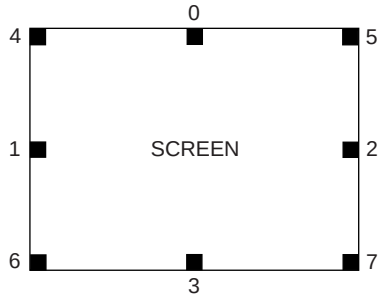
61R : “ RED CENT H ” offset overflow. (“ PWM2 ” may be required adjusting.)

Circuit Description

The sensor amplifier is responsible for taking the amount of light received by the sensors and outputting a DC value to the PJED CPU to represent the amount of light received. The optimal value achieved is memorized during the Auto Focus function in the Service Mode.

As the patterns of flashing light are seen on the screen, the outputs of the sensors are input to the A board at CN524, CN525 and CN501. These sensors are applied to IC1601 and IC1604. These ICs are current to voltage converters. They are required because the sensors output a current proportional to the amount of light they receive.

The outputs from IC1601 and IC1604 are output to peak hold circuits. These circuits consist of IC1605 and IC1606 and buffer transistors Q1609 through Q1616. To ensure precise measurements, each sensor also has its own reset line that grounds the peak hold circuit every vertical blanking pulse. The top, left, right and bottom sensors' outputs are applied directly to the BD board. The four corner sensors are applied to a switch. The switch is necessary because the PJED CPU only has six A/D inputs. Since we do not need to use the corner left and right sensors at the same time, they are switched. Pulses from CN1701/12 from the BD board are responsible for switching the sensors. The two sensors selected then have their outputs applied to the PJED CPU.



0 : UPPER SENSOR
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3 : LOWER SENSOR
4 : UL SENSOR
5 : UR SENSOR
6 : LL SENSOR
7 : LR SENSOR

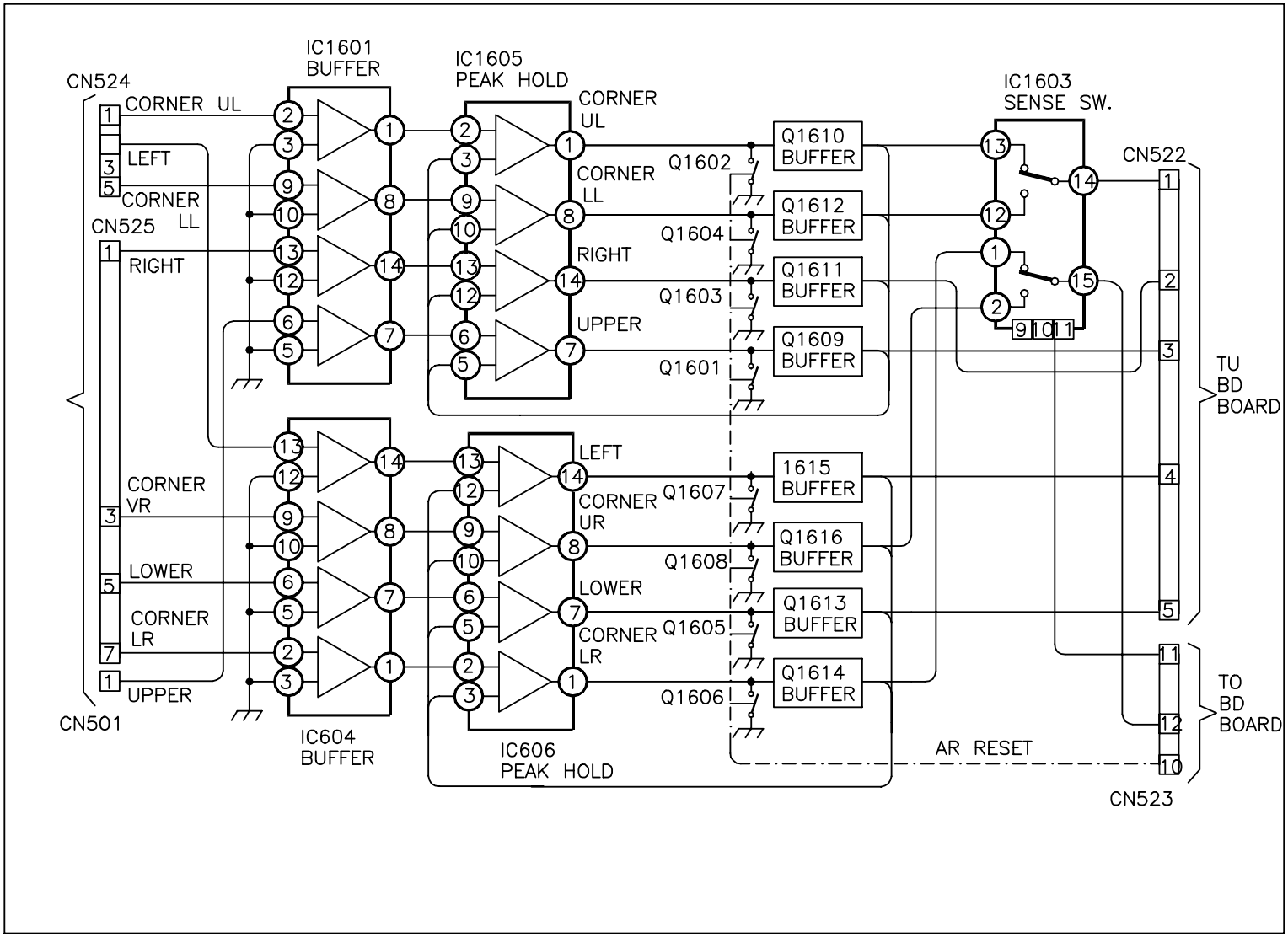
The picture above shows the sensor locations by number. The following are the formulas used to perform the centering and skew adjustments.

V Center = 1+2

V Skew = 1-2

H Center = 0+3+(1+2)/2

H Skew = 0-3+(4+5-6-7)/4



SENSOR AMP.

TVP08J82 1040 12 18 98

BD Input

Overview

The BD Input circuit is used to control the waveforms that will be output by the BD Output circuit. It also controls the Auto Focus by generating an OSD signal and receiving the sensor's input while adjusting the convergence data to vary the output waveforms. This circuit determines what the convergence data was when the optimal signal is received from the sensors.

Digital Convergence

This set uses Sony's new digital convergence system. This system contains two types of adjustments. They are classified as rough and fine adjustments. These adjustments are done in the PJED mode of the Service Mode. This mode uses a built in pattern generator so the servicer does not need to carry one.

Rough Adjustments

The rough adjustments are just like some of the adjustments used in the previous Sony projection sets. It uses the major adjustments in the old system. The table below shows which adjustments are available for each color in the rough mode.

SUB DEFLECTION ADJUSTMENT ITEM

Adjustment O : Yes – : No

Display	Adjustment item	Adjustment type					
		GH	GV	RH	RV	BH	BV
CENT	CENT	O	O	O	O	O	O
SKEW	SKEW	O	–	O	O	O	O
SIZE	SIZE	O	O	O	O	O	O
LIN	LIN	–	–	O	–	O	–
KEY	KEY	–	–	–	O	–	O
PIN	PIN	–	O	–	O	–	O

Centering - Changing the centering control causes all of the horizontal lines to move away from the center at the same rate. It is the first adjustment that should be made when aligning convergence.

Skew – Changing the skew data tilts the picture on its vertical or horizontal axis.

Size - The effect of the horizontal size control is to change the box width from the center outwards.

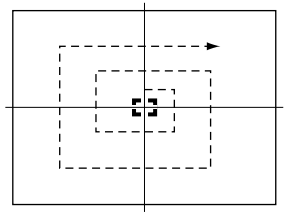
Linearity - The linearity control changes the linearity or the width of the boxes on the left side of center as compared to the right. While changing the linearity control, if the box width on the right side were getting smaller the box width on the left side would be getting larger.

Key – The key control is used to adjust keystone distortion. It works by tilting the left side of the line towards the top while tilting the lines on the right side towards the bottom.

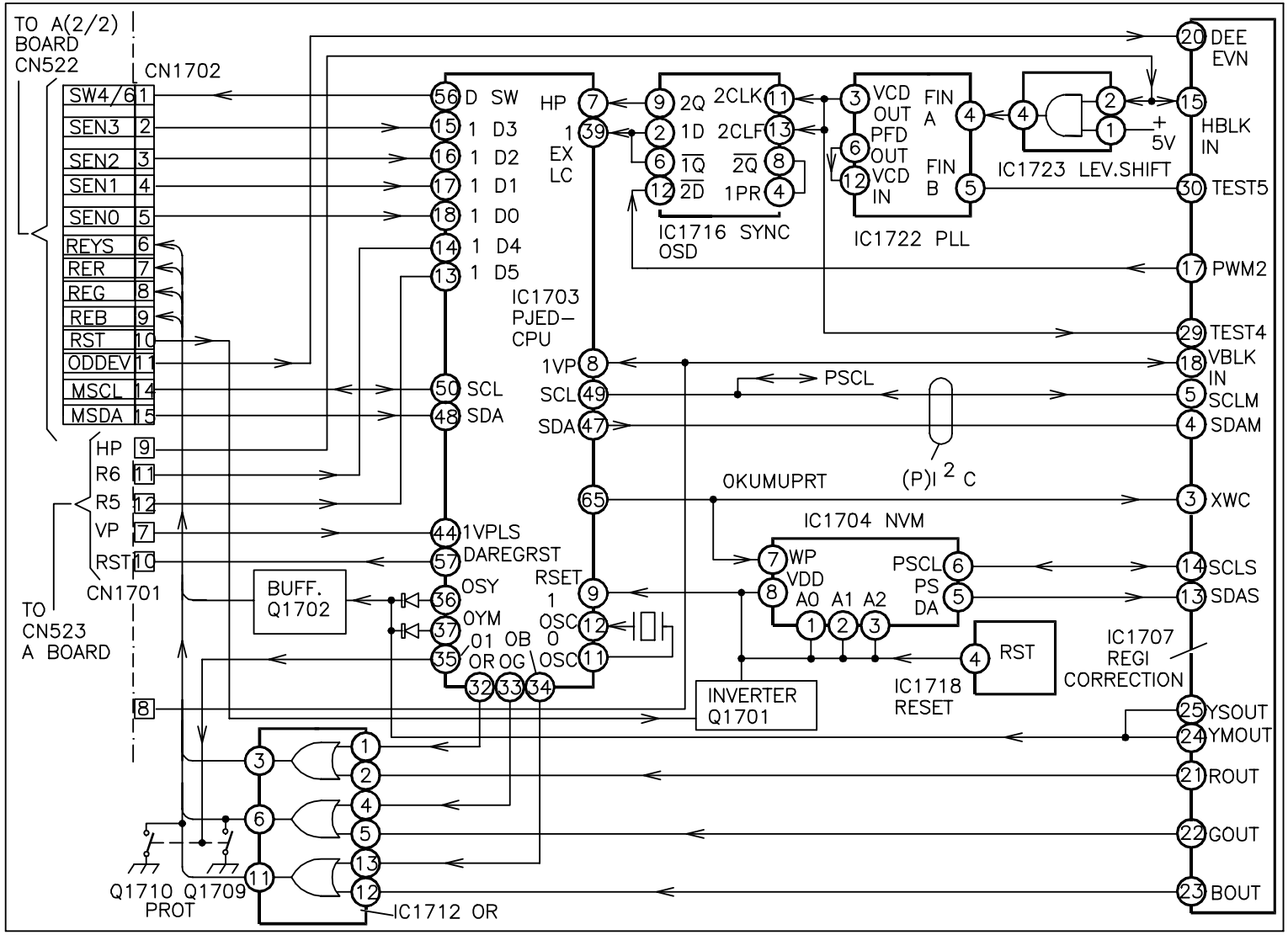
Pin – The pincushion control is used to adjust pincushion distortion out of the picture. Pincushion causes the top and bottom of the picture to bow in opposite directions.

Fine Adjustments

Once you have gotten the best picture you can by using the rough mode, you can adjust the rest of the picture using the fine mode. When the fine mode is selected a cursor appears on the screen. This cursor can be moved to anyone of 81 different points. These points are reached by moving the cursor in steps around in the vortex pattern shown below. All the points are at intersections of the horizontal and vertical lines of the self-generated crosshatch pattern.



The cursor color can be changed to any of the three colors. When you adjust a point you select the point and the color of the cursor. Then by using the joystick on the remote you can move the point inside the cursor up, down, left or right. You repeat this process for all the points that need to be adjusted.



BD INPUT (PJED)

TVP08J43 1022 12 21 98

BD Output

Overview

The BD Output takes the digital outputs from IC1707 Regi Correction and converts them to analog signals which are then output from the BD board to the Convergence Amps on the D board. (Not shown)

IC1707 Regi Correction

IC1707 Regi Correction receives sync and data signals that allow it to output the correct waveforms to control the convergence of the three tubes. These signals are output in digital format along with BCLK (Bit Clock) and WCLK (Word Clock). The HBLK is output from IC1707/26 for use as a compensation signal for blue to reduce corner distortions. There are six digital data streams output from IC1707 Regi Correction to the D/A Converters.

The Red Vertical Output is input to IC719/14 RSI and IC715/14 RSI. The analog signals are output from pin 6 of each of these ICs. They are combined and input to IC1705/2. IC1705 is a filter amplifier which will output the RV signal to CN523 on the A board.

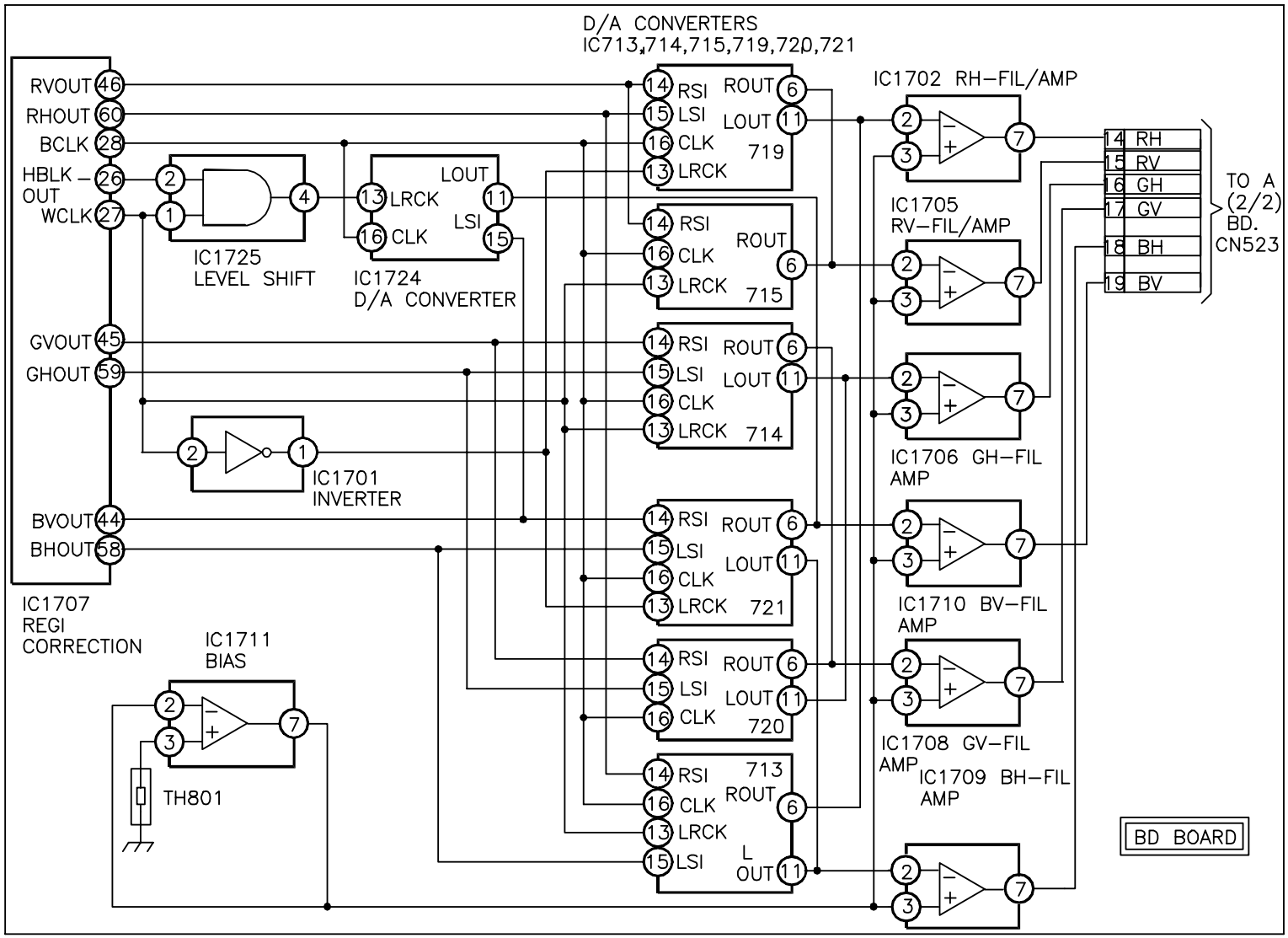
The Red Horizontal Output is input to IC719/15 LSI and IC713/14 RSI. The analog signals are output from IC719/11 and IC713/6, combined and input to IC1702/2. IC1702 is a filter amplifier outputs the RH signal to CN523 on the A board.

The Green Vertical Output is input to IC714/14 RSI and IC720/14 RSI. The analog signals are output from pin 6 of each of these ICs. They are combined and input to IC1708/2. IC1708 is a filter amplifier which outputs the GV signal to CN523 on the A board.

The Green Horizontal Output is input to IC714/15 LSI and IC720/15 LSI. The analog signals are output from IC714/11 and IC713/11. They are combined and input to IC1706/2. IC1706 is a filter amplifier which outputs the GH signal to CN523 on the A board.

The Blue Vertical Output is input to IC721/14 RSI and IC724/15 LSI. The analog signals are output from IC1721/6 and IC1724/11. These two signals differ because the LRCK signal of IC1724 is not the WCLK as it is in IC1721. The different signal is used to compensate for corner distortion problems. These different outputs are still combined and input to IC1710/2. IC1710 is a filter amplifier which outputs the BV signal to CN523 on the A board.

The Blue Horizontal Output is input to IC721/15 LSI and IC713/15 LSI. The analog signals are output from IC721/11 and IC713/11, combined and input to IC1709/2. IC1709 is a filter amplifier which outputsx the BH signal to CN523 on the A board.



BD OUTPUT (REGI-CORRECTION)

TVP08J44 1023 12 22 98

Convergence Out

Overview

The Convergence Out circuit amplifies the horizontal and vertical convergence signals that are output by the BD Output circuit for each color. The circuit below shows the IC5005 Convergence Amp. IC5006 is another Convergence Amp. It is not shown here because its circuitry is identical to the IC5005 circuit.

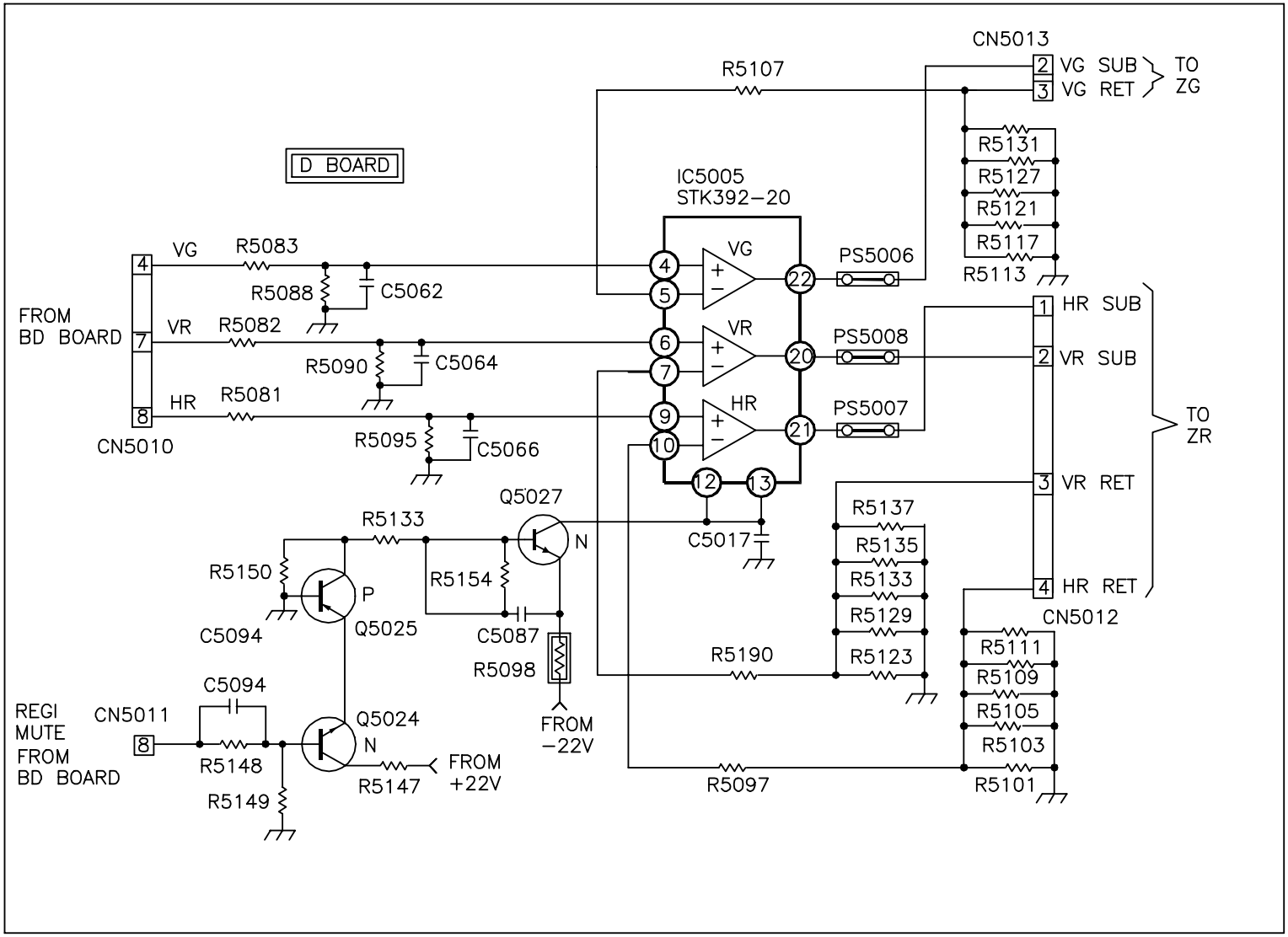
Regi Mute

When the set is first turned ON, a Regi Mute signal is required because the BD board outputs a High signal from the six convergence outputs for three seconds. If all Highs were output from the BD board simultaneously, it would probably result in a problem on the +/- 22 volt lines.

When the set is initially turned on, a LOW is output from the BD board to the A board. The A board transfers this LOW through CN5011/8 to the D board. This LOW is applied to the base of Q5024, keeping it OFF. If Q5024 is OFF, then Q5025 and Q5027 are also OFF. This causes IC5005/12 and 13 Mute to be 0 volts. This will mute IC5005 and it will not output any signals. After three seconds the Regi Mute output will go HIGH. This causes Q5024 to turn ON. This will cause Q5025 and Q5027 to turn ON. This places –19 volts on IC5005/12 and 13 which enables the outputs of IC5005.

Convergence Amp

IC5005 Convergence Amp contains three amplifiers. Each of these amplifiers contains two inputs, a Non-inverting and Inverting, and one output. If we look at the first amplifier inside IC5005 we see that the vertical green signal is input to IC5005/4 Non-inverting Input. It is output from IC5005/22 through PS5006 to the Green Vertical Sub Yoke. The signal passes through the yoke and is returned to IC5005/5 Inverting Input via R5017. The other two amplifiers in IC5005 work exactly like the circuit described above.



CONVERGENCE OUT

TVP8J16B 989 12 22 98

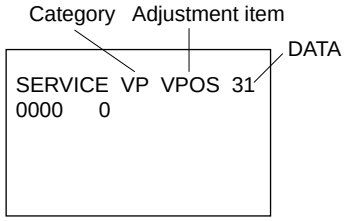
Service Mode

Overview

The normal service mode has not changed greatly. It is still entered the same way, but now the registration section is completely different. In this section we will concentrate on the new registration system and how adjustments are done in the PJED Mode.

Normal Service Mode

Entering service mode on the RA-4 chassis is done exactly the same way as in previous chassis. With the power OFF, press **Display Channel 5 Vol+ Power** on the remote. Be sure to press the buttons within one second of each other. After this is done, the following display will appear on the screen over the picture with the letters in green.



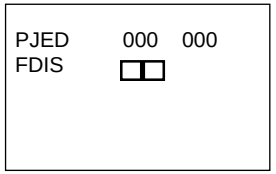
This data follows the same format as previous models. The category, adjustment item and data are shown.

Remote Functions

- The adjustment item can be changed up or down by pressing the **1 or 4** buttons.
- The category can be changed by using the **2** and **5** buttons.
- The data can be changed up or down by using the **3** or **6** buttons.
- Data values stored in memory can be read by pressing **0** and **Enter**.
- Data values can be written to memory by pressing **Muting** and **Enter**.

PJED Mode

If the 5 button is pressed after the unit enters the test mode, you will notice that the letters indicating the service adjustments have changed from green to white and the following will appear on the screen:

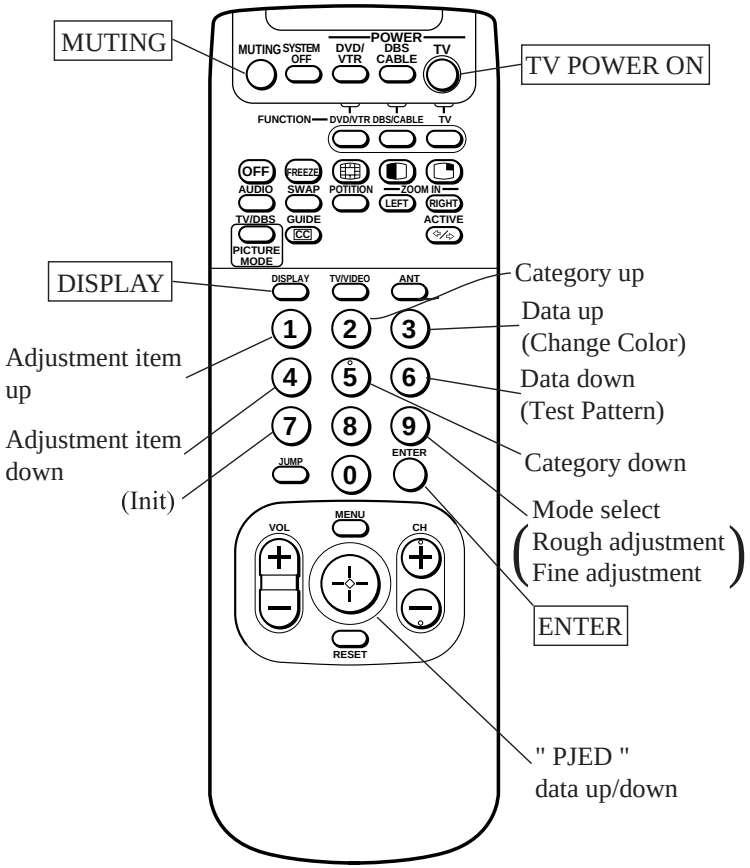


Remote Functions

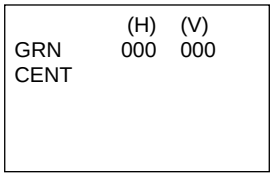
The PJED mode is for adjusting convergence. When this display appears, you have entered into the registration adjustment section. The buttons on the remote will no longer perform the same functions, but will perform the functions shown in parenthesis on the remote drawing.

- The **1** and **4** buttons on the remote are still used to change the adjustment items.
- The **2** and **5** buttons still can be used to change categories. If you change categories, you will no longer be in the PJED mode.
- The **3** button is used to change colors. Each time the button is pressed the color to be adjusted will change from green to blue to red and back to green and so on.
- The **6** button is used to display the self-generated test pattern. Each time it is pressed, the pattern will change from crosshatch over the picture to dots over picture, to crosshatch over black to dot over black, then back to OFF.
- When the **7** button is pressed, INIT will show up in green on the screen. If **Enter** is pressed, the sub deflection circuit will be turned OFF. In order to turn it back ON, you must press **0** and **Enter**.
- The **9** button is used to change between coarse and fine convergence adjustments.
- The **Muting**, **0** and **Enter** buttons perform their same functions.

• ADJUST BUTTONS AND INDICATOR



- Moving the joystick changes data. Moving the joystick up or down changes the V data, and moving the data left or right will change the H data. Data that does not have separate V and H adjustments can be adjusted by moving the joy stick up or down or left or right.



Adjustment

Let's look at how we would perform adjustments from a worst-case scenario. An example would be if all of the data were lost on the BD board since that is where all convergence data is stored.

If this scenario is encountered, the first thing that should be done is to enter the service mode got the PJED section and enter the default values that are in the service manual. After doing this, press **Muting** and **Enter** to save these values. The first 15 of these adjustments, with the exception of 13 PWM2, will not have to be adjusted after this. The default value will remain.

Next cover the blue and red tubes so only green can be seen. We use green as a reference for the other two colors so it must be correctly adjusted first. Press 6 on the remote so that a crosshatch can be seen over a black screen. If the V Size, H Size, V Pos and H Pos are not correct, use the **2** button to enter the VDSP category and make the necessary changes to those adjustments. If these adjustments are correct, then you can do the coarse adjustments for green.

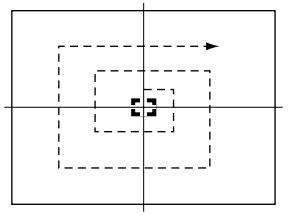
There are two sets of adjustments for convergence, coarse and fine. The coarse adjustments are similar to older convergence systems. The fine adjustments are the new point type. The coarse adjustments must be done first. You should try to achieve the best picture possible using these adjustments. The table below shows the adjustments available for each color:

SUB DEFLECTION ADJUSTMENT ITEM

Adjustment O : Yes – : No

Display	Adjustment item	Adjustment type					
		GH	GV	RH	RV	BH	BV
CENT	CENT	O	O	O	O	O	O
SKEW	SKEW	O	–	O	O	O	O
SIZE	SIZE	O	O	O	O	O	O
LIN	LIN	–	–	O	–	O	–
KEY	KEY	–	–	–	O	–	O
PIN	PIN	–	O	–	O	–	O

Once the coarse adjustments have been completed, it is time to perform the fine adjustments. Press 9 on the remote to enter the fine adjustment mode. The display will blank and a cursor will appear in the center of the screen.



Pressing the 1 or 4 buttons moves the cursor on the screen. The cursor will follow the vortex pattern shown in the drawing above. There are 81 separate points that can be adjusted. You can now adjust each point by moving the joystick on the remote. The point in the center of the cursor will be moved in the direction the joystick is moved. Continue to adjust each point until your green picture is correct. Repeat this procedure for red and blue and lay those pictures over green.

Auto Registration Adjustment

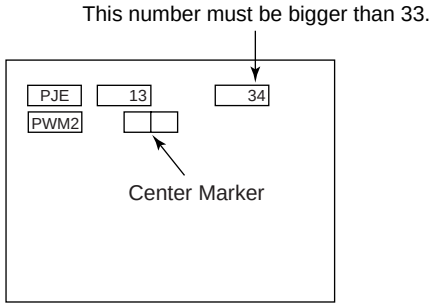
The Auto registration system or Auto Focus customer adjustment **does not optimize the centering and skew each time it is pressed. What it does is memorize the settings for an already optimized picture and adjust convergence back to that setting.** This means that when the customer presses the Auto Focus button on the front of the set, the function performed adjusts the center and skew controls for each color so that it matches what was previously memorized. The factory or the servicer sets the memorized information by pressing the Auto Focus button while in the test mode.

Therefore, whenever a servicer adjusts convergence, they should press the Auto Focus button after, and only after, they have a perfect picture. Generally this would be the last thing done before finishing the repair. It is also important that this be done every time that adjustment is made if Auto Focus is not run in the test mode

Auto Registration Offset Adjustment

This adjustment may need to be performed if errors occur while doing Auto Focus or the picture produced is off center horizontally.

Confirm that the OSDH value is 32. Go to the PWM2 adjustment in the PJED mode. A djust the center marker to the horizontal center of the picture (Between the O and the N in the SONY log). However, the data value must be above 33 in order for the set to work correctly. If the value is below 34, set it to 34 even if the marker is slightly off center.



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Service Bulletin
TV Products

CSV-1

Model: KP-53XBR200, KP-61XBR200 **No.** 378

Subject: Picture Is Partially Sandy Or Grainy. **Date:** November 2, 1996

Symptom:
(134X)

Dealers and sales personnel have recently advised us that the new Videosopa XBR models (KP-53XBR200 and KP-61XBR200) may exhibit a partially sandy or grainy picture. This occurs when the signal is sourced through component, S-video, or composite inputs and appears to happen most often with digital satellite systems, where the signals tend to be highly compressed. Generally, poor signal quality is responsible for grainy picture characteristics on most TVs. On these 2 models the symptom is most apparent when the Vivid mode is used, as this mode enhances the deficiencies of a poor signal.

Solution:

Use the service mode to change the settings of 2 data registers as follows:
1- Make sure the TV is OFF, then enter service mode by pressing the following keys on the remote commander in sequence: DISPLAY → 5 → VOL + → TV POWER.

2- Press the "2" button until the selected category is **3DCM 5**.

3- Press the "1" button until the selected adjustment item is **YNRL**.

4- Press the "6" button to change the data from "1" to "0".

5- Press the MUTE button (the word WRITE appears).

6- Press the ENTER button (the word WRITE turns red in color).

7- Press the "1" button until the selected adjustment item is **CNRL** (the category should still be 3DCM 5).

8- Press the "6" button to change the data from "1" to "0".

9- Press the MUTE button (the word WRITE appears).

10- Press the ENTER button (the word WRITE turns red in color).

11- Turn off the set's power. Re-enter the service mode and confirm that the new data you entered has been accepted. Finally, return the set to normal mode by turning off the power, followed by turning the power on again.

12- Inform the customer that the best picture quality for the typical household will be obtained when using the Standard, Movie, Game, or PRO modes.

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Service Bulletin
TV Products

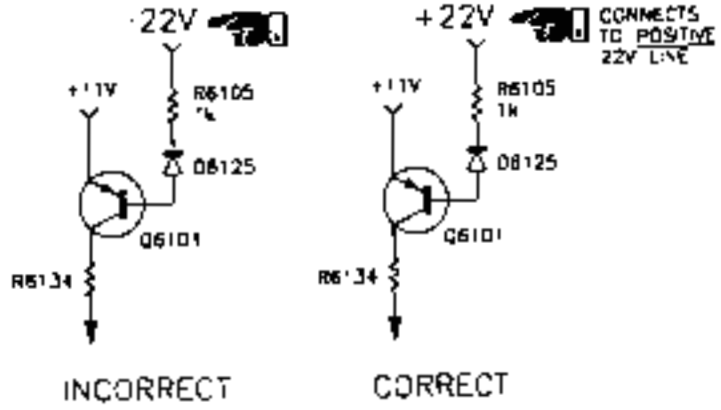
CSV-1

Model: KP-53XBR200, KP-61XBR200 **No.** 382

Subject: Service Manual Correction D6125 **Date:** November 17, 1998

Symptom:
(1XXX) D1255 on the C Board page 128 schematic location F-14 is shown connected to the -22-volt line. This is incorrect.

Solution: The schematic connection for D6125 should be between the base of Q6101 and the +22V line.



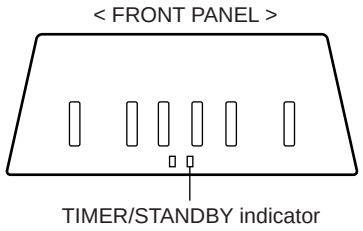
Protection Block

Overview

The RA-4 chassis employs a Self-Diagnostic system that uses the Timer LED and an on screen menu to help indicate where the problem with the set has occurred. Generally you will have to use the flashing LEDs since the set will be shut down. In order to turn the set off once shutdown has occurred, AC power must be disconnected.

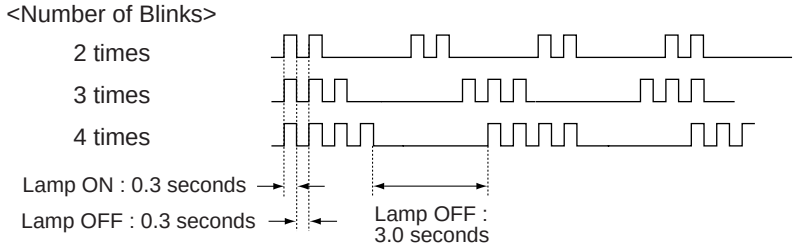
Diagnostic Indication

When a problem occurs that causes shutdown, the Timer LED may blink in a pattern as shown below:



•EXAMPLE

<Diagnosis Items>
- +B overcurrent
- +B overvoltage
- Vertical deflection stop



The number of times the LED blinks may correspond to that shown in the following table:

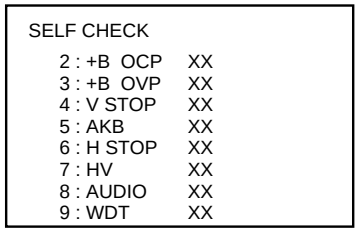
Diagnosis item	Standby/ sleep lamp, Number of blinks	Self-diagnosis screen display, Diagnosis item:Results
• Power not ON	Not lit	
+B OCP detection	LED blinks 2 times	2 : +B OCP XX
+B OVP detection	LED blinks 3 times	3 : +B OVP XX
V detection	LED blinks 4 times	4 : V STOP XX
AKB detection	LED blinks 5 times	5 : AKB XX
H detection	LED blinks 6 times	6 : H STOP XX
HV abnormality detection	LED blinks 7 times	7 : HV XX
Audio abnormality detection	LED blinks 8 times	8 : AUDIO XX

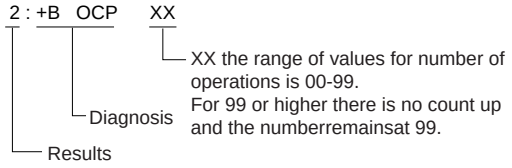
∗ : XX the range of values for number of operations is 00-99. For 99 or higher there is no count up and the number remains at 99.

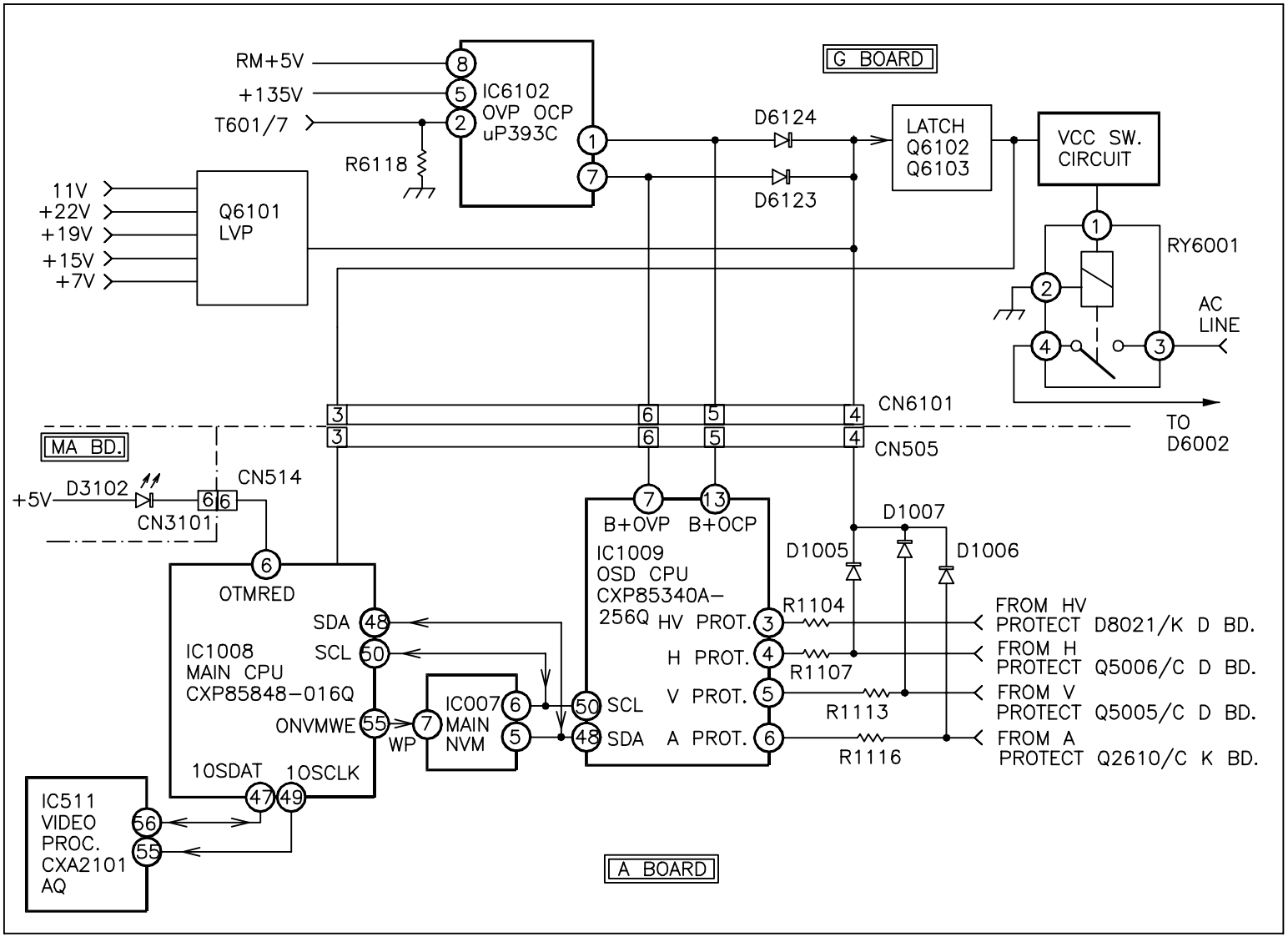
If the problem is intermittent and you can get the set to operate, you can display a menu showing the number of times failures have occurred. This is done by pressing the following sequence of buttons on the remote.

Display Channel 5 Vol - Power

The display will look as follows.







PROTECTION BLOCK

tvp08j48 1026 12 18 98

This display can be cleared by pressing **8 and Enter** in this mode.

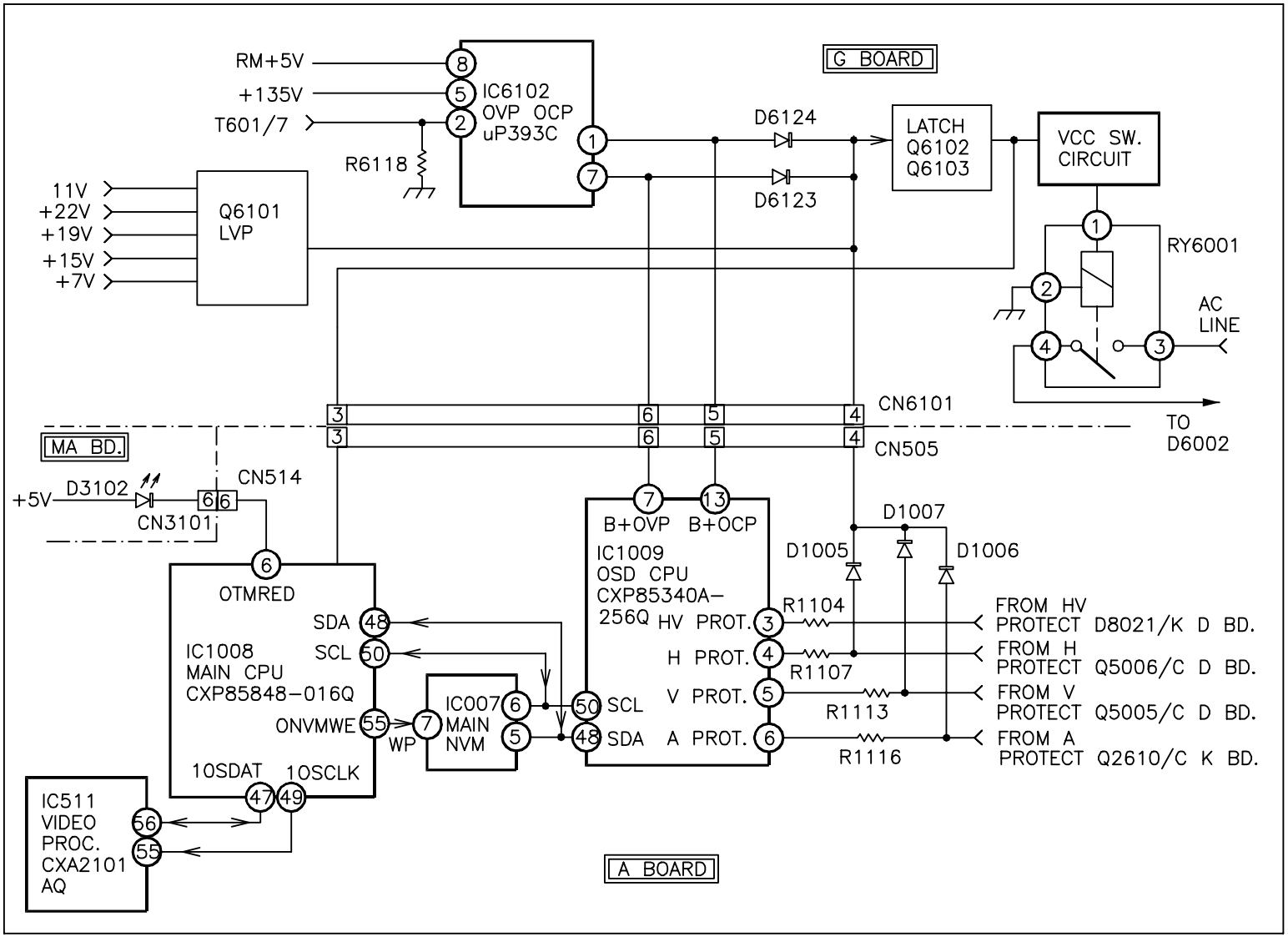
There may be situations when the diagnostic system will not work. These situations generally occur when there are power supply problems with the set. When this occurs, the LED will blink continuously at .3 second intervals. More information on troubleshooting these problems will be covered in the power supply section. Keep in mind that other power supply problems could cause a false indication to be given by the Self-Diagnostic section.

Circuit Description

All of the circuits that can be indicated by the self-diagnostic have an input to IC1009 OSD CPU, except for the AKB circuit. The indication from AKB is sent over the I²C data lines to IC1008 Main CPU. This data is then sent to IC1009 OSD CPU to be displayed. These indicators are from protection circuits, which will be discussed in more detail in the individual circuit descriptions. They all output a HIGH when they are activated. When a failure is received from one of the circuits, it is stored in IC1007 NVM. This can be helpful when problems are intermittent. Keep in mind that failures might not always indicate the correct circuit. For example, if there is an intermittent HV failure, the indication could be displayed as AKB failure.

In addition to sending a signal to the OSD processor, all of these protect lines are connected to the power supply latch on the G board, except for AKB and HV. This means that if there is a protect condition indicated by any circuit except AKB or HV, the set will shut down. When the set shuts down, the Timer LED will blink as stated previously. The set must be unplugged before you can attempt to operate it when a shutdown occurs.

There is also an additional LVP circuit on the G board that will not be indicated when a failure occurs. This is due to a problem in this area that causes a number of dilemmas and usually occurs too quickly for an indication to be given. When there is a failure in this area, the Timer LED will flash continuously every .3 seconds.



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1 Sony Drive
Park Ridge, New Jersey 07656

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