SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

VERTICAL DEFLECTION CIRCUITS FOR TV & MONITOR

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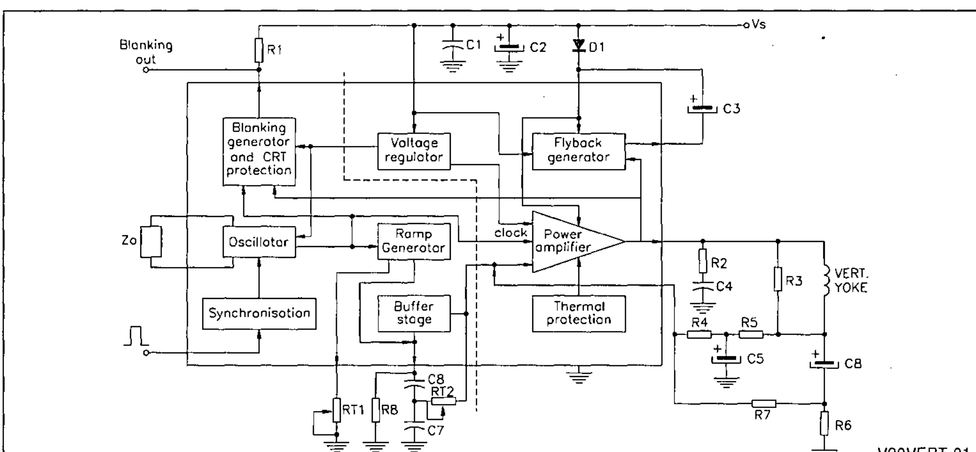
INDEX

1. INTRODUCTION

In a general way we can define vertical stages circuits able to deliver a current ramp suitable to drive the vertical deflection yoke.

In Figure 1 is represented the more general possible block diagram of a device performing the vertical deflection.

Figure 1 : Block Diagram of a General Deflection Stage.

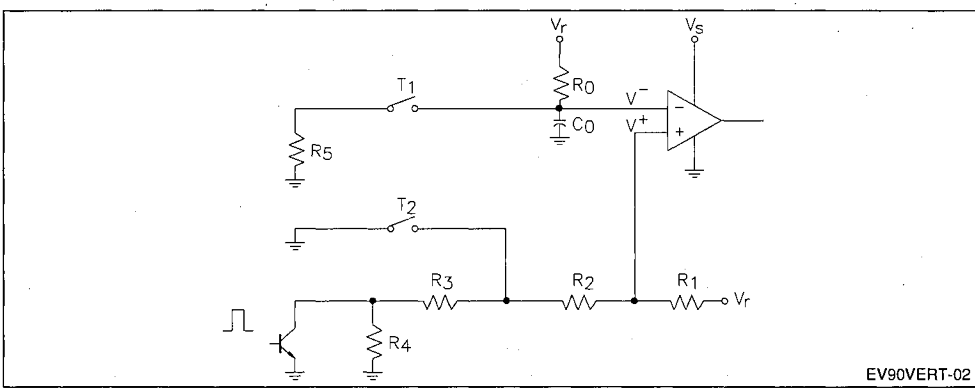


Such a device will be called "complete vertical stage" because it can be simply driven by a synchronization pulse and it comprises all the circuitry necessary to perform the vertical deflection that is : oscillator, voltage ramp generator, blanking genetor, output power and flyback generator.
At the right side of the dotted line in Figure 1 is represented the circuitry characterizing a "vertical output stage". This kind of device comprises only the power stages and it has to be driven by a voltage sawtooth generated by a previous circuit (for example a horizontal and vertical synchronization stage.
In the first class there are the following devices : TDA1170D, TDA1170N, TDA1170S, TDA1175, TDA1670A, TDA1675, TDA1770A, TDA1872A, TDA8176.
In the second class there are : TDA2170, TDA2270, TDA8170, TDA8172, TDA8173, TDA8175, TDA8178, TDA8179.
There is also a third class of vertical stages comprising the voltage ramp generator but without the oscillator; these circuits must be driven by an already synchronized pulse. In this third class there are : TDA1771 and TDA8174.

2. OSCILLATOR

There are two different kinds of oscillator stages used in SGS-THOMSON complete vertical deflections, one is used in TDA1170D, TDA1170N, TDA1170S, TDA1175 and TDA8176, the other in TDA1670A, TDA1675, TDA1170A and TDA1872A.
The principle of the first kind of oscillator is represented in Figure 2.
The following explanations will be the more general possible; we shall inform the reader when we refer to a particular device.

Figure 2 : First Kind of Oscillator Stage.

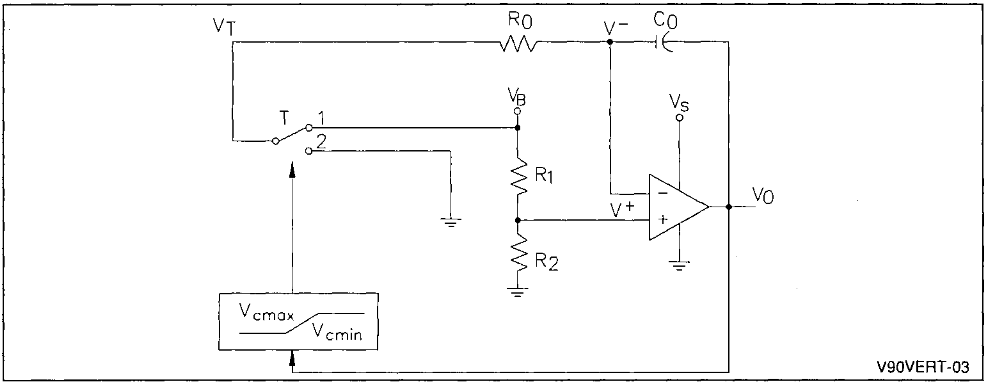


When the switches T_1 and T_2 are opened the C_O capacitor charges exponentially through R_O to the value $V^+_{(MAX)}$ determined by the integrated resistors R_1, R_2, R_3 and R_4. At this point the switches are closed, short-circuiting R_3 and R_4, so the voltage at the non-inverting input becomes $V^+_{(MIN)}$. The capacitor C_O discharges to this value through the integrated resistor R_5.
The free running frequency can be easily calculated resulting in :

$$T_O = R_O \cdot C_O \cdot \log \frac{V_R - V^+_{(MIN)}}{V_R - V^+_{(MAX)}} + R_5 \cdot C_O \cdot \log \frac{V^+_{(MAX)}}{V^+_{(MIN)}} \quad (1) \qquad f_O = \frac{1}{T_O}$$

with $R_O = 360\ k\Omega$ and $C_O = 100\ nF$, it results in 43.7 Hz.
The oscillator synchronization is obtained reducing the superior threshold $V^+_{(MAX)}$ short-circuiting the R_4 resistor when a vertical synchronization pulse occurs.
The second kind of oscillator is represented in Figure 3.

Figure 3 : Second Kind of Oscillator Stage.



When the switch T is in position 2, a constant current $I_{CO} = V^- / R_O$ flows through C_O charging it with a voltage ramp. When the voltage V_O reaches $V_{O(MAX)}$, T passes in position 1, so a constant current $I_{CO} = (V_B - V^-) / R_O$ discharges the capacitor causing the inversion of the voltage ramp slope at the output V_O (t). The discharges stops when V_O reaches the value $V_{O(MIN)}$ and the cycle takes place again.

It is possible to calculate the free running frequency f_O with the following formula :

$$T_O = \frac{(V_{O(MAX)} - V_{O(MIN)}) \cdot R_O \cdot C_O}{V^-} + \frac{(V_{O(MAX)} - V_{O(MIN)}) \cdot R_O \cdot C_O}{V_B - V^-} \quad (2)$$

with $V_{O(MAX)} - V_{O(MIN)} = 3.9V$, $V_B = 6.5V$, $V^- = 0.445V$, $R_O = 7.5k\Omega$ and $C_O = 330nF$ it results in : $f_O = 43.8Hz$.

The oscillator synchronization is still obtained in the above mentioned way.

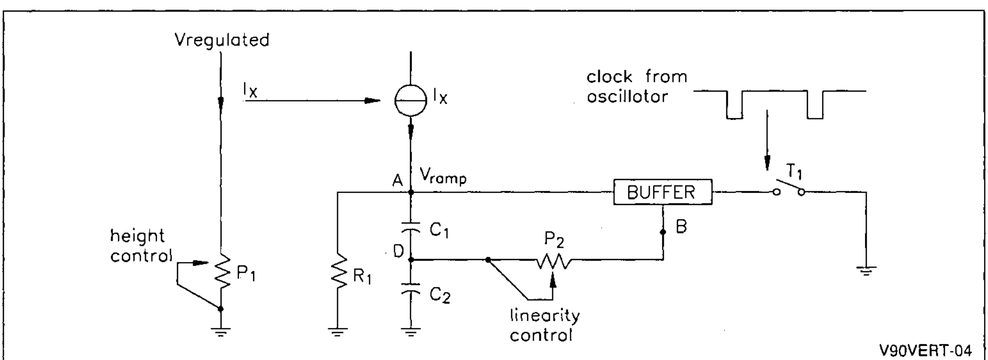
In order to guarantee a minimum pull-in range of 14Hz the threshold value has been chosen in $V_P = 4.3V$.

The spread of the free running frequency in this kind of oscillator is very low because it mainly depends from the threshold values $V_{O(MAX)}$, $V_{O(MIN)}$ and V^- that are determined by resistor rates that can be done very precise.

3. RAMP GENERATOR

The ramp generator is conceptually represented in Figure 4.

Figure 4 : Ramp Generator.



The Voltage ramp is obtained charging the group R_1, C_1 and C_2 with a constant current I_X.

It is easy to calculate the voltage V_{RAMP} That results in :

$$V_{RAMP}(t) = (V_{(MIN)} - R_1 \cdot I_X)\ e^{-\frac{t}{R_1 \cdot C}} + R_1 \cdot I_X \qquad (3)$$

where $V_{(MIN)}$ is the voltage in A when the charge starts and C is the series of C_1 and C_2.
The resistor R_1 is necessary to give a "C correction" to the voltage ramp. The ramp amplitude is determined by $I_X = V_{REG} / P_1$,so the potentiometer P_1 is necessary to perform the height control.
The voltage ramp is then transferred on a low impedence in B through a buffer stage.
Te P2 potentiometer connected between D and B performs the ramp linearity control or "S correction" that is necessary to have a correct reproduction of the images on the TV set.
The voltage ramp in B grows up until the switch T_1 is closed by a clock pulse coming from the oscillator; in this way the capacitors discharge fastly to $V_{(MIN)}$ that is dependent upon the saturation voltage of the transistor that realizes the switch.
At this point the exponential charge takes place again.

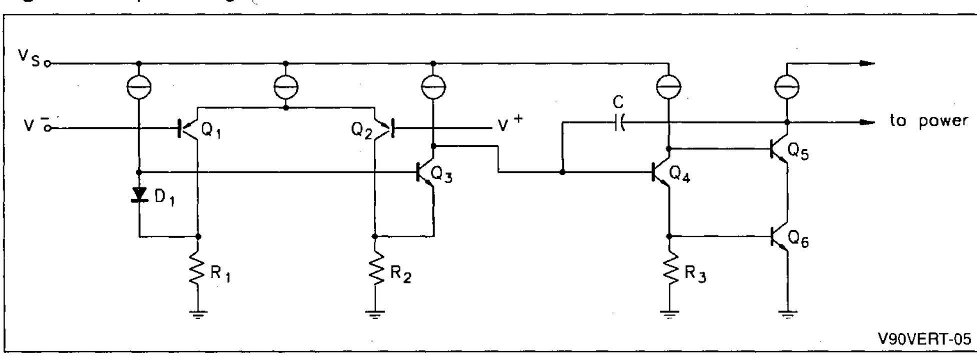
4. BLANKING GENERATOR AND CRT PROTECTION

This circuit senses the presence of the clock pulse coming from the oscillator stage and the flyback pulse on the yoke. If both of them are present a blanking pulse is generated able to blank the CRT during the retrace period. The duration of this pulse is the same of the one coming from the oscillator.
If for any reason the vertical deflection would fail, for instance for a short circuit or an open circuit of the yoke, the absence of the flyback pulse puts the circuit in such a condition that a continuous vertical blanking is generated in order to protect the CRT against eventual damages.
This circuit is available only in the following devices : TDA1670A, TDA1675, TDA1770A and TDA1872A.
The stages we will consider starting from this point are common both to complete vertical stages and vertical output stages.

5. POWER AMPLIFIER STAGE

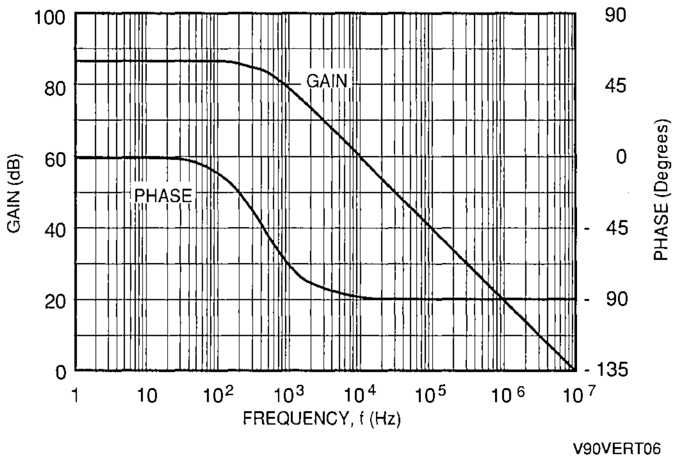
This stage can be divided into two distinct parts : the amplifier circuit and the output power.
The amplifier is realized with a differential circuit; a schematic diagram is represented in Figure 5.

Figure 5 : Amplifier Stage.



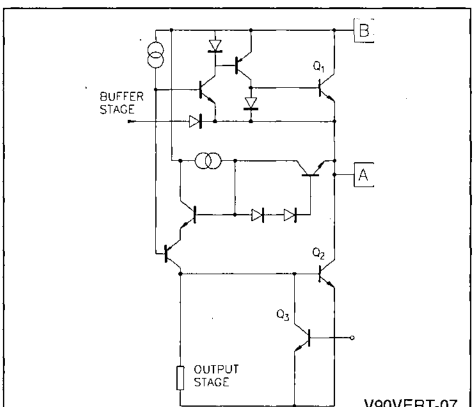
The open-loop gain of the circuit is variable from 60dB to 90dB for the different integrated circuits.
The compensation capacitor C determines the dominant pole of the amplifier. In order to obtain a dominant pole in the range of 400Hz, the capacitor must be of about 10pF.
As an example in Figure 6 is represented the boole diagram of the amplifier open loop gain for TDA8172.

Figure 6 : Amplifier Open Loop Gain and Phase.



The output power stage is designed in order to deliver to the yoke a vertical deflection current from 1 to 2 Apeak, depending upon the different devices, and able to support flyback voltages up to 60V. A typical output stage is depicted in Figure 7.

Figure 7 : Power Stage.



The upper power transistor Q_1 conducts during the first part of the scanning period when the vertical deflection current is flowing from the supply voltage into the yoke; when the current becomes negative, that is it comes out of the yoke, it flows through the lower power transistor Q_2.The circuit connected between the two output transistors is necessary to avoid distortion of the current at the crossing of zero, when Q_1 is turned off and Q_2 is turned on.
When the flyback begins, Q_2 is switched-off by Q_3 in order to make it able to support the high voltage of the flyback pulse.
The circuit behaviour during flyback is explained in chapter 7.

6. THERMAL PROTECTION

The thermal protection is available in all the devices except the TDA1170 family and the TDA8176.
This circuit is usefull to avoid damages at the integrated circuit due to a too high junction temperature caused by an incorrect working condition.
It is possible to sense the silicon temperature because the transistor V_{BE} varies of - 2 mV/ °C, so a temperature variation can be reconducted to a voltage variation.
If the temperature increases and it is reaching 150°C, the integrated circuit output is shut down by putting off the current sources of the power stage.

7. FLYBACK BEHAVIOUR

In order to obtain sufficiently short flyback times, a voltage greather than the scanning voltage must be applied to the deflection yoke.
By using a flyback generator, the yoke is only supplied with a voltage close to double the supply during flyback.
Thus, the power dissipated is reduced to approximately one third and the flyback time is halfed.

The flyback circuit is shown in Figure 8 together with the power stage.

Figure 8 : Output Power and Flyback stages.

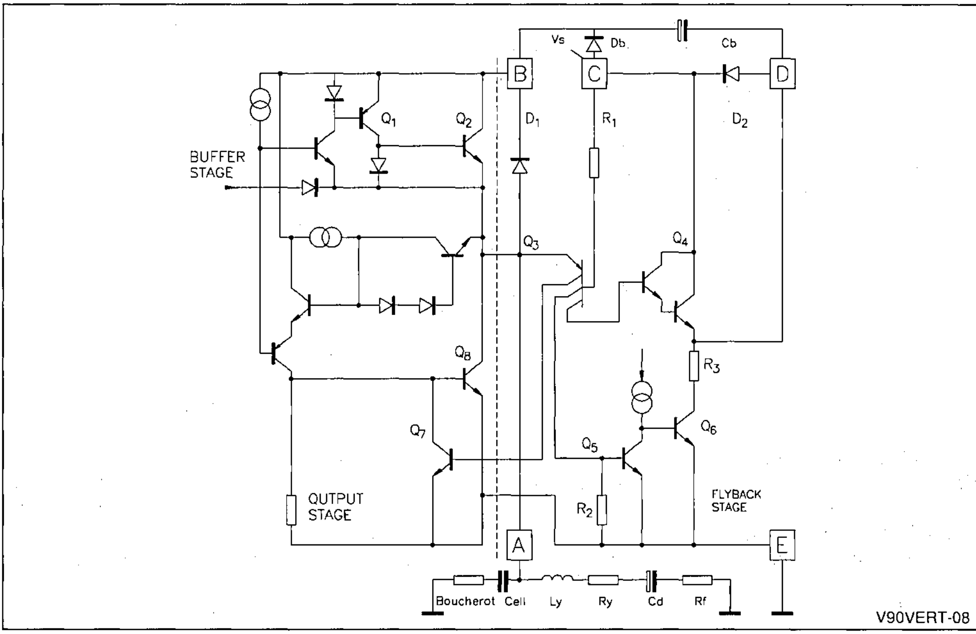
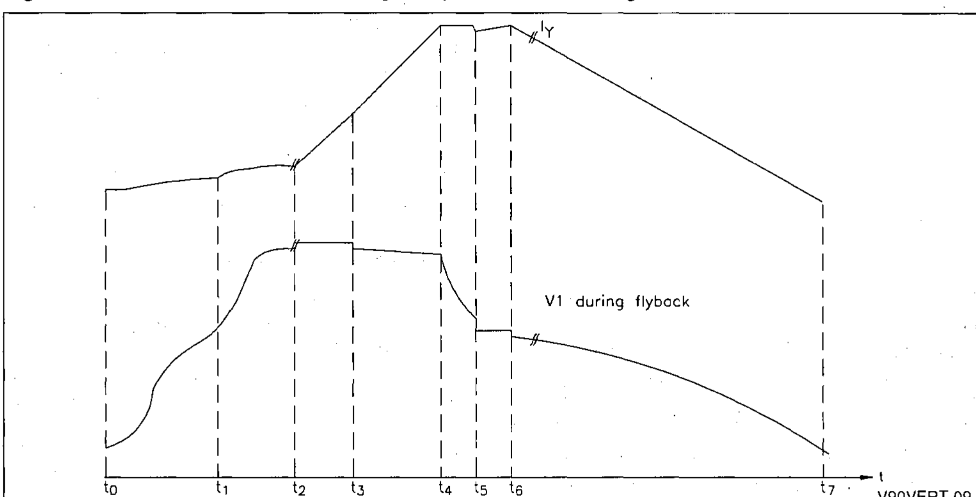


Figure 9 shows the circuit behaviuor, to show operation clearly. The graphs are not drawn to scale. Certain approximations are made in the analysis in order to eliminate electrical parameters that do not significantly influence circuit operations.

Figure 9 : Current in the Yoke and Voltage Drop on the Yoke during Vertical Deflection.



a) Scan period (t_6 - t_7) : Figure 10

During scanning Q_3, Q_4 and Q_5 are off and this causes Q_6 to saturate.

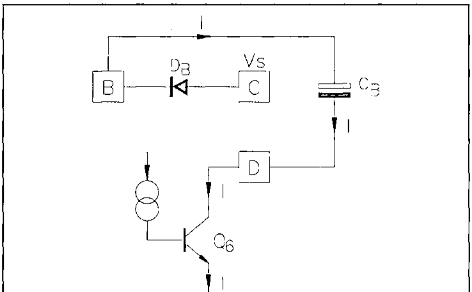
A current from the voltage supply to ground flows through D_B, C_B and Q_6 charging the C_B capacitor up to :

$$V_{CB} = V_S - V_{DB} - V_{Q6SAT} \qquad (4)$$

At the end of this period the scan current has reached its peak value (I_P) and it is flowing from the yoke to the device. At the same time V_A has reached its minimum value.

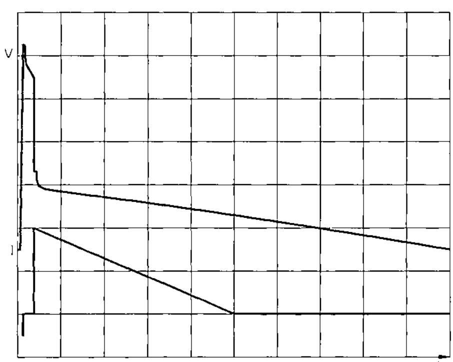
In Figures 11 and 12 are depicted the voltage drop on the yoke and the currents flowing through D_B and the yoke.

Figure 10 : Circuit Involved during Scan Period.



V90VERT-10

Figure 11 : Voltage Drop on the Yoke and Current Flowing through D_B.
V = 10V/div.
I = 0.5A/div.
t = 2ms/div.



V90VERT-11

Figure 12 : Voltage Drop on the Yoke and Current Flowing through the Yoke.
V = 10V/div.
I = 1A/div.
t = 5ms/div.

V90VERT-12

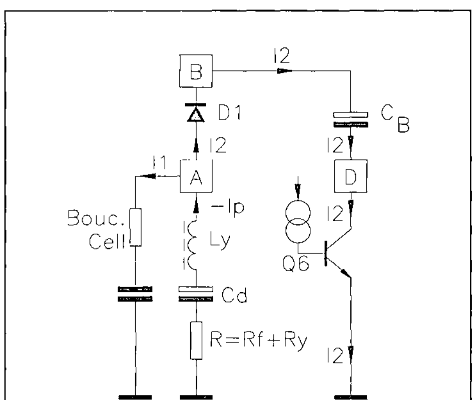
b) Flyback starting (t_0 - t_1) : Figure 13

Q_8, that was conducting the - I_P current, is turned off by the buffer stage.

The yoke, charged to I_P, now forces this current to flow partially through the Boucherot cell (I_1) and partially through D_1, C_B and Q_6 (I_2).

In Figures 14, 15 and 16 are represented the currents flowing through the yoke, the Boucherot cell and D_1.

Figure 13 : Circuit Involved during Flyback Starting.



V90VERT-13

c) Flyback starting (t_1 - t_2)

When the voltage drop at pin A rises over V_S, Q_3 turns on and this causes Q_4 and Q_5 to saturate. Consequently Q_6 turns off.

During this period the voltage at pin D is forced to :

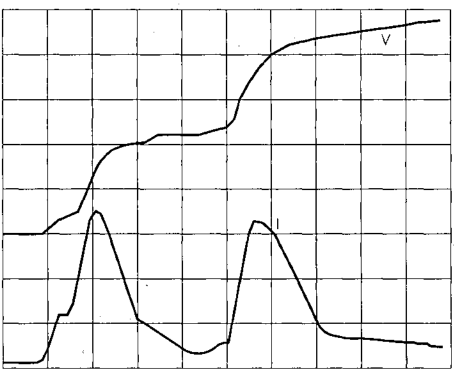
$$V_D = V_S - V_{Q4SAT} \qquad (5)$$

Therefore the voltage at pin B becomes :

$$V_B = V_{CB} + V_D \qquad (6)$$

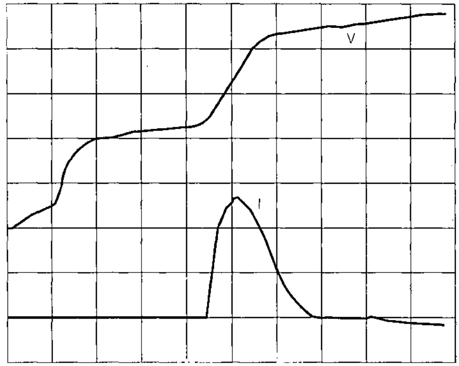
The yoke current flows in the Boucherot cell added to another current peak flowing from V_S via Q_4 and C_B (Figures 14 and 15).

Figure 14 : Voltage Drop on the Yoke and Current Flowing through the Boucherot Cell.
V = 10V/div.
I = 1A/div.
t = 1µs/div.



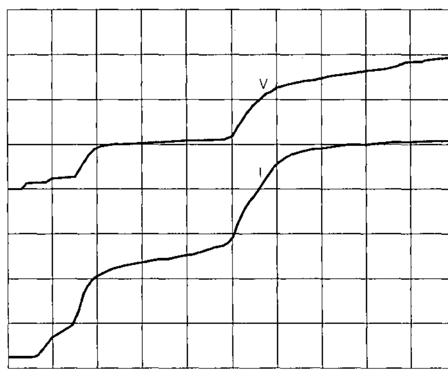
V90VERT-14

Figure 15 : Voltage Drop on the Yoke and Current Flowing through D_1.
V = 10V/div.
I = 1A/div.
t = 1µs/div.



V90VERT-15

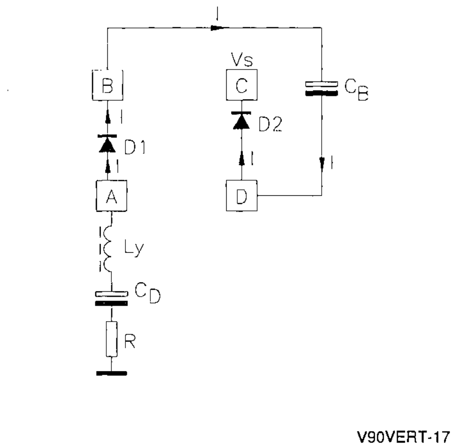
Figure 16 : Voltage Drop on the Yoke and Current Flowing through the Yoke.
V = 10V/div.
I = 100mA/div.
t = 1µs/div.



V90VERT-16

d) Negative current rise (t_2 - t_3) : Figure 17

Figure 17 : Circuit Involved during the Negative Current Rise.



During this period, the voltage applied at pin A is :

$$V_A = V_B + V_{D1},$$
$$V_A = V_{CB} + V_D + V_{D1},$$
$$V_A = V_S - V_{DB} - V_{Q6SAT} + V_S + V_{D2} + V_{D1},$$
$$V_A = 2 \cdot V_S + V_{D1} + V_{D2} - V_{DB} - V_{Q6SAT} \qquad (7)$$

It is possible to calculate the current solving the following equation :

$$V_A = L_Y \frac{di}{dt} + \frac{1}{C_D}\int i \cdot dt + R \cdot i \qquad (8)$$

where $R = R_F + R_Y$

Because the voltage at pin A is approximatively constant (error less than 2%) we can simplify the (8) in the following equation :

$$\frac{d^2 i}{dt^2} + \frac{R}{L_Y}\frac{di}{dt} + \frac{1}{L_Y C_D} i = 0 \qquad (9)$$

It results in :

$$i(t) = \frac{I_P}{e^{2\beta\Delta T_1} - 1} e^{(-\alpha+\beta)t} - \frac{I_P}{1 - e^{-2\beta\Delta T_1}} e^{(-\alpha-\beta)t} \qquad (10)$$

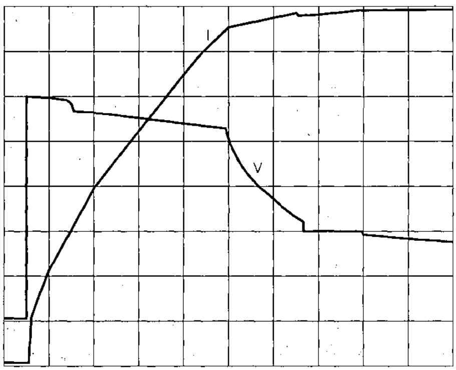
where :

$$\alpha = \frac{R}{2\ L_Y} \qquad \beta = \sqrt{\frac{R^2}{4 \cdot L_Y^2} - \frac{1}{L_Y C_D}} \qquad \Delta T_1 = t_3 - t_2$$

Because of ΔT_1 is two orders of magnitude lower than the scan time, we can apply an exponential sum to obtain the following equation :

$$i(t) = I_P \frac{\alpha \cosh(2\beta\,\Delta T_1) + \beta \sinh(2\beta\,\Delta T_1) - \alpha}{\cosh(2\beta\,\Delta T_1) - 1} t - I_P \qquad (11)$$

Figure 18 : Voltage Drop on the Yoke and Current Flowing through the Yoke.
V = 10V/div.
I = 250mA/div.
t = 100µs/div.



V90VERT-18

Simplifying :

$$i(t) = I_P\left(\alpha + \frac{1}{\Delta T_1}\right)t - I_P \qquad (12)$$

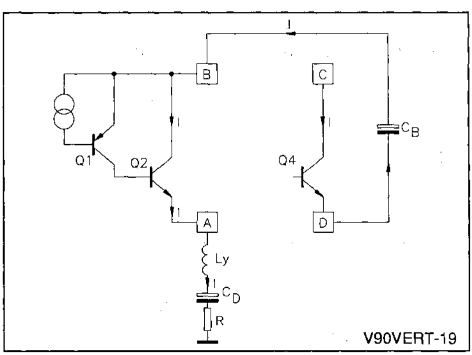
The slope of the current is therefore :

$$\frac{di}{dt} = \left(\frac{R}{2\,L_Y} + \frac{1}{\Delta T_1}\right) I_P \quad \text{(A/s)} \qquad (13)$$

The current flows from the yoke to V_S through D_1, C_B and D_2, and it is depicted in Figure 18.

e) Positive current rise (t_3 - t_4) : Figure 19

Figure 19 : Circuit Involved during the Positive Current Rise.



V90VERT-19

When the current becomes zero, D_1 turns off and Q_2 saturates; so the pin A voltage becames :

$$V_A = V_B - V_{Q2SAT}$$
$$V_A = 2 \cdot V_S - V_{DB} - V_{Q6SAT} - V_{Q4SAT} - V_{Q2SAT} \qquad (14)$$

The current flows from $+V_S$ into the yoke through Q_4, C_B and Q_2 and rises from zero to I_P as it can be seen in Figure 18.
By using the previous procedure explained in section d), we can obtain the slope of the current :

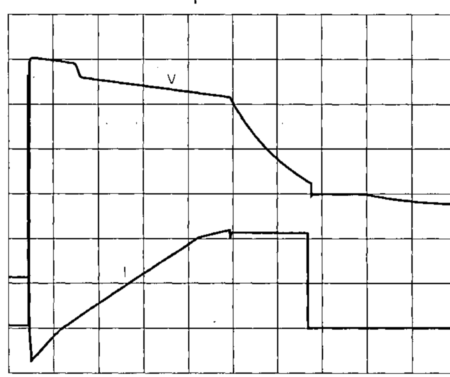
$$\frac{di}{dt} = \left(\frac{R}{2\,L_Y} + \frac{1}{\Delta T_2}\right) I_P \quad \text{(A/s)} \qquad (15)$$

where $\Delta T_2 = t_4 - t_3$

f) Flyback decay (t_4 - t_5)

When the yoke current reaches its maximum peak, Q_2 desaturates and conducts the maximum peak current flowing from V_S via Q_4 and C_B into L_Y; the current flowing through C_B is depicted in Figure 20.

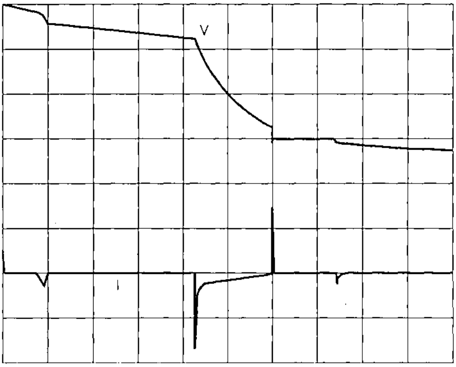
Figure 20 : Voltage Drop on the Yoke and Current Flowing through C_B.
V = 10V/div.
I = 0.5A/div.
t = 100µs/div.



V90VERT-20

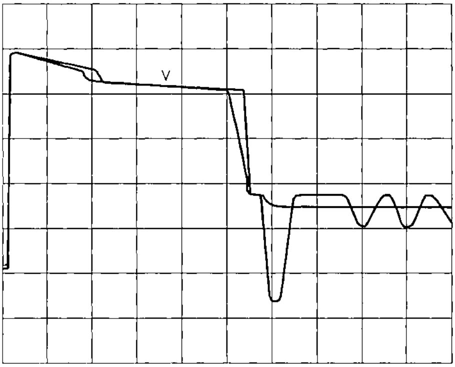
An eventual antiringing parallel resistor modify the linear decay slope in an exponential one, as it can be seen in Figure 22.
This continues until the buffer stage turns Q_2 on.
The effect of the Boucherot cell during this periode is negligible (see Figure 21).

Figure 21 : Voltage Drop on the Yoke and Current Flowing through the Boucherot Cell.
V = 10V/div.
I = 100mA/div.
t = 100µs/div.



V90VERT-21

Figure 22 : Effect of the Resistor in Parallel connected to the yoke.
V = 10V/div.



V90VERT-22

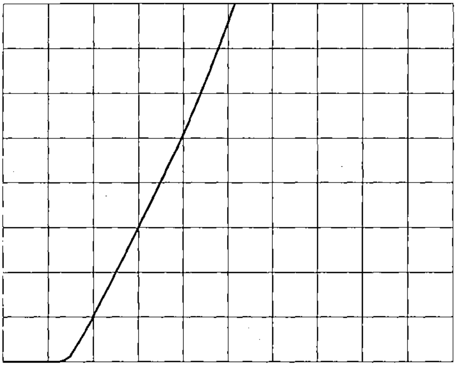
g) V_A pedestal (t_5 - t_6)

When V_A reaches the value V_S of the supply voltage, the flyback generator stops its function.
Q_3 is turned off and turns off Q_4 that open the connection between pin D and V_S.
Therefore V_B drops to V_S - V_{DB} while : $V_A = V_S - V_{DB} - VQ_{2CE\ on}$
At this point the normal scan takes place.

8. CURRENT-VOLTAGE CHARACTERISTICS OF THE RECIRCULATING DIODES.

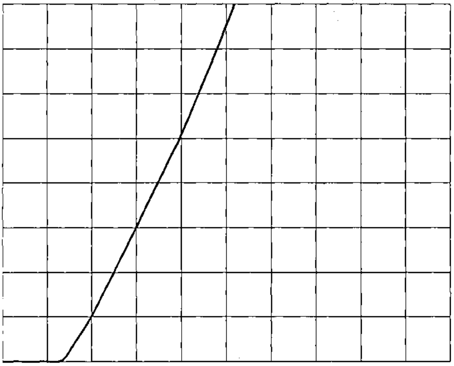
The following Figures 23 and 24 reproduce the I - V characteristics of the integrated recirculating diodes D_1 and D_2 (see Figure 8).

Figure 23 : I - V Characteristic of the Diode D_1.
V = 500mV/div.
I = 200mA/div.



V90VERT-23

Figure 24 : I - V Characteristic of the Diode D_2.
V = 500mV/div.
I = 200mA/div.



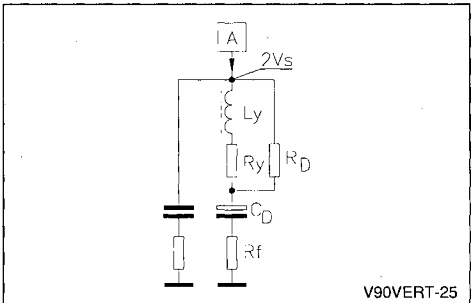
V90VERT-24

These characteristics are useful in order to calculate the maximum voltage reached at pin A with the formula (7) explained in chapter 7.

9. CALCULATION PROCEDURE OF THE FLYBACK DURATION

The flyback duration can be calculated using the following procedure (referring to Figure 25).

Figure 25 : Circuit Involved in the Calculation of Flyback Duration.



During the flyback period the voltage applied at pin A is about 2 V_S, as previously explained in chapter 7. The voltage drop across C_D is approximatively a constant voltage little less than $V_S/2$. The voltage on the feedback resistor R_F is :

$V_{RF}(t) = R_F \, I_Y(t)$

so in the period which we are considering it is negligible respect to $V_S/2$.

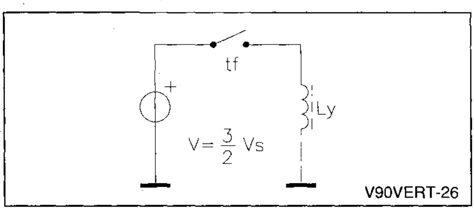
The effect of the Boucherot cell during this period is not sensible as it can be seen in Figure 21; while R_D acts principally during the flyback decay time (Figure 9 : $t_4 - t_5$) reducing its slope and the resulting oscillations but doesn't influence the total flyback time as shown in Figure 22. So their influences are also negligible.

Now the effective voltage drop across the yoke can be approximated to :

$$2 \cdot V_S - \frac{V_S}{2} = \frac{3}{2} V_S$$

Figure 25 can be simplified as shown in Figure 26.

Figure 26 : Simplified Circuit for the Calculation of Flyback Duration.



The voltage charges the coil with a linear current that can be calculated in the following way :

$$i(t) = \frac{1}{L_Y}\int V \cdot dt = \frac{1}{L_Y}\int \frac{3}{2} V_S \cdot dt \quad (16)$$

$$i(t) = \frac{1}{L_Y}\frac{3}{2} V_S \cdot t + K$$

K is calculated imposing that the current at the beginning of the flyback is - I_P.

$$i(0) = -I_P \qquad K = -I_P$$

$$i(t) = \frac{3}{2}\frac{V_S}{L_Y}\, t - I_P \quad (17)$$

At the end of the flyback period the current will be + I_P, so we can write :

$$I_P = \frac{3}{2}\frac{V_S}{L_Y}\, t_F - I_P$$

The duration of the flyback period is then :

$$t_F = \frac{4}{3}\frac{I_P L_Y}{V_S} = \frac{2}{3}\frac{I_Y L_Y}{V_S} \quad (18)$$

10. APPLICATION INFORMATION

The vertical deflection stages producted by SGS-THOMSON are able to cover the complete range of applications that the market need for color television and high/very high resolution monitors.

Television and monitor applications are not very different but in monitor field, in addition to the linearity and interlacing problems, we have to pay attention to the flyback time that must be very short for very high resolution models.

In television applications the most important requirement is to choose the lowest supply voltage possible in order to minimize the power dissipation in the integrated circuit, reducing the dimension of the heatsink, and the power dissipation from the voltage supplier.

These results can be reached very easily with SGS-THOMSON deflection stages because of the high efficiency of the flyback generator circuit used.

In high resolution monitors one of the main problems is to reach the very short flyback time requested; the flyback generator, together with the high current and power dissipation capabilities, solve all the problems in a simple way.

In Figures 27, 28 and 29 are depicted three typical application circuits for the different kinds of integrated circuits available.

Figure 27 : Application Circuit for TDA1170.

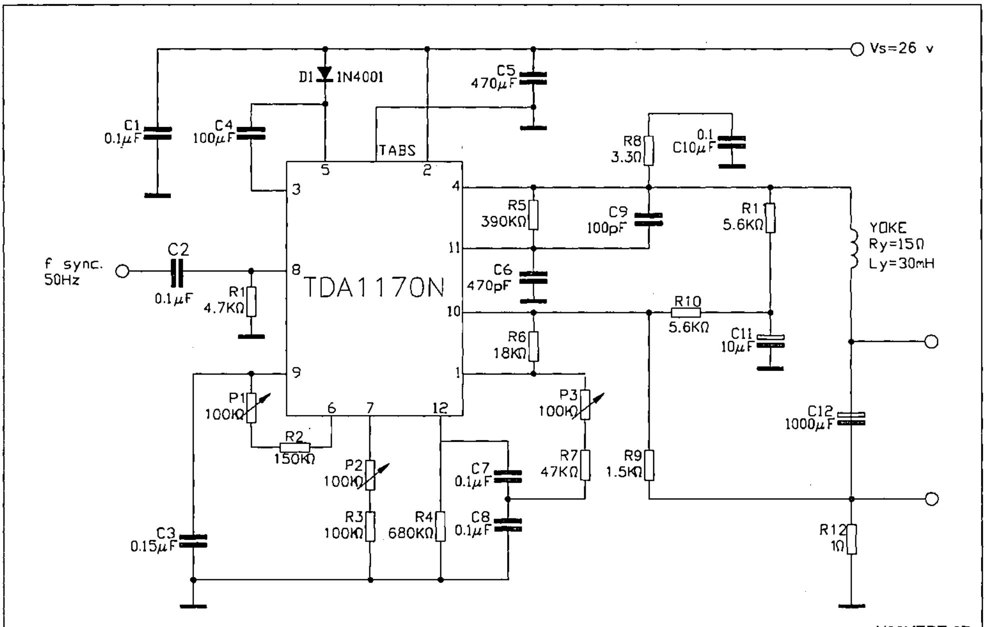
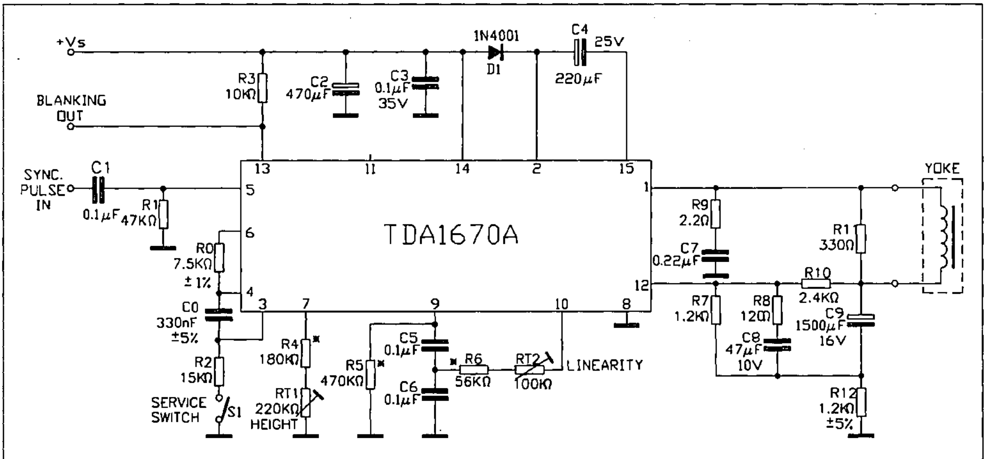


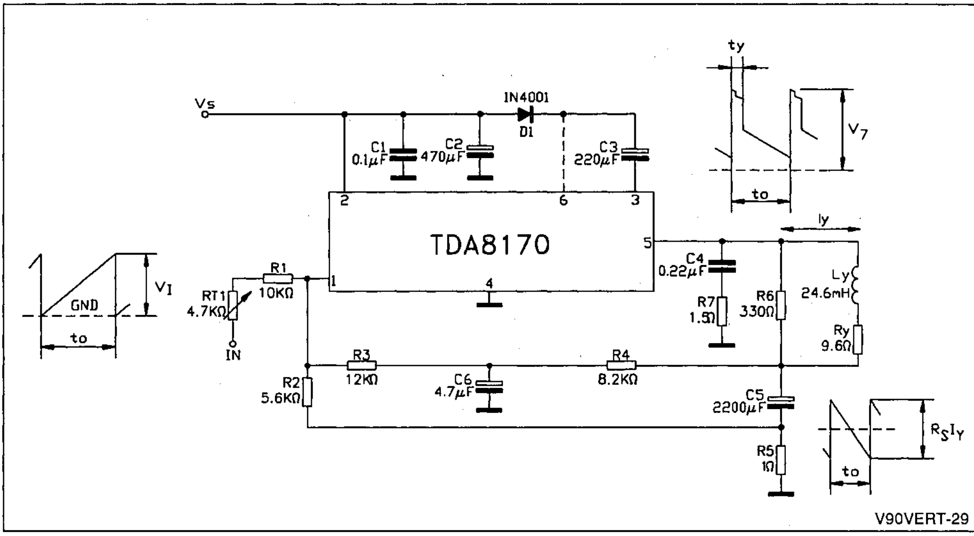
Figure 28 : Application Circuit for TDA1670A.



* The value depends on the characteristics of the CRT. The value shown is indicative only.

V90VERT-28

Figure 29 : Application Circuit for TDA8170.



In the following chapters we shall do the calculation for television and monitor in order to choose the right voltage supply and external network for the yoke used and the current requirements.

11. SUPPLY VOLTAGE CALCULATION

For television applications we shall calculate the minimum supply voltage necessary to have vertical scanning knowing the yoke characteristics and the current required for the given application.

Figure 30 shows the terms used in this section, while the circuit part involved in the following calculations is depicted in Figure 31.

Figure 30 : Parameters Used in the Calculation of the Supply Voltage.

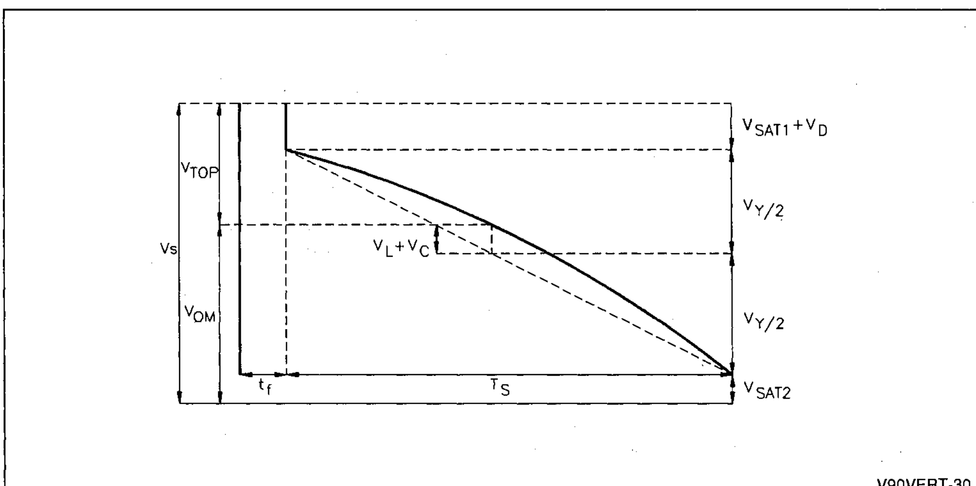
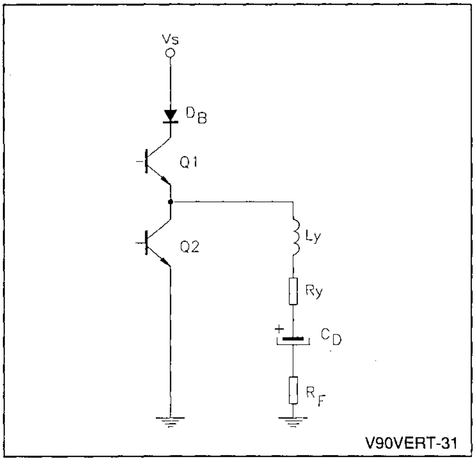


Figure 31 : Circuit Involved in the Calculation of the Supply Voltage.



V_S = supply voltage.

V_Y = nominal voltage required to produce the scanning current including the feedback resistance and the 20% increasing for temperature variations in the yoke current;

$$V_Y = (1.2\,R_Y + R_F)\ I_Y \qquad (19)$$

V_{SAT1} = nominal output saturation voltage due to the upper power transistor Q_1 (see Figure 32);

V_{SAT2} = nominal output saturation voltage due to the lower power transistor Q_2 (see Figure 33);

V_{OM} = nominal quiescent voltage (midpoint) on the output power transistors;

V_C = voltage peak due to the charge of C_D capacitor;

$$V_C = \frac{I_Y \cdot t_S}{8 \cdot C_D} \qquad (20)$$

V_L = voltage drop due to the yoke inductance L_Y;

$$V_L = \frac{L_Y \cdot I_Y}{t_S} \qquad (21)$$

Figure 32 : Saturation characteristic of the Upper Power Transistor.

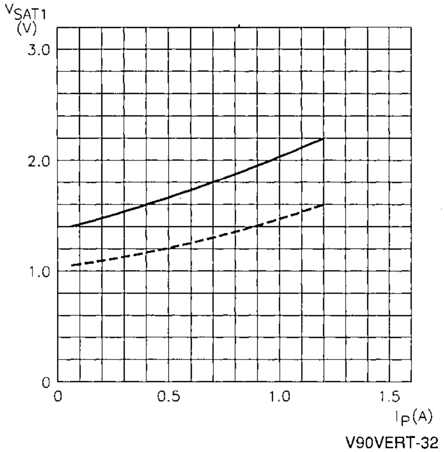
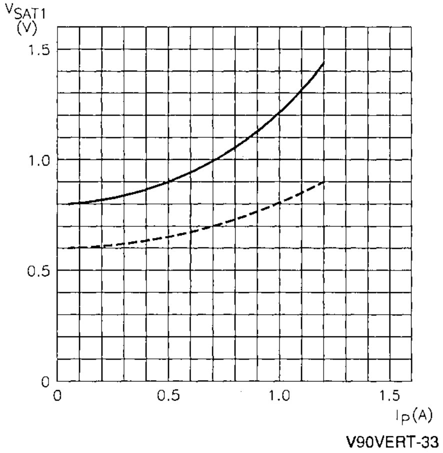


Figure 33 : Saturation characteristic of the Lower Power Transistor.



V_D = nominal voltage drop on D_B diode in series with the supply;

T = vertical scan period;

t_F = flyback time;

$$t_F = \frac{2}{3}\,\frac{I_Y \cdot L_Y}{V_S}$$

t_S = scanning time;

$$t_S = T - t_F$$

I_Y = peak to peak deflection current;
R_Y = nominal yoke resistance;
L_Y = nominal yoke inductance;
R_F = feedback resistor.

Referring to Figure 30 it is easy to see that the minimum supply voltage is given by :

$$V_S = V_{OM} + V_{TOP} \qquad (22)$$

where :

$$V_{OM} = \frac{V_Y}{2} + V_{SAT2} + V_C + V_L \qquad (23)$$

and :

$$V_{TOP} = \frac{V_Y}{2} + V_D + V_{SAT1} - V_L - V_C \qquad (24)$$

So we obtain :

$$V_S = V_Y + V_D + V_{SAT1} + V_{SAT2} \qquad (25)$$

The (25) gives the minimum voltage supply if we do not consider the tolerances of the integrated circuit and of the external components, but the calculation, even if it was not realistic, it was useful in order to understand the procedure.
Now we shall do the same thing considering all the possible spreads; we can in this way obtain the real minimum supply voltage.
We shall follow the statistical composition of spreads because it is never possible that all of them are present at the same time with the same sign.

We must consider the following spreads :

- ΔV_Y due to the variation of yoke and feedback resistance and yoke current, supposing a 10% of regulation range in scanning current and a precision of 7% for resistors;

$$\Delta V_Y = (1.2\ R_Y + R_F)\ 1.07\ (1.1\ I_Y) - V_Y \qquad (26)$$

- ΔV_C due to the tolerance of C_D and yoke current regulation;

$$\Delta V_C = \frac{1.1\ I_Y\ t_S}{8\ C_{D(MIN)}} - V_C \qquad (27)$$

- ΔV_L due to the tolerance of L_Y (± 10%) and yoke current regulation;

$$\Delta V_L = \frac{1.1\ I_Y\ 1.1\ L_Y}{t_S} - V_L \qquad (28)$$

$$\Delta V_{SAT1} = V_{SAT1(MAX)} - V_{SAT1}$$
$$\Delta V_{SAT2} = V_{SAT2(MAX)} - V_{SAT2}$$

For each parameter, it is necessary to calculate the factor ρ, expressing the percentual influence of every parameter variation on the nominal supply voltage, with the following formulas :

for V_{OM} :

$$\rho = \frac{\Delta V}{V_{OM}}$$

for V_{TOP} :

$$\rho = \frac{\Delta V}{V_{TOP}}$$

We have then to calculate the square mean root of the spreads expressed as :

$$\sqrt{\Sigma\ \rho^2}$$

So if we call :

$$V_{OM1} = V_{OM}\left(1 + \sqrt{\Sigma\ \rho^2}\right)$$

and :

$$V_{TOP1} = V_{TOP}\left(1 + \sqrt{\Sigma\ \rho^2}\right)$$

We can write :

$$V_S = V_{OM1} + V_{TOP1} \qquad (29)$$

An example of calculation will better explain the procedure. We shall consider a 26", 110°, neck 29.1mm tube whose characteristics are :
$I_Y = 1.2$ App;
$R_Y = 9.6\Omega \pm 7\%$;
$L_Y = 24.6$mH $\pm$ 10%.

We shall use a coupling capacitance C_D of 1500µF with + 50% and - 10% tolerance and a feedback resistance R_F of 1.2Ω.

a) Nominal minimum supply voltage :

$$V_Y = (1.2\,R_Y + R_F)\,I_Y = 15.264\text{ V}$$
$$V_C = \frac{I_Y \cdot t_S}{8 \cdot C_D} = 2\text{ V}$$
$$V_L = \frac{L_Y \cdot I_Y}{t_S} = 1.476\text{ V}$$
$$V_{SAT1} = 1.25\text{ V} \qquad V_{SAT2} = 0.68\text{ V}$$
$$V_D = 1\text{ V}$$
$$V_{OM} = 11.788\text{ V} \qquad V_{TOP} = 6.406\text{ V}$$

We obtain : $V_S = 18.2$V

b) Statistical minimum supply voltage :

$$\Delta V_C = 2.702\text{V}$$
$$\rho V_{YM} = \frac{V_{Y/2}}{V_{OM}} \qquad \rho^2\,V_{YM} = 1.313 \cdot 10^{-2}$$
$$\rho V_{YT} = \frac{V_{Y/2}}{V_{TOP}} \qquad \rho^2\,V_{YT} = 4.447 \cdot 10^{-2}$$
$$\Delta V_C = 0.445\text{ V} \qquad \rho^2\,V_{CM} = 1.421 \cdot 10^{-3}$$
$$\rho^2\,V_{CT} = 4.813 \cdot 10^{-3}$$
$$\Delta V_L = 0.31\text{ V} \qquad \rho^2\,V_{LM} = 6.914 \cdot 10^{-4}$$
$$\rho^2\,V_{LT} = 2.341 \cdot 10^{-3}$$
$$\Delta V_{SAT1} = 0.45\text{ V} \qquad \rho^2\,V_{SAT1T} = 4.935 \cdot 10^{-3}$$
$$\Delta V_{SAT2} = 0.27\text{ V} \qquad \rho^2\,V_{SAT2M} = 5.246 \cdot 10^{-4}$$
$$V_{OM1} = V_{OM}\left(1 + \sqrt{\sum \rho^2}\right) = 13.268\text{ V}$$
$$V_{TOP1} = V_{TOP}\left(1 + \sqrt{\sum \rho^2}\right) = 7.930\text{ V}$$
$$V_S = V_{OM1} + V_{TOP1} = 21.2\text{ V}$$

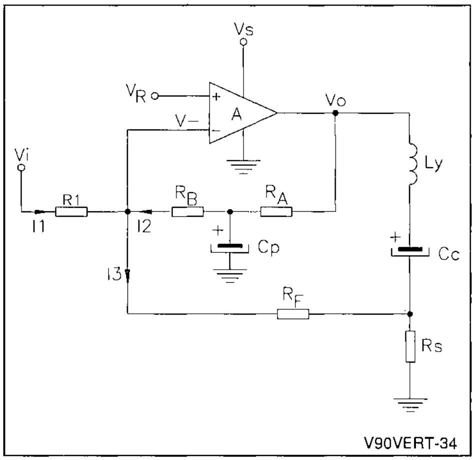
This is a real value for the minimum supply voltage needed by the above mentioned application.
In this case we obtain a flyback duration of about :

$$t_F = \frac{2}{3}\,\frac{I_Y \cdot L_Y}{V_S} \approx 900\ \mu\text{s}$$

12. CALCULATION OF MIDPOINT AND GAIN

For the calculation of the output midpoint voltage, it is necessary to consider the different feedback network for the applications of the various integrated circuits.
We shall first consider the TDA1170 family, the TDA1175, TDA2170, TDA2270, TDA8170, TDA8172, TDA8173, TDA8175 and TDA8176.
The equivalent circuit of the output stage is represented in Figure 34.

Figure 34 : Circuit Utilized for the Calculation of midpoint and gain for TDA1170, TDA1175, TDA8176, TDA2170, TDA2270, TDA8170, TDA8172, TDA8173 and TDA8175.



For DC considerations we shall consider the two capacitors as open circuits. Because of the very high gain of the amplifier we can suppose :
$V^- = V_R$.
We can so write :

$$I_1 + I_2 = I_3 \qquad (30)$$

where :

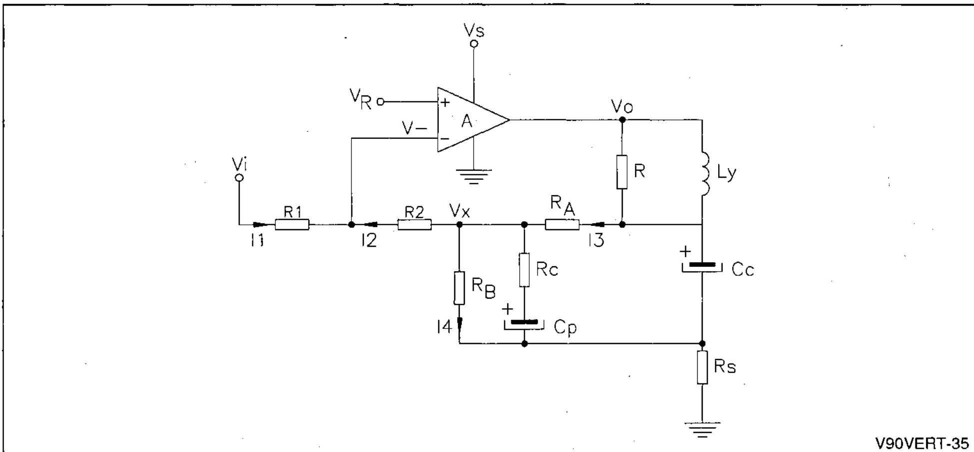
$$I_1 = \frac{V_i - V_R}{R_1} \qquad I_2 = \frac{V_O - V_R}{R_A + R_B} \qquad I_3 = \frac{V_R}{R_F + R_S}$$

Substituting into the (30) we obtain :

$$V_O = V_R \left(1 + \frac{R_A + R_B}{R_F + R_S}\right) - (V_i - V_R)\frac{R_A + R_B}{R_1} \qquad (31)$$

Let's consider now TDA1670A, TDA1675, TDA1770A, TDA1771, TDA1872A and TDA8174. The equivalent output circuit is depicted in Figure 35.

Figure 35 : Circuit Utilized for the Calculation of Midpoint and Gain for TDA1670A, TDA1675,TDA1770A, TDA1771, TDA1872A and TDA8174.



We can write :

$$I_1 = I_2 \qquad (32)$$

$$I_2 + I_3 = I_4 \qquad (33)$$

where :

$$I_1 = \frac{V_i - V_R}{R_1} \qquad I_2 = \frac{V_R - V_X}{R_2} \qquad I_3 = \frac{V_O - V_X}{R_A} \qquad I_4 = \frac{V_X}{R_B + R_S}$$

with the (32) and (33) we can calculate the DC output voltage. It results in :

$$V_O = V_R\left(1 + \frac{R_A + R_2}{R_1} + \frac{R_A(R_1 + R_2)}{R_1(R_B + R_S)}\right) - V_i\left(\frac{R_A + R_2}{R_1} + \frac{R_A \cdot R_2}{R_1(R_B + R_S)}\right) \qquad (34)$$

Referring to Figures 34 and 35, it is possible to calculate the transconductance gain of the power amplifier. For this calculation we shall do the following approximations :

- the capacitors are practically short circuits;
- the gain A of the amplifier is very high ($A \to \infty$).

For the circuit represented in Figure 34 we obtain :

$$I_Y = \frac{R_F}{R_1 \cdot R_S} V_i \qquad (36)$$

while for the application in Figure 35 the yoke current results in :

$$I_Y = \frac{R_2 + R_A // R_B // R_C}{R_1 \cdot R_S} V_i \qquad (37)$$

Using the (31), (34), (35) and (36) it is possible to calculate the external feedback network for every different yoke known the scanning current and the midpoint output voltage.

Figure 36 : Open Loop Gain and Phase for the Application Circuit in Figure 27.

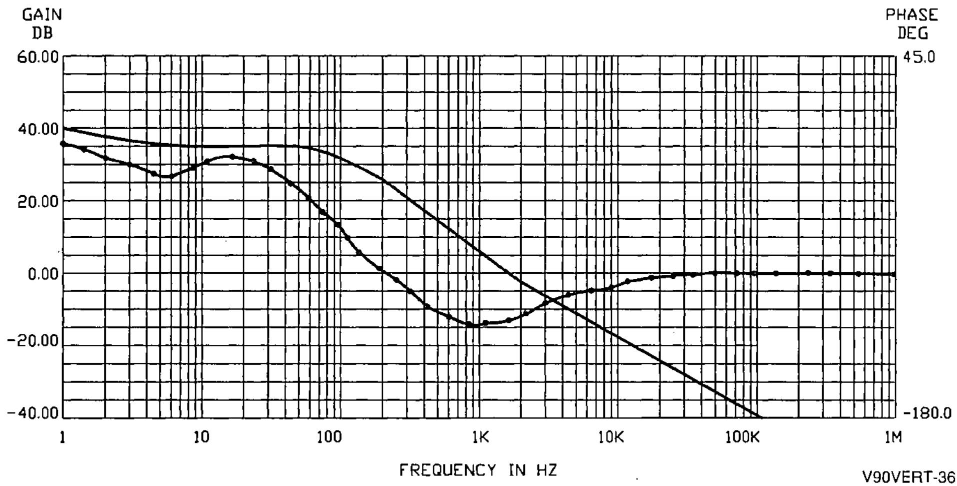
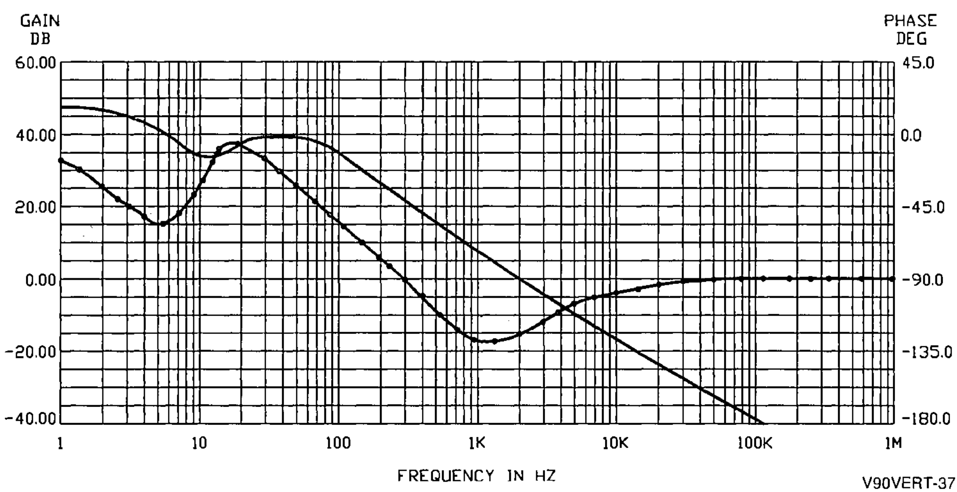
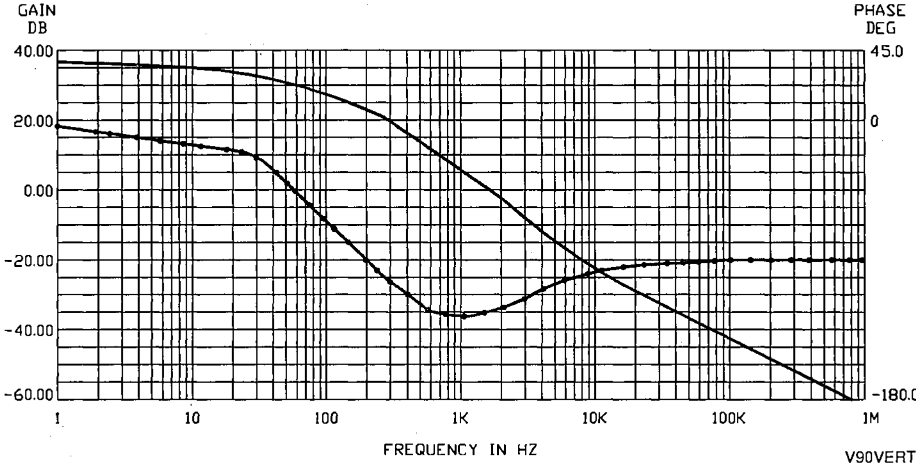


Figure 37 : Open Loop Gain and Phase for the Application Circuit in Figure 28.



We can now consider the open loop gain of the whole system amplifier plus external feedback network. This calculation is useful in order to verify that no oscillations can occur at any frequency.

Figure 38 : Open Loop Gain and Phase for the Application Circuit in Figure 29.



We shall consider some typical applications; the results are reported in Figures 36, 37 and 38.
It is easy to verify that in all cases, when the gain reaches 0dB, the phase margin is about 60°, so the stability of the system is assured.

13. MONITOR APPLICATIONS

In monitor applications the flyback time needed could be very smaller than the one we get using the minimum supply voltage calculation.

It is possible to reduce the flyback time in two different ways :
a) increasing the supply voltage, when the nominal value calculated is lower than the integrated circuit limit;
b) choosing a yoke with lower values in inductance and resistance and by supplying the circuit with the voltage needed for getting the right flyback time.

In both cases we have to calculate the biasing and the gain conditions using the nominal voltage and then we fix the supply voltage for the flyback time requested with the formula (18) :

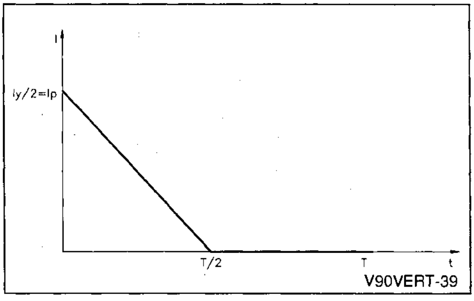
$$V_S = \frac{2}{3} \frac{I_Y \cdot L_Y}{t_F}$$

The calculation procedure for monitors is so the same as the one we have explained in the previous chapters for television applications.

14. POWER DISSIPATION

We shall now examine the power dissipation of the integrated circuit and the dimensions of the heatsink.
To calculate the power dissipated we must consider the maximum scanning current required to drive the yoke $I_{Y(MAX)}$ and the maximum supply voltage $V_{S(MAX)}$ because we have to dimension the heatsink for the worst case.
The current absorbed from the power supply is depicted in Figure 39.

Figure 39 : Current Absorbed from the Power Supply during Scanning.



The equation of the curve is :

$$i(t) = \frac{I_Y}{2} - \frac{I_Y}{T}\,t \qquad \text{for } 0 < t \le T/2$$
$$i(t) = 0 \qquad \text{for } T/2 < t \le T \qquad (37)$$

To the previous one we have to sum the DC current necessary to supply the other parts of the circuit (quiescent current).

The power absorbed by the deflection circuit is then :

$$\begin{aligned} P_A &= \int_0^{T/2} V_{S(MAX)} \cdot i(t) \cdot dt + V_{S(MAX)} \cdot I_{DC} \\ &= V_{S(MAX)} \int_0^{T/2} \left(\frac{I_{Y(MAX)}}{2} - \frac{I_{Y(MAX)}}{T}\,t \right) dt + V_{S(MAX)} \cdot I_{DC} \end{aligned}$$

The solution is :

$$P_A = V_{S(MAX)} \left(\frac{I_{Y(MAX)}}{8} + I_{DC} \right) \qquad (38)$$

The power dissipated outside the integrated circuit is formed by the three following fundamental components : the scanning power dissipated in the yoke for which the minimum resistance of yoke $R_{Y(MIN)}$ and the maximum scanning current $I_{Y(MAX)}$ must be considered, the power dissipated in the feedback resistance R_F and that one dissipated in the diode for recovery of flyback.

The power dissipated outside the integrated circuit is then :

$$\begin{aligned} P_Y &= \int_0^{T} (R_{Y(MIN)} + R_f)\, i^2(t) \cdot dt + \int_0^{T/2} V_D\, i(t) \cdot dt \\ &= (R_{Y(MIN)} + R_f) \int_0^{T} \left(\frac{I_{Y(MAX)}}{2} - \frac{I_{Y(MAX)}}{T}\,t \right)^2 dt + V_D \int_0^{T/2} \left(\frac{I_{Y(MAX)}}{2} - \frac{I_{Y(MAX)}}{T}\,t \right) dt \end{aligned}$$

The solution is :

$$P_Y = \frac{I^2_{Y(MAX)}\,(R_{Y(MIN)} + R_f)}{12} + \frac{I_{Y(MAX)} \cdot V_D}{8} \qquad (39)$$

The power dissipated inside the integrated circuit is :

$$P_D = P_A - P_Y \qquad (40)$$

The thermal resistance of the heatsink to be used with the integrated circuit depends upon the maximum junction temperature $T_{J(MAX)}$, the maximum ambient temperature T_{AMB} and the thermal resistance between junction and tab $R_{TH\ (J\text{-}TAB)}$ that is different for the various packages used. The thermal resistance of the heatsink is expressed by the following formula :

$$R_{TH\ J\text{-}AMB} = \frac{T_{J(MAX)} - T_{AMB(MAX)}}{P_{D(MAX)}} - R_{TH\ J\text{-}TAB} \qquad (41)$$

As an example we can calculate the dissipated power and the thermal resistance of the heatsink for the 26", 110°, neck 29.1mm tube for which we calculated the minimum supply voltage in chapter 11.

We shall consider the integrated circuit TDA1670A and we can suppose a maximum supply voltage of 25V.

The power absorbed from the supply is :

$$P_A = 25\left(\frac{1.2}{8} + 0.04\right) = 4.75\ W$$

The power dissipated outside the integrated circuit is :

$$P_Y = \frac{1.2^2\,(9.6 \cdot 0.93 + 1.2)}{12} + \frac{1.21}{8} = 1.37\ W$$

therefore the power dissipated by the integrated circuit is :

$$P_D = 4.75 - 1.37 = 3.38\ W$$

The thermal resistance of the heatsink, considering the $R_{TH\ J\text{-}TAB}$ for the multiwatt package of 3°C/W, a maximum junction temperature of 120°C and a maximum ambient temperature of 60°C is :

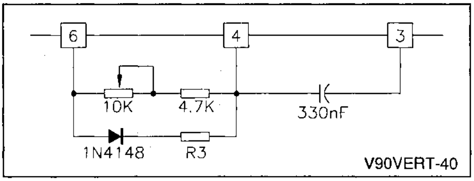
$$R_{TH\ H\text{-}AMB} = \frac{120 - 60}{3.38} - 3 = 15°C/W$$

For the same application with TDA1170S we have a thermal resistance for the heatsink of about 8°C/W.

15. BLANKING PULSE DURATION ADJUSTMENT

For the devices that have the blanking generator it is possible to adjust the blanking pulse duration. We shall consider as an example the TDA1670A; the circuit arrangement is depicted in Figure 40.

Figure 40 : Circuit Arrangement for Blanking Pulse Duration Adjustment.



By adjusting R_3 the blanking pulse duration will be adapted to the flyback time used and the picture tube protection will be ready to work properly.

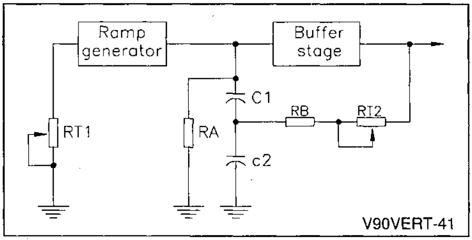
When necessary, it is possible to use a trimmer system to adjust it very carefully.

16. LINEARITY ADJUSTMENT

The complete vertical stages have the possibility to control the linearity of the vertical deflection ramp. There are two different methods to obtain the above mentioned performance.

a) For the first method we shall refer to Figure 41.

Figure 41 : Circuitry for Ramp Linearity Regulation.



The linearity regulation is obtained by means of R_A, R_B and R_{T2}.

In order to choose the right values of this components we suggest to follow the following procedure :

1 - Set the amplitude regulation potentiometer R_{T1} for the nominal raster size;

2 - Disconnect the R_A resistance;

3 - Adjust the linearity control potentiometer R_{T2} in order to obtain the top and the bottom of the raster with the same amplitude;

4 - In this condiotion the center of the raster must be narrower then the top and the bottom. If with R_A

disconnected the center is larger than the top and the bottom it is necessary to act on the feedback network. Referring to Figures 27, 28 and 29 it is necessary to increase the capacitors C_{11}, C_8 or C_6;
5 - After increasing the capacitors it is necessary to repeat the linearity adjustment (R_{12} potentiometer) in order to get the top and the bottom with the same amplitude again;
6 - Connect the R_A resistor and repeat the linearity adjustment (point 3 regulation);
7 - Check the top and the bottom amplitude comparing it with the center. If the center amplitude is still narrower it is necessary to reduce R_A. If the center amplitude becomes larger it is necessary to increase R_A.

Note : Every time the linearity conditions are changed (for adjusting or setting) before checking the linearity status, the point 3 adjustment must be repeated.

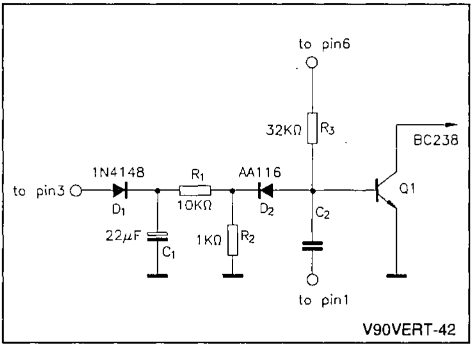
b) For the second method we shall refer to Figure 28.
In this case the linearity regulation is obtained acting directly on the feedback network, that is substituting the R_8 resistance with a potentiometer. This solution is cheaper than the first one, because it is possible to save the resistors R_A, R_B (see Figure 41), the potentiometer R_{T2} and to use only a capacitor instead of the series C_1 and C_2.
On the other hand a disadvantage is due to the fact that the resistance R_8 influences not only the linearity of the ramp but also the gain of the amplifier, as it can be seen in the equation (36). So to perform a linearity adjustment it is necessary to act at the same time on the potentiometer in the feedback loop and on the potentiometer R_{T1} (see Figure 41) in order to correct the vertical amplitude variations.
On the contrary, in the method a) the linearity control network doesn't influence any other parameters. this is the reason why the a) method is generally adopted by all television set producers.

17. FACILITIES AND IMPROVEMENTS

In this section we shall briefly examine some facilities which may be useful to improve operations of the television set.

a) Blanking generator and CRT protection for TDA1170 family.
At pin 3 a pulse is available which has the same duration and phase as the flyback and amplitude equal to the supply voltage.
If the retrace duration is not sufficient for carrying out correct vertical blanking, for instance in the presence of text and teletext signals the circuit of Figure 42 can be used.
The true blanking generator is formed by Q_1,R_3 and C_2 and the blanking duration is dependent upon the values of R_3 and C_2. The other components are used for picture tube protection in the event of loss of vertical deflection current. If for any reason there is no flyback, the transistor Q_1 is permanently inhibited and provides continuous switch off which eliminates the white line at the center of the screen. Thermal stability and stability with the supply voltage is good in relation to the simplicity of the application.

Figure 42 : Blanking Generator and CRT Protection for TDA1170.



b) Vertical deflection current compensation to maintain picture size with beam current variations.

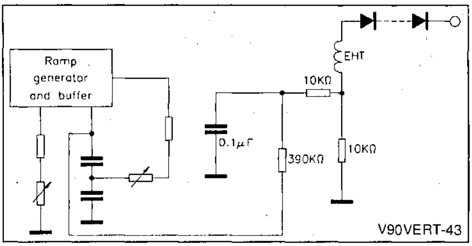
Changes in the supply voltage or the brightness and contrast controls will bring out changes of the beam current, thus causing EHT and picture size variations.
The rate of change of the picture size is mainly dependent upon the EHT internal resistance.
In order to avoid variations of the vertical picture size it is necessary to track the scanning current to the beam current. Because the tracking ratio :

$$\frac{\Delta I_{YOKE}}{\Delta I_{BEAM}} \cdot 100 \qquad (42)$$

varies from one chassis design to another, three suggested tracking circuits are shown in Figures 43, 44 and 45.

The circuit in Figure 43 adopts the straight forward technique of linking the vertical scanning current directly to the beam current .Its drawback lies in the fact that a long wire connection is required between the EHT transformer and the vertical circuit, and the layout of this connection could be critical for flashover.

Figure 43 : Circuit for Vertical Scanning Current Variation according with the Beam Current.



The circuit of Figure 44, which links the vertical scanning current directly to the supply voltage, is the simplest one. Its drawback could be incorrect tracking ratio and ripple on the supply voltage.To overcome the drawbacks of the preceding circuit it is usefull to filter out the supply voltage ripple and adjust the tracking ratio by transferring the supply voltage to a lower level by means of a Zener diode as shown in Figure 45. Tracking ratio is adjusted by choosing a suitable Zener voltage value.

Figure 44 : Circuit for Vertical Scanning Current Variation according with the Supply Voltage.

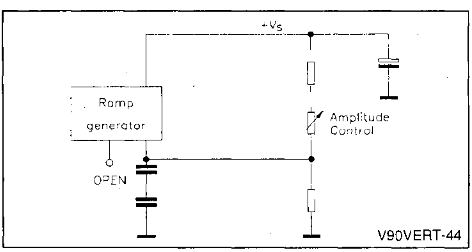
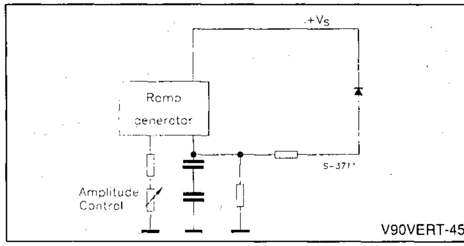


Figure 45 : Circuit for Vertical Scanning Current Variation according with the Supply Voltage.



18. GENERAL APPLICATION AND LAYOUT HINTS

In order to avoid possible oscillations induced by the layout it is very important to do a good choice of the Boucherot cell position and ground placing. The Boucherot cell must be placed the most possible closed to the vertical deflection output of the integrated circuit, while the ground of the sensing resistor in series connected with the yoke must be the same as the one of the integrated circuit and different from the one of other power stages. Particular care must be taken in the layout design in order to protect the integrated circuit against flashover of the CRT. For instance the ground of the filter capacitor connected to the power supply must be near the integrated circuit ground.

19. REFERENCES

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