VERY HIGH SPEED DATA ACQUISITION

Pertinent Information About High-Resolution "Video" Converters

by Ed Graves

Until now, we have given readers of this Journal and other Analog Devices publications little opportunity to find information about very high-speed converters and their applications. Now, in this and the following pages, our colleagues at the Computer Labs Division seek to provide you with the information necessary for a basic understanding of the technology. In the future, you can expect to read more about the increasing applications of these techniques and some exciting new products that will place these powerful tools more firmly within your grasp.

The world of multi-MHz conversion differs, to a greater or a lesser extent, from the lower-frequency fields: in circuitry, terminology, applications, testing, and emphasis. As the uses of digital technology spread, the analog-digital interface must handle increased amounts of information; for this reason, knowledge of this heretofore esoteric technology becomes increasingly necessary, even for engineers not specifically involved in radar or TV projects.

The discussion that follows is not intended to be complete or all-encompassing; we hope that it will tempt you to read further in the literature (some of it available from Analog Devices). A brief Bibliography, with a great deal of fanout, appears at the end of this article.*

WHAT DO WE MEAN BY "VIDEO"?

The spectrum of high-resolution conversion equipment that is commercially available in the form of "subsystem-solution" products* covers the range of resolutions from 4 to 13 bits, with sample (word) rates from 2MHz to more than 100MHz. Such products are designed to encode or decode analog signals with maximum bandwidths exceeding 1 to 2 MHz.

A good example of such a device is the MOD-1005 a/d converter, depicted on this issue's cover. Characterized by 10-bit resolution and a 5MHz sample (or throughput) word rate, this converter is really a complete single-channel data-acquisition subsystem; it includes an input track-and-hold, a 10-bit encoder, an output latch, and all the necessary timing circuitry – all on a single circuit card suitable for plugging into a mother board. The only external connections needed to digitize an analog input are external power supplies and an *encode* (convert) pulse. The MOD-1005 has a systemic aperture uncertainty (at the instant the sampling switch is opened) of ±25ps (25×10^{-12} s). This means that analog signals having frequencies in excess of 6MHz can be digitized with slew-rate errors less than *1/2LSB* (0.05% of full scale).† That is,

$$f_s = \frac{2^{-n}}{2\pi\tau_A} = \frac{1}{2\pi \cdot 1024 \cdot 25 \times 10^{-12}\text{s}} = 6.2\text{MHz} \qquad (1)$$

Other typical video a/d converters available from us include the MATV-0820 (8 bits at 20MHz), the CLB-1310 (13 bits at 10MHz), and the CL-7120 (10 bits at 20MHz). The overriding advantage of these converters is that they are *complete*. No extensive interface design is required to use them; in effect, just apply power, and they are ready to go!

*Use the reply card for a short-form catalog, for data on specific products mentioned here, or for reprints of articles available from Analog Devices.

†If the input signal in 5MHz sampling must be restricted to the Nyquist rate (2.5MHz) or less, the slewing error will be considerably less than 1/2LSB for a 10-bit conversion.

ARE YOU A POTENTIAL "VIDEO" CONVERTER USER?

With the advent of less-expensive monolithic and hybrid state-of-the-art components, many new applications for video-converter products are surfacing that were out of the question just a few years ago because of their high cost. High-resolution converters are now used extensively in commercial, industrial, military, and research applications, such as radar, sonar, television, communications, spectrum analysis, and others. Figure 1 illustrates an application in the field of spectrum (or signature) analysis.

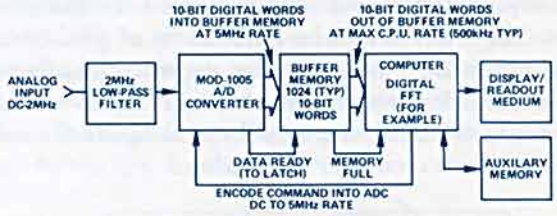

Figure 1. Typical digital signal-processing system.

In this example, the MOD-1005 ADC is used to digitize a band-limited analog signal at sample rates up to 5MHz. The digital output of the a/d converter is entered into a buffer

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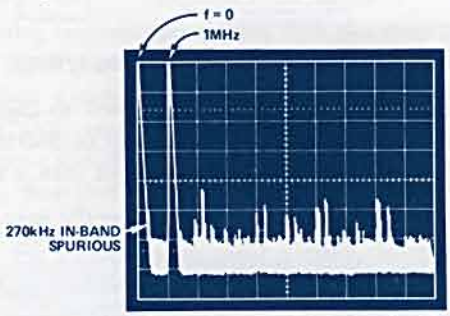
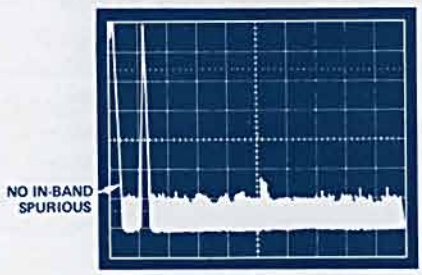
memory capable of writing large blocks of data at this rapid rate. Under control of the central processing-unit (CPU), the data is then shifted into the computer for number-crunching.

These days, it is feasible to consider using a microprocessor to implement a relatively inexpensive spectrum analyzer by the execution of Fourier-transform algorithms. Since the μP, in its least-expensive form, is a slow device, the buffer memory is needed to hold the rapidly acquired fast data from the converter for processing at a comfortable pace. Such a system, using a fast ADC – such as the MOD-1005, in this case – makes analysis of the spectra of 10-bit signals, at rates extending into the video range, economically feasible. The same basic system concept can be used for transient analysis, using proper input signal-level detection and processing (triggering).

The "system-solution" approach can be applied to the design and application of fast *d/a converters*, too. In many applications, including video, the effect of *glitches* in the DAC output can be intolerable. Glitches are the result of a combination of causes: bit-timing asymmetry, conversion-circuit switch asymmetry, circuit layout, and numerous less-than-obvious sources. The errors caused by a typical set of glitches can be seen in Figure 2a, which illustrates the spectrum of a reconstructed 1.05MHz waveform, sampled at a 14.32MHz rate. Note that filtering the DAC output will not eliminate the in-band spurious products created by the glitch.



(a) Spectrum without deglitching.



(b) Spectrum of deglitched waveform.

Figure 2. Deglitcher in action. Spectrum of 1.05MHz sine wave sampled and reconstructed at 14.32MHz rate. Scales: 1MHz/div horizontally, 10dB/div vertically. Spreading of single frequency spikes is due to filter limitations in spectrum analyzer. Note 270kHz spike in (a) removed in (b).

A good solution is to use a video DAC that includes a track-and-hold type deglitcher (Figure 3). In this type of d/a subsystem, the T/H seizes the DAC output just before the DAC is updated and holds the output constant while the d/a converter is changing states. During this time, the output ignores the glitch. After the DAC has had time to settle, the T/H returns to the *track* state, and the subsystem output slews smoothly to the next level, eliminating the effect of the nonlinear glitches. As Figure 2b shows, the remaining considerably smaller noise components tend to be of essentially uniform amplitude; they can be handled with relative ease by filtering.

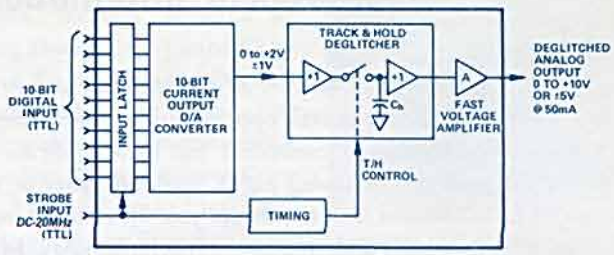


Figure 3. Functional diagram of MDD-1020A deglitched D/A subsystem module.

Applications for "video" d/a-conversion subsystems include cathode-ray-tube graphics displays, for X & Y (position) and Z (intensity) modulation, fast X-Y plotters, composite television-picture reconstruction, digitally controlled voltage-controlled oscillators (VCO's), and others.

CONVERSION TECHNIQUES

The first commercially available high-resolution video a/d converter, originated more than a decade ago by Computer Labs, utilized the *serial (or cascade) Gray code* technique. It was implemented by having one basic gain-element and one digital comparator per bit. The resulting output, in Gray code*, was converted to binary within the a/d converter.

A block diagram of a serial Gray-code converter is shown in Figure 4. For an n-bit converter, there are n cascaded decision stages. Each stage exhibits a transfer characteristic similar to the ones shown, with gain of +2 for inputs from 0 to $E_{MAX}/2$ and gain of –2 for inputs from $E_{MAX}/2$ to E_{MAX}. For values of input between 0 and $E_{MAX}/2$, the digital bit value is 0, and for inputs between $E_{MAX}/2$ and E_{MAX}, the digital bit value is 1.

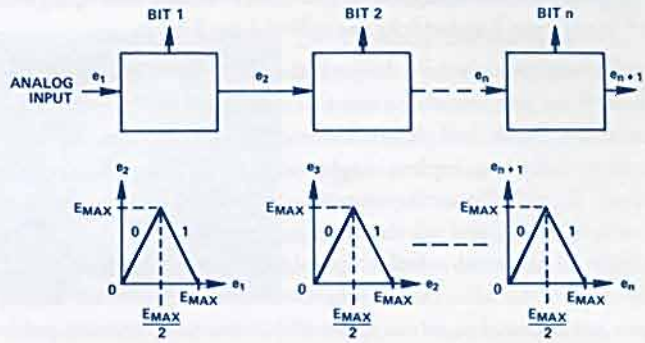


Figure 4. General A/D converter with Gray-code output.

When an analog signal, e_1, is applied at the input, and held constant by a track-and-hold, it will propagate quickly through the stages and produce a steady state in which the outputs of the stages, both analog and digital, bear a unique relationship to the analog input. For example, if the analog input to the first stage is equal to $E_{MAX}/3$, the digital output will be "0", since the input is less than $E_{MAX}/2$, and the analog output will be $2E_{MAX}/3$. This output, e_2, applied to the next stage, will produce an analog output of $2E_{MAX}/3$ and a digital output of "1". In this example, the outputs of all the following stages will be $2E_{MAX}/3$, and the digital outputs will be "1", hence

*See *Analog-Digital Conversion Notes*, D. H. Sheingold, ed., 1977, pages 102-104 for a discussion of Gray Code and its relationship to binary. Analog Devices, Inc., Box 796, Norwood MA 02062, $5.95.

the output word will be 01111...1. That is the Gray Code for $E_{MAX}/3$ can be demonstrated by performing a conversion from Gray code to binary.*

The *complete time for one conversion* is determined by the overall propagation delay through the ADC and the settling time of the last stage that settles. However, the digital output of each stage can be latched as soon as that stage has settled, and a new conversion can, in principle, be started as soon as the first bit has been latched, permitting the conversion *rate* to be based on a much shorter time interval than the time for a complete conversion (cf. delay lines). By contrast to methods, such as successive approximations, in which decisions must be made one bit at a time, this technique can permit encoding at rates approaching word-at-a-time.

The serial (actually serial-analog, parallel-digital) Gray-code technique is still to be found in many of our video-converter products, such as the MATV series ADC's. The technique requires the use of extremely wide-band amplifiers, which must at the same time exhibit extraordinary dc stability. In the real world, there is a practical limit to the number of stages that can be cascaded; for example, the 8-bit MATV series ADC's use the serial Gray-code technique for the first six bits and a parallel "flash" encoder (see below) for the remaining two bits. Such combinations of techniques have been used to construct a/d converters with resolutions of up to 13 bits and word rates up to 10MHz.

Another useful, and increasingly popular, type of conversion technique is the all-parallel, or "flash" encoder, illustrated in Figure 5. It calls for 2^{N-1} analog comparators, where N is the number of bits. For an eight-bit encoder, this requires 255 comparators; for 10 bits, 1023 comparators are needed. The V_{REF} of each comparator is set by I_{REF} and the total resistance below its level; the V_{REF} of each comparator is one LSB higher than that of the comparator below it.

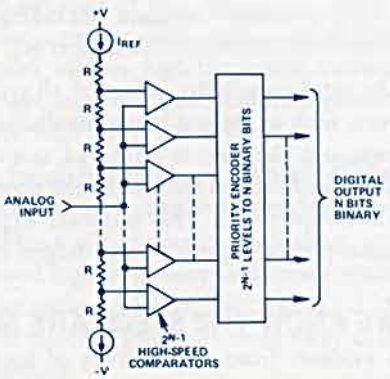


Figure 5. N-bit "flash" encoder.

When an analog input signal is present at the input of the comparator bank, all comparators which have V_{REF} below the level of the input signal will assume logic "1" output. The comparators with V_{REF} above the input signal level will have logic "0" output. The output of the comparator bank is applied to a digital priority encoder, which converts the "thermometer" input to a binary output. Since the comparator inputs and outputs have parallel configurations, the "flash" converter is extremely fast.

It is easy to see that the flash encoder, though simple in concept, is an extremely complex device to build, requiring a very high parts count and high power dissipation for high-speed use beyond about 8-bit resolution. In its lower-resolution versions, the flash encoder can be a useful subsystem component upon which complex high-resolution ADC's can be based. The 10-bit MOD-1005, which uses flash encoders in a unique *digital subrange correction* technique, is a pertinent example of this approach, employing *subranging*.

An example of subranging, as applied to an 8-bit a/d converter, is shown in Figure 6. In this encoder, the analog signal from a track-and-hold is applied through two buffer amplifiers to a 4-bit flash encoder and a summation network simultaneously. The 4-bit encoder converts the signal to the four more-significant bits of digital information; these are stored in a holding latch and also applied to a 4-bit d/a converter. The 4-bit DAC must be *at least 8-bit accurate* in this application. The inverted analog output is summed with the buffered analog input; the output of the summation network is the difference between the original input signal and the quantized value represented by the first four bits.

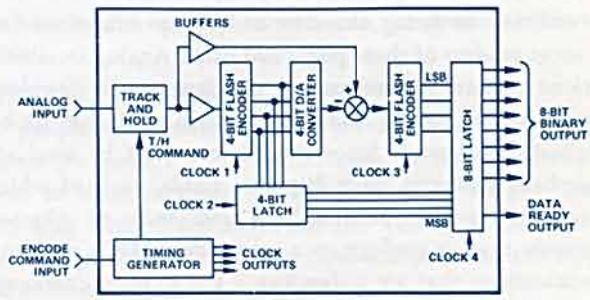


Figure 6. 8-bit subranging A/D converter.

4-bit "residue" is then converted to digital form by a 4-bit flash encoder and provides the four less-significant information. The outputs of the first 4-bit holding latch and the second 4-bit encoder are then combined in an output latch to yield an 8-bit all-parallel output from the ADC.

Timing is of vital importance in this type of ADC, since each element of the conversion process must be allowed time to settle adequately before the required strobe signals are applied. The subranging high-speed ADC is perhaps one of the most challenging kinds of converter to design and manufacture, because both speed and accuracy are essential for each circuit element. It is not easy, even in 8-bit video a/d converters of this design, to avoid differential-linearity discontinuities around the 1/32-scale (Bit 5) transition points, due to mismatch between the first and second encoding sections. These discontinuities, which could exceed 1 LSB and cause skipped codes, can be eliminated by careful design and – more powerfully – by the use of a "smart" encoding technique called *digitally corrected subranging* (DCS).

In converters using DCS, the architecture is very similar to that of other converters employing subranging, but the analog signal is *over-resolved*; the excess resolution is used in digitally cor-

*In a Gray-code-to-binary conversion, the MSB is left unchanged. Each succeeding bit of the Gray-code word determines whether the binary bit is to be changed (1) or unchanged (0). In this example, the corresponding binary word is 0 1 0 1 0 1 . . . . When evaluated in fractional binary ($2^{-2} + 2^{-4} + 2^{-6} + 2^{-8} + \ldots$), the sum amounts to 0.333. . .

recting incremental errors that are inherent in subranging converters employing practical components. The technique, used in the MOD-1005, is outlined in Figure 7.

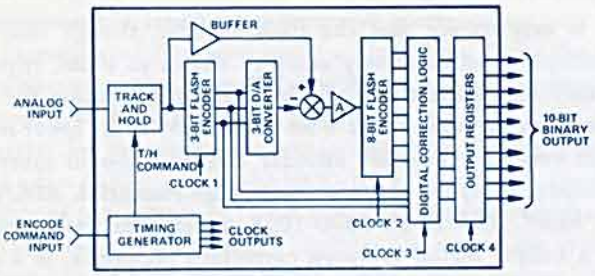


Figure 7. MOD-1005 A/D converter employs digitally corrected subranging (DCS).

Though basically similar to the 8-bit ADC shown in Figure 6, the MOD-1005 uses a 3-bit flash encoder in the front end and an 8-bit flash encoder as the second bank. The 11 bits that are encoded, combined with digital correction logic and a *12-bit-accurate 3-bit DAC*, serve to preserve 10-bit accuracy at the output at word rates through 5MHz. Further developments in hybrid and monolithic technology promise to yield even higher resolutions and speeds utilizing this technology in the very near future.

FAST CONVERTERS – A DIFFERENT WORLD

In addition to being characterized by specifications familiar to most readers of these pages and other Analog Devices publications (linearity, temperature coefficients, etc.), video converters require further characterization in terms that are heavily application-oriented. Since the devices must be used at very high bandwidths in quite-disparate fields, each of which has developed specific terminology and tests to characterize dynamic system performance, our video ADC's require some specifications that are unfamiliar – and in some cases unguessable – to the low-frequency *aficionado*.

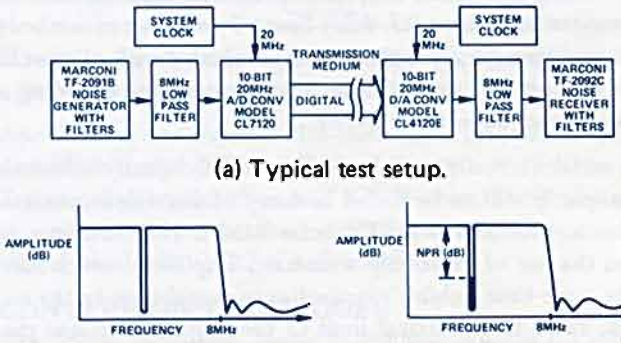
Some of these specifications appear in Table 1, together with a list of fields for which they are principally applicable. Since their definitions would require lengthy explanations, which the limited space in this brief survey does not permit, we urge the interested reader to use the reply card to request those reprints, listed in the Bibliography with an asterisk (*), that seem most relevant.

SPECIFICATION	APPLICATION
Signal-to-noise ratio (S/N)	Radar, communications, spectrum analysis
AC Linearity	Radar, spectrum analysis
Noise power ratio (NPR)	Communications
Two-tone intermod distortion	Communications, spectrum analysis
Transient response	Transient analysis, radar
Overvoltage recovery	Radar
Aperture uncertainty	All
Differential phase	Television
Differential gain	Television

Table 1. Dynamic specifications typically applied to high-speed converters.

However, as an example of how one of these specifications would apply to a real-world application, let's consider *noise-power ratio* (NPR), a specification which is of particular importance to users of telecommunications transmission equipment. With the advent of a/d and d/a converters for coding/decoding (CODECS), which have the resolution and speed to handle baseband signals greater than the basic 4kHz voice channel, this spec has recently gained increased significance.

NPR is the measure of the spectral power of all contributed errors, such as intermodulation and harmonic distortion, in a narrow frequency-slot within the baseband of the composite signal being processed. An example of such a communication system, including the testing hookup that may be used, is shown in Figure 8.



(a) Typical test setup.

(b) Transmitted spectrum, with slot.

(c) Received spectrum, slot partly filled with garbage.

Figure 8. 1600 channel digital communication system.

In such a system, the baseband signal is dc to about 8MHz, and the a/d and d/a encoding rates are 20 megawords per second. The NPR test consists of encoding a limited band of white noise, being produced by the noise generator, and examining this signal at the output of the DAC, using the noise receiver. The noise generator is equiped with band-stop filters, which eliminate very narrow "slots" from the transmitted frequency spectrum (b). At the receiving end, the noise receiver is equipped with complementary filters to allow the receiver to examine power spectral-density of the "noise" contributed by the transmission medium (including the ADC and the DAC) within these ideally noiseless slots (c).

This noise, the total cumulative effect of all transmission and encoding errors, such as IM and harmonic-distortion products, aperture errors, and the like, is displayed as a weighted ratio of the output noise found in the slot to the power of the total transmitted noise-spectrum. This number, expressed in dB, is called "noise-power ratio" – the larger its magnitude, the better.

HOW DO WE KNOW THE SPECS ARE MET?

It should be evident, from the diversity of applications, that the field of high-resolution video conversion is becoming more complex. While every user of these conversion products wants the "best device for the job," the many different types of users have equally many divergent interests in differing operational parameters, none of which is easy to measure objectively. To meet this variety of requirements, our engineers and technicians at Computer Labs have devised a sophisticated computer-controlled testing system, which goes well beyond the "dc linearity testing" that is often adequate for conversion equipment designed for use at conversion rates well below 1MHz.

Since most high-speed conversion products are used with computers or microprocessors, we have devised a method of ADC and DAC testing which uses a DEC PDP-11 minicomputer to

analyze the dynamic characteristics of the product under test. If you will refer back to Figure 1, you can get an idea of how this works. The ADC under test is provided with a test signal of known spectral content. The computer can then analyze the converter's output under controlled conditions to provide assurance that the device will meet almost any specification within its capability for which a test can be programmed. Various input signals, such as fast linear ramps, pure sine waves, or white noise can be used as inputs to test dc and ac linearity, distortion products, and NPR – just to name a few.

All these tests (and more) can be performed rapidly under software control on a time-sharing basis from different locations in our factory. The system is capable of testing ADC's with analog input bandwidths up to 10MHz, encoding rates up to 20MHz, and resolutions up to 16 bits. In addition, up-to-date specialized system test equipment is available to perform tests calling for specific configurations of test hardware.

TROUBLE – AND HOW TO AVOID IT

Probably the most ubiquitous problem in the implementation of high-speed systems involving analog signals and a/d conversion is noise. This should not be surprising when you consider that the value of the LSB for a 13-bit ADC with a full-scale range of ±2V is less than 500μV – which makes the ADC a pretty good radio receiver: with 250μV p-p noise at the input, the LSB would be lost. Here are some key suggestions for minimizing the effects of noise and interference in high-speed conversion systems.

- Use massive, low impedance ground systems. The analog and digital grounds are connected together inside converters of these types, so bus bars are essential for system grounding and power distribution; use lots of ground plane on PC boards.

- Use linear regulated power supplies wherever possible. Yes, switching regulators are more efficient, and the ripple and noise specs look pretty good – but remember that the noise specs for most supplies of this type are in terms of *rms*. The peak-to-peak output noise of switchers can be several hundred millivolts – with vicious high-frequency components. Such spikes love to get into the most-elaborate grounding systems and create havoc with video converters.

- Watch out for *digital* feedback. (What?) If the ADC's output lines are in close proximity to the analog input, the output signals can feed back into the input. Remember, you're working with rf signals and high-frequency front ends – many involving frequencies that exceed 50MHz. Use coaxial cabling for analog signals wherever possible and route them away as far as possible from the digital junk.

- Use lots of power-supply bypassing capacitors. They are cheap compared to the cost of debugging and adding them later. Bypass each power-supply line with a good ceramic (0.1μF) in parallel with a good tantalum (1 to 10μF) capacitor to ground right at the converter. When in doubt, add more capacitors – you can always take them out later (after carefully checking) if you need to save a few cents of parts cost.

- When interfacing, use source and load terminations for analog signals wherever possible to prevent reflections on the lines. Keep impedances as low as feasible, bearing in mind that the lower the impedance, the lower the probability of noise pickup. (On the other hand, the lower the impedance, the more difficult it is to drive, and the higher the circuit distortion and power-driving requirements.) Observe proper shielding techniques. One of the most-commonly encountered sources of difficulty in this regard seems to be the use of unshielded twisted wiring. Avoid it like the Plague – unless there's no other way.

EXPENSIVE BUT MORE COST-EFFECTIVE

As we have shown, video converters, such as the MOD-1005, are (the) critical building blocks in wide-band signal-processing systems. Since they straddle the gap between component and system engineering, and between analog and digital technology, they are among the most misunderstood of system elements and the most tricky to implement (much less design!) Though they are considerably more expensive than their low-frequency cousins, their cost has usually been small in relation to the cost of systems in which they have been used.

Consequently, with the advent of complete "system-solution" converter products having increasingly smaller size and lower cost – with every reason to expect a continuation of the trend – systems engineers should think twice about committing expensive design talent and hardware toward designing their own high-speed a/d conversion subsystems or seeking to implement patch-work solutions. Such efforts generally turn out to be more costly and time-consuming than using complete, tested, guaranteed devices, backed up by the technical commitment and knowhow of the Computer Labs Division of Analog Devices. The wheel would be easy to re-invent, compared to the video ADC!

ACKNOWLEDGEMENT

Many people have contributed to the advancement of video-converter technology at Computer Labs. In particular, thanks are due to these members of our engineering staff – Bryan Smith, Walt Kester, Bill Pratt and Joe Young, – for their invaluable help in the preparation of this article and the Application Brief on page 9.

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BIBLIOGRAPHY

SUGGESTED READING – HIGH-SPEED CONVERTER TOPICS

Only starred items (*) are available from Analog Devices

**Short-Form Catalog*, Computer Labs Division of Analog Devices, Inc., 1978

*Kester, W.A., "Characterizing and Testing A/D and D/A Converters for Color Video Applications", *IEEE Transactions on Circuits and Systems*, Volume CAS-25, No. 7, July 1978

*Oliver, W., "White Noise Loading of Multi-Channel Communication Systems", Marconi Instruments, 1964

*Pratt, W.J., "Test A/D Converters Digitally", *Electronic Design*, December 6, 1975

Schmid, Hermann, *Electronic Analog/Digital Conversions*, Van Nostrand Reinhold Company, New York, 1970

*Smith, B.F. and Pratt, W.J., "Understanding High-Speed A/D Converter Specifications", Computer Labs, 1974

Digital Video, Society of Motion Picture and Television Engineers, 862 Scarsdale Ave., Scarsdale, N.Y. 10583, March, 1977

"Matthey Video Filters", Catalog, Television Equipment Associates, South Salem, N.Y.

Bosch, B.G., "Gigabit Electronics - A Review", *Proceedings of the IEEE*, 67-3, March, 1979, 340-379