Dc restorer for video use offers ultra-stability

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A sample-and-hold technique, along with strong degenerative feedback, permits an active dc restorer to operate with very high stability over a wide temperature range. Restoration stability can be maintained to within 30 microvolts, even in the presence of a dc offset voltage as large as 100 millivolts.

The circuit is useful in radar applications, where it is often essential to peak-detect or integrate video signals relative to a stable dc reference. This is especially true if the video sensor contains diodes that have a temperature-dependent offset voltage.

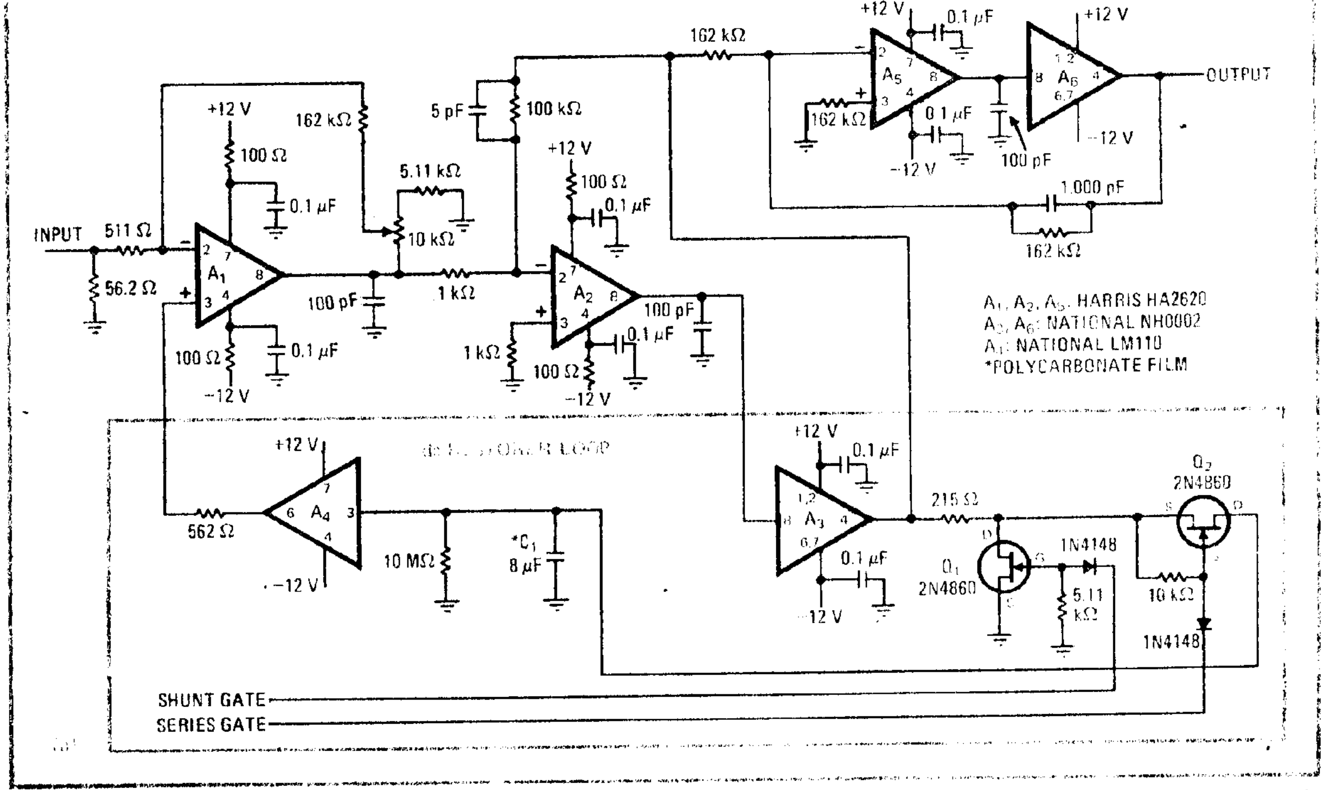
The dc restoration must be performed without any temperature-induced offset voltage, since dc coupling must be preserved in the video processing (peak detection or integration) following dc restoration. Accurate signal detection, then, heavily depends on providing a stabilized dc restoration level. The video output signals must be independent of any thermal variations that may occur in the video detector and dc restorer.

Conventionally, a dc restorer operates at relatively high signal levels and requires considerable video gain prior to dc restoration. Moreover, a dc restorer generally employs a temperature-compensated zener diode, and two matched diodes to keep the dc restored level relatively constant over a wide temperature range. But even with the best matched diodes and the most stable temperature-compensated zener, the dc restored level cannot be made more stable than ±10 mv over a 100°C temperature range. With the dc restorer shown here, however, stabilities of 30 μV can be established at extremely low video levels.

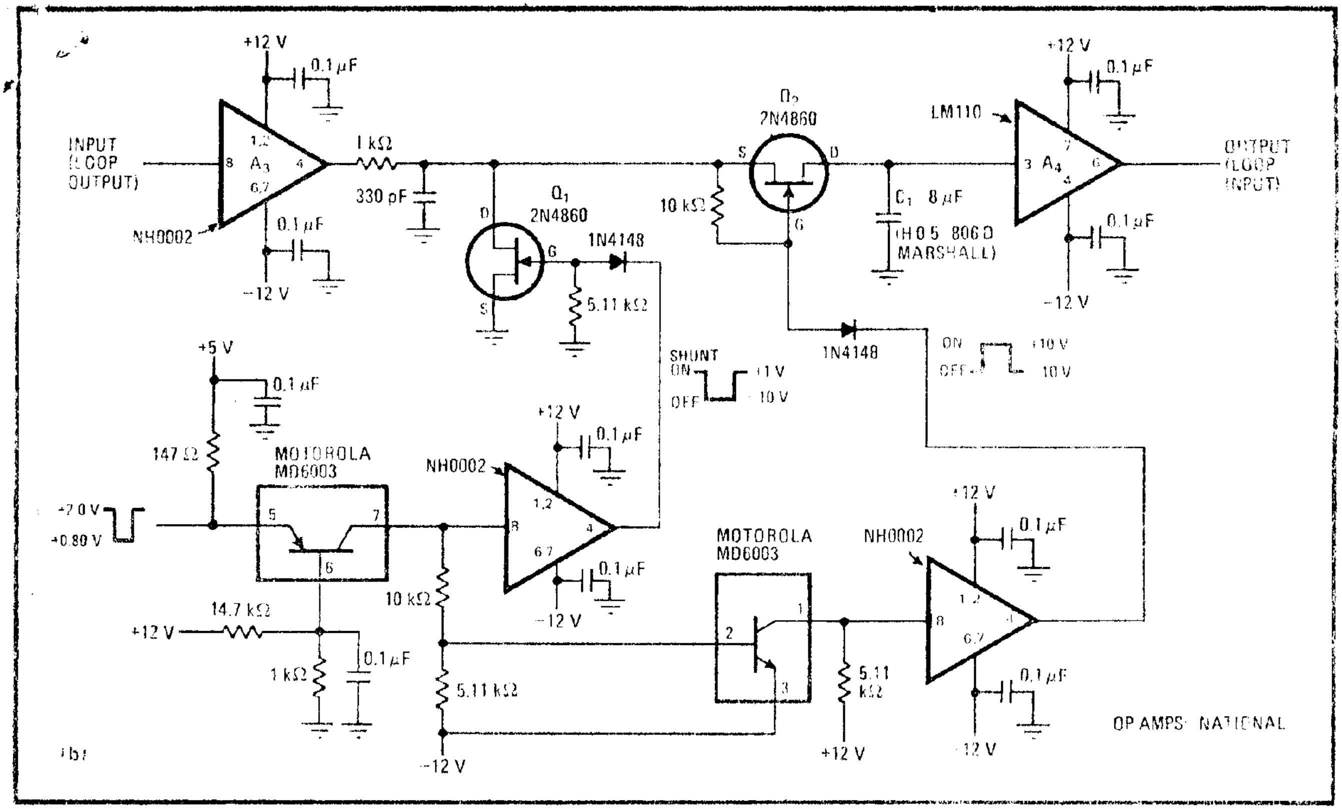
A complete video amplifier employing this improved dc restoration technique is drawn in (a). In this circuit's sample-and-hold scheme, the dc output of a dc-coupled amplifier is sampled over a 50-microsecond gating interval. It should be noted that dc coupling must be maintained from the input (sensor) through to the output integrator or peak detector. As a result, dc signal changes longer than the sensor's thermal time constant, which is typically less than 10 milliseconds, can be recognized as a valid signal/target by the peak detector or integrator.

The full schematic of the dc-restorer section of the video amplifier is given in (b). During the dc-restoration interval, the FET shunt gate, Q_1, is open, while the FET series gate, Q_2, is closed. During the gating interval, sampling capacitor C_1, which is a highly temperature-stable polycarbonate-film capacitor, charges to the average noise level present at the output of amplifier A.

When the sampling gate is closed, the circuit's sampling process activates a degenerative-feedback loop that forces the average signal value at A_3's output to approach the signal-noise level. In effect, the dc level at the noninverting terminal of input amplifier A_1 is forced to match the dc level at A_1's inverting terminal to



Emphasizing stability. Dc restoration loop of video amplifier (a) allows the amplifier to match dc input levels to within 30 microvolts, in spite of widely varying temperatures. The sample-and-hold circuitry of the dc restorer loop is shown in (b). During the gating interval, which is 50 microseconds long, FET shunt gate Q_1 is off, FET series gate Q_2 is on, and capacitor C_1 (a temperature-stable unit) charges.



within 30 μV. During the signal processing interval, when shunt FET gate Q_1 is on and series FET gate Q_2 is off, the voltage across capacitor C_1 establishes an ultra-stable dc-restored level at the positive input to amplifier A_1 as a reference for detecting whatever video signals may be present at the negative input of A_1.

To realize a high degree of dc-restoration stability within the gating aperture, it is essential to select op amps for amplifiers A_1 and A_2 that have fast slew rates. This is why Harris' type HA2620 op amp, which has a gain-bandwidth product of greater than 30 megahertz, is used for both A_1 and A_2. Amplifier A_4 is a high-stability buffer that serves as a high-input-impedance load for the sampling capacitor, C_1.

This active dc restorer can reduce a 100-mV dc offset at the sensor to an equivalent dc offset of less than 30 μV. And because of the low leakage of the sampling gate, the stored charge on capacitor C_1 is not disturbed during the hold interval, even if a 10-V signal is present at the gate input.

The forward gains (80 decibels) of amplifiers A_1, A_2, and A_3 contribute to the degenerative-feedback loop during the dc restoration interval, forcing A_1's positive input to follow the dc offset present at A_1's negative (sensor) input. The circuit's integrating stage containing amplifiers A_5 and A_6 must be placed outside the dc-restoration loop, since the fast slew rate of the forward-control loop must be preserved during the dc restoration interval.

For the circuit to operate properly, the input-signal condition must be known during the dc-restoration interval. In radar systems, this time occurs between pulse transmission and signal reception; for television signals, this time occurs during the sync tip transmission. □