Buffered Multiplexers for Video Applications

by Eamon Nash

Video functions, such as scanners, video routers, and pixel-in-pixel switching are generating a need for high-speed switching with multiplexers (muxes) and crosspoint switches. Increasing system compactness demands switch ICs with low power consumption and increased functionality, such as the ability to drive 75-Ω or 150-Ω loads without additional buffering. They also require good video specifications, e.g., low differential gain and differential phase, good gain flatness, low crosstalk, and fast settling.

Figure 1 shows block diagrams of the AD8174 and AD8180, two members of a new family of buffered analog multiplexers (muxes), distinguished by excellent video specifications at high speeds and very low power consumption. The **AD8180** is a single 2-to-1 mux; the AD8182 (not shown) is a dual version. Both devices offer a –3-dB bandwidth of 750 MHz and a slew rate of 750 V/µs. With > 80 dB of crosstalk rejection and isolation at 5 MHz, they are useful in many high-speed applications. The differential gain and differential phase errors of 0.02% and 0.02°, plus 0.1-dB flatness to beyond 200 MHz, make them ideal for professional video muxing. Their 10-ns switching time makes them an excellent choice for pixel switching (picture-in-picture), while consuming less than 3.8 mA on ±5-V supplies.

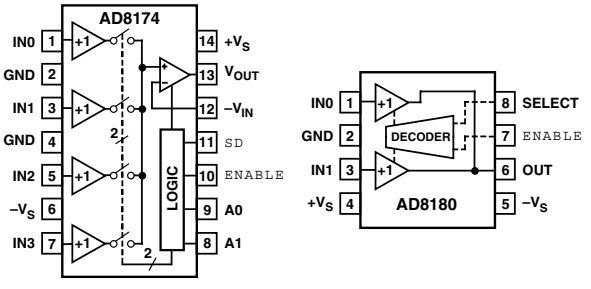

Figure 1. Block diagrams of the AD8174 and AD8180.

The **AD8174*** is a high-speed 4-to-1 multiplexer. Not shown is the AD8170*, a 2-to-1 mux with similar specs. These devices offer 200-MHz –3-dB signal bandwidth, slew rate greater than 1000 V/µs, and 0.1-dB gain flatness to 80 MHz. With a low 75 dB of crosstalk at 5 MHz, these devices are useful in many high speed applications.

The AD8170 and AD8174 contain a current-feedback output amplifier, whose gain can be programmed using external resistors. The amplifier has high output drive current of 50 mA and can drive a back-terminated 75-Ω load (R_L=150 Ω) to ±3.8 V. Power consumption is low at 8.25 mA (AD8170) and 9.7 mA (AD8174) from a ±5-V supply.

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Self-contained buffering reduces power consumption, saves board space, and allows direct connection of muxes to high speed ADCs. This is especially important in the case of CMOS ADCs, which generally have variable input impedance, associated with switched capacitance.

APPLICATIONS

An 8 × 2 Crosspoint Switch: While 8 × 8 and 16 × 16 crosspoint switches are commonly available, crosspoints with arbitrary numbers of inputs and outputs still must be designed using multiplexers as building blocks.

Figure 2 shows a modular 8 × 2 crosspoint switch that uses 4 AD8174 4-to-1 buffered muxes, two per 8-to-1 multiplexer channel. The $\overline{\text{Output Enable}}$ function on each device allows the outputs to be tied together. In this way, the $\overline{\text{Enable}}$ pin, with sense inverted to one of the multiplexers, can be used as the third address line on the 8-to-1 multiplexer.

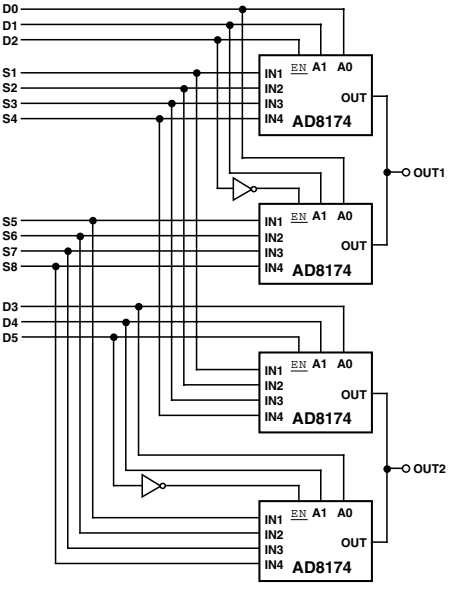

Figure 2. 8-input, 2-output crosspoint switch.

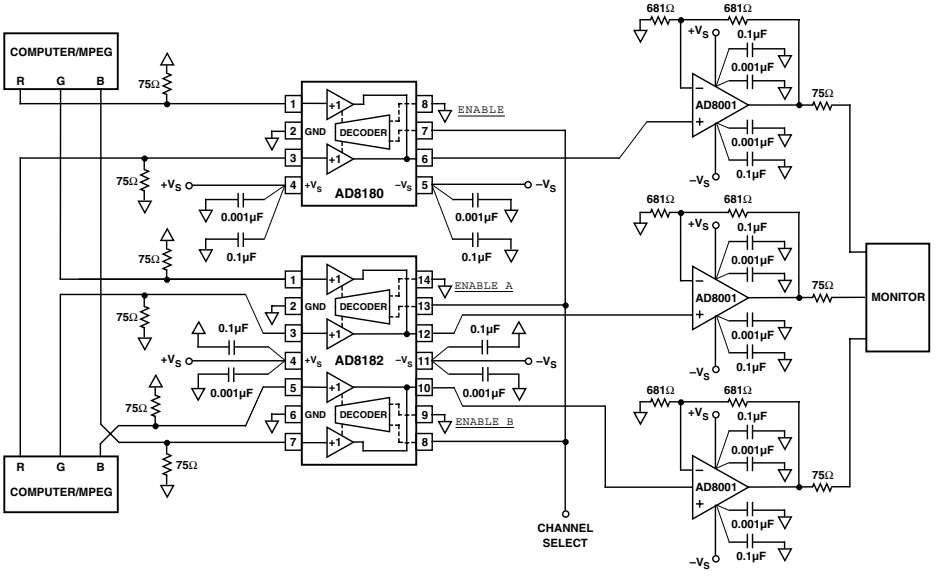

Figure 3. Switching two color video channels.

Connecting all eight input lines to both 8-to-1 multiplexers results in an 8 × 2 crosspoint switch. Any one of eight inputs can be switched to either of two outputs. The number of multiplexers that can be paralleled is limited only by the drive capability of the input signal sources. An input impedance of 2 MΩ and an input capacitance of 2 pF help to ameliorate this limitation. In applications where higher bandwidth is necessary, the AD8182 could be used to implement the same crosspoint function.

Multiplexing two Video Sources: A common video application requires two RGB sources to be multiplexed together before the selected signal is applied to a monitor (e.g., a PC's normal output and a specialized source, such as MPEG video). Figure 3 shows how such a circuit could be realized using the AD8180 and AD8182.

Because all three multiplexers are permanently active, the $\overline{\text{ENABLE}}$ pins are tied permanently low. The three SELECT pins are tied together and this signal is used to select the source. In order to drive a 75-Ω back-terminated load (R_L = 150 Ω) and provide an overall gain of unity, the multiplexer outputs are buffered using AD8001 current-feedback op amps configured for gain of 2.

Picture-in-Picture or Pixel Switching: Many high-end display systems require simultaneous display of two video pictures on one screen. Video conferencing is one such example. The remote site might be displayed as the main picture with a picture of the local site "inset" for monitoring purposes. The circuit of Figure 3 could be used to implement this "picture-in-picture" application.

Implementing a picture-in-picture algorithm is difficult. Both sources are being displayed simultaneously (i.e., during the same frame) and both sources are in real time. Figure 4 shows the raster-scanning common to all monitors. During each horizontal scan that includes the inset, the source must be switched twice (i.e., from main to inset and from inset to main). To avoid screen artifacts, switching must be clean and fast. The AD8180, used in the above application, switches and settles to 0.1% in 10 ns. Root-square-summed with the 10-ns settling time of the AD8001, the overall settling time is 14 ns. This yields a sharp, artifact-free border between the inset and the main picture.

The video source selector of Figure 3 could also be implemented with three AD8170 buffered multiplexers. Since this device has high output drive current and is capable of delivering ±3.8 V into a 150-Ω load, it doesn't require an external high current buffer op amp. In addition, the inverting input of the output buffer is pinned out so that a closed loop gain of 2 can be set.

In Figure 5, the video signals from two current output RAM-DACs are multiplexed using the AD8170. The selected signal drives a monitor. RAM-DACs typically deliver a full scale current of 26.67 mA. A doubly terminated 75-Ω line presents an effective resistance of 37.5 Ω to the DAC and converts the current into a full-scale voltage of 1 V (100 IRE or video white level) at the input to the multiplexer. Doubly terminating is good practice, minimizing

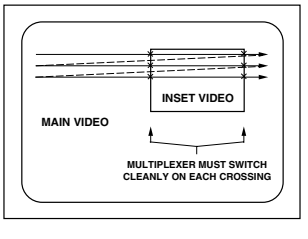

Figure 4. The key to clean picture-in-picture switching.

reflections, because the load and source impedances are both equal to the characteristic impedance of the line. Because the RAM-DAC has a relatively high output impedance, the source resistance is close to 75 Ω.

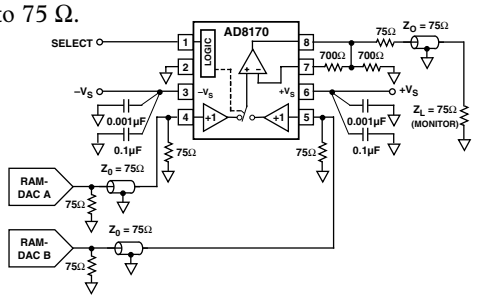

Figure 5. Complete switching for two video sources.

The output of the multiplexer must drive a back-terminated line. In order not to lose signal level, it is necessary to double the signal amplitude before application to the line. This can be conveniently done by setting the gain of the multiplexer's output op amp to +2.

Color Image Scanner: Charge-coupled devices (CCDs) find widespread use in scanner applications. A monochrome CCD delivers a serial stream of voltage levels; each level is proportional to the light shining on a single cell of the CCD. For the color image scanner shown in Figure 6, there are three output streams, representing red, green and blue. Interlaced with the stream of voltage levels is a voltage representing the reset level. A correlated double sampler (CDS) subtracts these two voltages from each other.

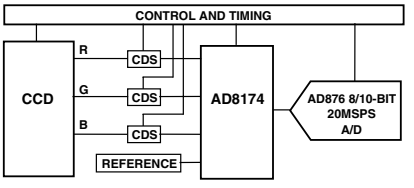

Figure 6. Color image scanning.

The next step in the data acquisition process is to digitize the three signal streams. Assuming that the ADC chosen has a fast-enough sample rate, multiplexing the three streams into a single ADC is more economic than using three ADCs. Here, the AD8174 multiplexes the red, green and blue channels into the AD876, an 8- or 10-bit 20-MSPS ADC. Because of its wide bandwidth, the AD8174 can drive the AD876's switched-capacitor input stage without additional buffering. In addition to the bandwidth, it is necessary to consider the settling time of the multiplexer. The ADC's 20-MHz sample rate corresponds to a sampling period of 50 ns. Typically, one phase of the sampling clock is used for conversion, with all levels held steady; the other phase is used for switching and settling to the next channel. For a 50% duty cycle, the signal chain must settle within 25 ns. The 18-ns mux settling time to 0.1% easily satisfies this criterion.

The fourth (spare) channel of the AD8174 is used to occasionally measure a reference voltage. Muxing a reference voltage offers the advantage that any temperature drift effects caused by the multiplexer will equally impact the reference voltage and the CCD signals. If the fourth channel is unused, it is good design practice to tie it permanently to ground.

The AD81xx multiplexer family was designed by Kimo Tam, in Wilmington, MA, and JoAnn Close, in Santa Clara, CA. A

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