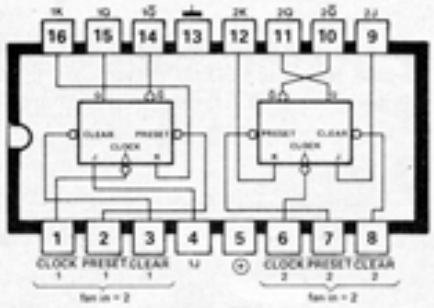
Digi-Course II

(Chapter - 4)

The internal working of the logic gates inside a Flipflop is quite complex, as we have seen in the last chapter. However, there is nothing to worry about, because once all this complex circuitry is put inside an IC, we are concerned with only the external connections. These external connections, and the logical behaviour of the Flipflop is all that we need to know, when we are using the Flipflop.

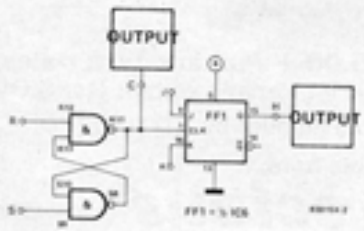
We have two sockets provided on our Digilex board for the Flipflop ICs 74LS76. These are marked IC 6 and IC7. These ICs are quite inexpensive and you can obtain them from any good electronic components hop. Each of these ICs contains two Flipflops and thus we have four universal Flipflops available for experiments.

1



For studying the properties of these Flipflops we can connect the circuit shown in figure 2. A Flipflop made of two NAND gates is used at the input to the clock (CLK) pin of the Flipflop FF1 (half of IC 6). The NAND Flipflop is used for obtaining noise free clock pulses. These pulses are indicated by the output indicator LED C. Terminals S and R are alternately connected to the ground line to generate the clock pulses.

2



The supply pins of IC 6 and IC 7 are not connected to ⊕ and ⊖ on the Digilex board. They need external connection to these supply lines. Output indicator H is connected to the pin Q of the JK Flipflop from IC 6 to show the state of the JK Flipflop. Pins J and K are used to select the J/K combination at the input of FF1.

When Pin R is momentarily connected to Ground line it gives a 0/1 combination at the input R/S of the NAND Flipflop and sets that Flipflop. This is indicated by the glowing LED indicator C. This high level appears at the clock input of FF1. Now you can connect the pins J and K to get either a 0/1 or a 1/0 combination. During this, the Flipflop FF1 is unaffected because it has a '1' on its clock input. After setting the J/K combination to 0/1 or 1/0, touch the S terminal to the Ground line. This resets the NAND Flipflop and its output becomes '0', (observe the LED C). This negative going edge at the clock input triggers the Flipflo FF1 and it latches the 0/1 or 1/0 combination which was present on the J/K inputs at that moment.

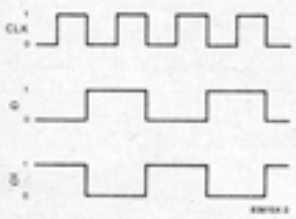
In short, we can describe the above operation as follows :

The Flipflop FF1 latches the input combination J/K into the output Q/$\overline{Q}$ on the negative going edge at the clock input.

We have just seen the effect of setting up J/K either as 0/1 or 1/0. Now let us find out what happens when J/K is 0/0 or 1/1. For this, first reset the NAND Flipflop. Then set the J/K inputs as 0/0 and clear the Flipflop FF1 by connecting the CLEAR pin to ground momentarily. This gives a 0/1 at Q/$\overline{Q}$ output. If the NAND Flipflp is now set and reset using the terminals R & S, it will produce a clock pulse at the clock input of FF1. Note that the Flipflop FF1 remains unaffected and retains its state.

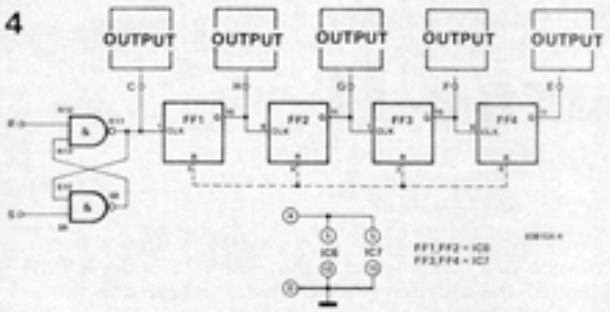
Repeat the same experiment with J/K = 1/1. This time, the Flipflop FF1 changes its state on every negative going edge at its clock input. Figure 3 shows the timing diagram of levels at the clock input and the outputs Q and $\overline{Q}$ of the Filpflop FF1 (Figure 3)

3



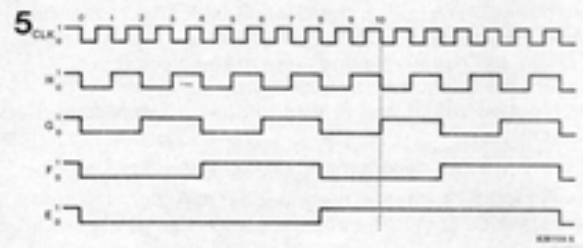
If you observe the relation between the pulses available at the outputs Q and $\overline{Q}$ and the input clock pulses, a very interesting point can be noted. The input pulses are exactly halved in the output, or in other words, we have just covered a circuit which is a 2:1 divider. It is quite obvious that if we feed the output of the first Flipflop to the clock input of another Flipflop and keep its inputs J/K as 1/1 again, we will have a 4:1 divider. Using all the four Flipfolps available to us we can generate a divider chain with 2:1, 4:1, 8:1, and 16:1 divided outputs. This arrangement is shown in figure 4. Note that all the four CLEAR inputs are connected together. This can be used to clear all four Flipflops before we start giving the input clock.

4



The timing diagram for this circuit is given below, in figure 5.

5



As we have a chain of dividers which divide the incoming pulses by two at each stage, the ratios we obtain are all binary values. Though this is quite natural in digital technology, it becomes a bit inconvenient in actual practice when we work with the decimal system. A decimal divider would be of much more value than a binary divider when we are working with the decimal system. This is possible if we take the help of the CLEAR inputs we have connected together.

6

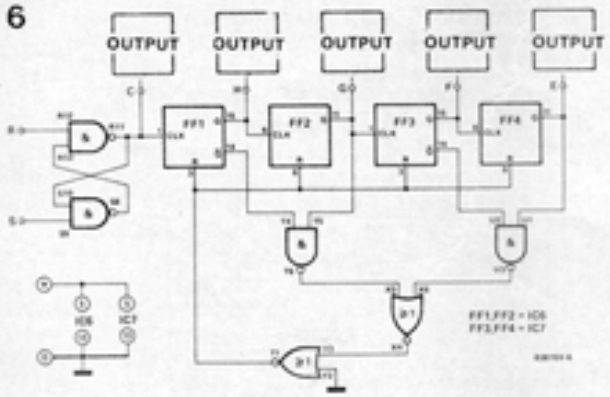
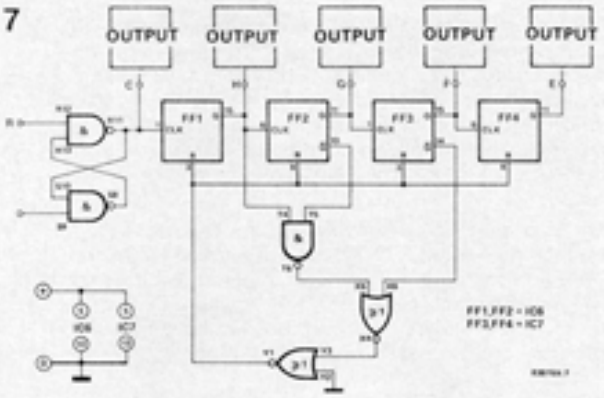


Figure 6 given above, shows a modified circuit. This has a few additional NAND and NOR gates to detect when the tenth pulse comes at the input. This moment is used to clear all four Flipflops simultaneously, so that the counting starts all over again. The LED indicator now glows once for every ten pulses at the clock input of FF1.

The additional circuit detects the condition when FF1 and FF3 are reset and FF2 and Ff4 are set. At this point, the output of the NOR gate (at Y1) becomes 'O' and clears all four Flipflops.

This arrangement has one disadvantage, which can be clearly seen from figure 5. The LED 'E' glows during 9th and 10th pulses and remains off during the first eight pulses. This defect called non symmetrical duty cycle can be rectified by modifying the circuit again as shown in figure 7.

7



Here the chain is rearranged into a 5:1 divider followed by a 2:1 divider. Now the LED 'E' remains off for five input pulses. This gives us a 10:1 divider with symmetrical duty cycle.