

CREATES CHARACTERISTIC CURVES FOR MOST SEMICONDUCTORS

BY JOHN KEITH

SEMICONDUCTOR characteristic curve tracers have been used very little by experimenters and hobbyists because many people are just not familiar with their operation. Then too, commercial units are expensive. However, a curve tracer is almost indispensable when you need to know the characteristics of the semiconductors you have on hand, especially when you are looking for a pair of matched devices for a particular application.

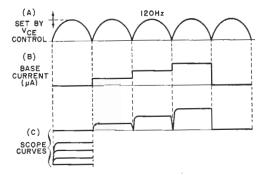
A curve tracer automatically displays the voltage-current parameters of a semiconductor device by varying one parameter while measuring another. Although this can be done manually, it is a slow, tedious job requiring many individual plots. An automatic tracer, used in conjunction with an oscilloscope, can display a family of curves in a matter of seconds. For example, the collector current curves of a transistor are created by applying the selected collector-toemitter voltage through a load resistor and varying the base current. A voltmeter connected across the collector resistor will show a variation in indicated voltage as the base bias is varied. Obviously, a selection of different values of applied base bias currents will be needed to plot a "family" of curves such as those seen in transistor manuals.

The low-cost automatic curve tracer described here is straightforward in design, easy to use, and makes an excellent addition to any workbench.

Details of Circuit Design. Timing in the curve tracer circuit is set by the frequency of the ac power input. After it is rectified, the input is a 120-Hz half sine wave with a maximum value of about 20 volts as shown in Fig. 1A. This voltage is used as the collector-emitter supply $(V_{\rm CE})$ for the transistor being tested, with the upper limit determined by a potentiometer. The $V_{\rm CE}$ supply is also used for the horizontal sweep on the external scope while the collector-emitter voltage drop (across a resistor) is applied to the scope's vertical sweep.

During the time of one 120-Hz sweep, the base bias current to the transistor under test is held at a selected constant value by a built-in "staircase" generator that changes

Fig. 1. Waveform at (A) is basic timing voltage. Transistor base current is at (B); while (C) shows how family of characteristic curves is generated.



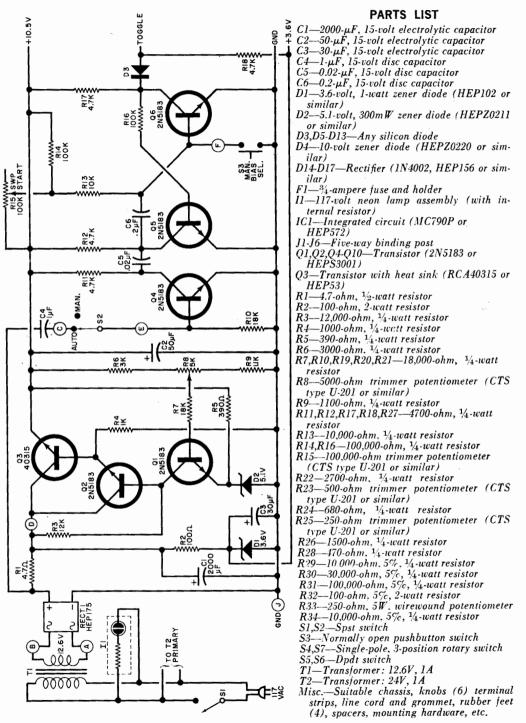


Fig. 2. Power supply and delay circuit of tracer. Regulated supply insures stable operation. The sweep start control is adjusted to remove any curve instability.

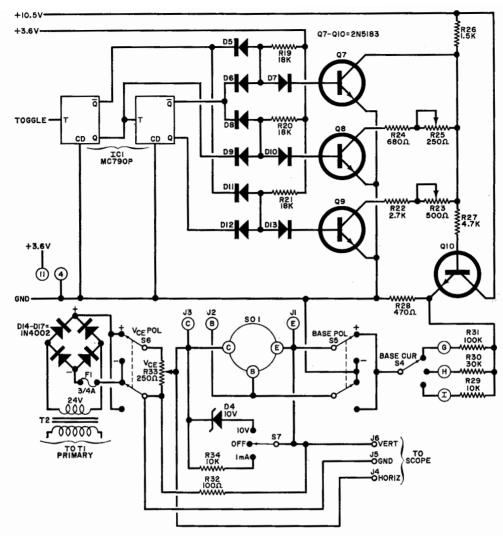


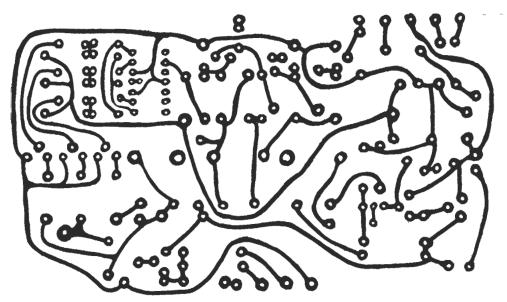
Fig. 3. Staircase generator uses divide-by-four logic circuit in association with diode gating to produce the four bias levels needed to create family of curves.

the bias current during each sweep interval to display a family of four curves. The staircase generator is synchronized to the power line frequency as shown in Fig. 1B. Figure 1C shows the scope curves for each value of base bias, and the final composite family of curves.

As shown in Figs. 2 and 3, a delay circuit consisting of Q4, Q5 and Q6 provides a variable delay to insure that the staircase switches at exactly the same time as the $V_{\rm CE}$ trace starts. This prevents "clutter" in the display.

Integrated circuit *IC1* provides a binary four count which is applied to *Q7*, *Q8*, and *Q9* through a diode gating network to produce the staircase bias levels. These are summed in *Q10* whose emitter is always at one of four voltage states: 0, 3, 6, or 9 volts. These voltages are determined by the divider made up of *R22* through *R26*; and they are preset by *R8*, *R23*, and *R25*.

The voltage staircase is coupled through one of three series bias resistors—R29, R30, or R31, selected by S4. This provides bias current values of 30, 60, and 90 microam-



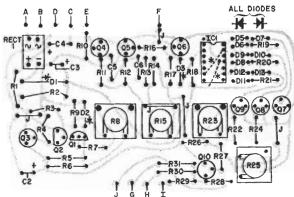


Fig. 4. Actual size foil pattern for circuit board is shown above with component layout at left. Circuit can be assembled on a standard perf board if preferred.

*USE INSULATED WIRE JUMPERS ON FOIL SIDE PIN 6 TO PIN 13; PIN II TO +3.6V

peres; 100, 200, and 300 microamperes; and 300, 600, and 900 microamperes. Each has an automatic zero voltage preceding it.

To add versatility, the polarities of V_{CE} and the base bias are independently selected by S6 and S5, respectively. This permits the analysis of both junction and insulated gate FET's, as well as conventional npn and pnp transistors.

Construction. The curve tracer can be built on a perf board or a printed circuit board (Fig. 4). The board and other components can be mounted as shown in the photograph of the prototype. There is nothing critical about the layout, except that the horizontal and vertical scope termination wires should be kept away from other leads.

Calibration. With the circuit complete and power turned on, check that pin 11 of *IC1* is at 3.6 volts dc. Connect the dc voltmeter to the emitter of Q3 (ground to minus side of *RECT1*), and adjust trimmer R8 for 10.5 volts.

To check the staircase generator, connect an oscilloscope to the emitter of Q10, making sure that S2 is in the AUTO position. When the existence of the staircase wave has been confirmed, remove the scope and place S2 in the MANUAL position. Reconnect the dc voltmeter (10-volt scale) to the emitter of Q10. Operate pushbutton S3 until the voltmeter indicates approximately 9 volts. (There should be four discrete voltage levels indicated as S3 is operated.) With the voltmeter indicating approximately 9 volts,

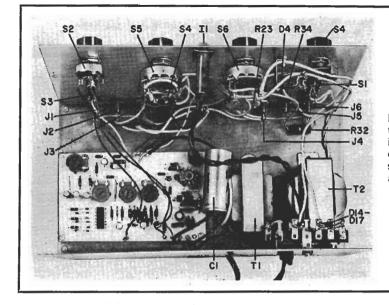


Photo of author's prototype. Note how C1 is not mounted on circuit board. Power supply components are mounted at right.

adjust R8 for exactly 9 volts. Operating S3 once should cause the voltage to drop to zero, and operating S3 once more should bring the needle up near the 3-volt mark. Adjust R25 to obtain exactly 3 volts. The next operation of S3 should produce a 6-volt indication which is set by R23. The zero is automatic. Retest S3 to indicate 0, 3, 6, and 9 volts at the emitter of Q10. When S2 is placed in the AUTOMATIC position, the voltage will be an average 4.5 volts.

For most purposes, the base currents developed by these voltages can be assumed to be correct. However, it is actually one of these voltages minus the base-emitter drop of the transistor under test. For accurate calculations (if needed), the exact base currents can be found from the staircase voltage minus V_{BE} divided by $R23,\ R30,\ \text{or}\ R31.$

Operation. Connect the vertical, ground, and horizontal outputs to the proper terminals on the oscilloscope and set the scope for external horizontal input. To calibrate the scope graticule, place the CAL switch (S7) to the 10V position, set $V_{\rm CE}$ control (R33) to minimum, and place $V_{\rm CE}$ polarity switch on +. Rotate R33 until the horizontal scope trace curves up. At this point, $V_{\rm CE}$ equals 10 volts (determined by diode D4). Adjustment of the scope horizontal gain enables calibration in volts per inch. Setting S7 to the 1-mA position and adjusting the scope vertical control permits calibration in milliamperes per inch.

Insert a known good transistor in socket SOI and set polarity switch S6 accordingly (+ for npn; - for pnp). Place switch S2 on auto and select the desired base currents with S4. A family of four curves will be displayed on the scope. If you are using an ac-coupled scope, the curves will center about the zero axis; however, with a dc scope, the display will be more stable. Adjust RI5 for a stable display.



I really don't think this is the way we should be deciding which of our designs is best for the project.