MEASURE RMS WITH LESS RIPPLE IN LESS TIME

Follow an RMS Converter with a Two-Pole Filter; Design Guides Simplify Component Choice

by Lew Counts

The output of rms-to-dc converters, such as Analog Devices models 440 and 441*, consists of a dc level and an undesired ac "ripple" voltage. The ripple amplitude is inversely proportional to the product of the input-signal frequency and the filter time constant, viz.,

$$\rho \approx \frac{16}{f\tau}, \qquad f > 1/\tau \qquad (1)$$

for sine-wave input, where

- ρ = peak-to-peak ripple voltage as a % of dc output
- τ = 50(ms/μF)C_1 for 440 or 441
- C_1 = 0.2μF + C_{EXT}μF (C_{EXT} an external capacitor)
- f = Input frequency, in Hz

The ripple introduces a small dc error into the rms computation. However, the ripple itself is the limiting uncertainty factor in measuring the rms of low-frequency signals, since the associated dc error is less than 0.1% of reading for values of ρ up to 10%.

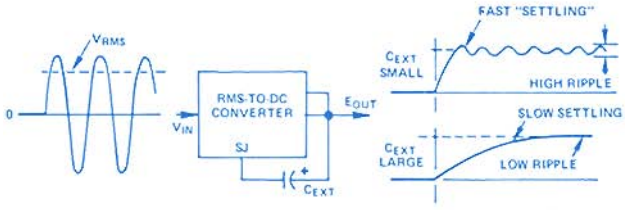

Figure 1. The dilemma — settling time and low-frequency ripple are inversely related for a given choice of C_{EXT}.

Reducing the ripple within the rms converter by adding external capacitance in parallel with the internal filtering capacitor poses a dilemma, illustrated in Figure 1. If the averaging time-constant, τ, is increased, the ripple is reduced; but the settling time to <1% of a step change of input rms is increased in direct proportion to τ,

$$t_{si} \text{ (increasing rms input)} = 2\tau \qquad (2)$$

$$t_{sd} \text{ (decreasing rms input)} = 4.6\tau \qquad (3)$$

The circuit designer can resolve the dilemma by using an external post-filter, like that shown in Figure 2. Here, the two-pole, low-pass filter greatly attenuates the ripple, with only a 40% increase in settling time, for a fixed τ. Or, for the same amount of ripple, the settling time can be greatly decreased. The filter time-constants chosen for the example of Figure 2 provide a critically-damped response to step changes in the input rms level.

Figure 3 graphically compares the ripple for Figures 1 and 2, in the case where C_{EXT} for both is 1μF. Percent ripple, ρ, is plotted as a function of frequency. Note the dramatic reduction of ripple for Figure 2 — the frequencies at which 0.1% and 1% ripple occur are reduced by factors of about 80 and 20, respectively! Figure 3 also shows the ripple-induced dc error in this case, as a function of input frequency; it is negligible, compared to the ripple, in both circuits.

*Use the reply card to request information on models 440 & 441.

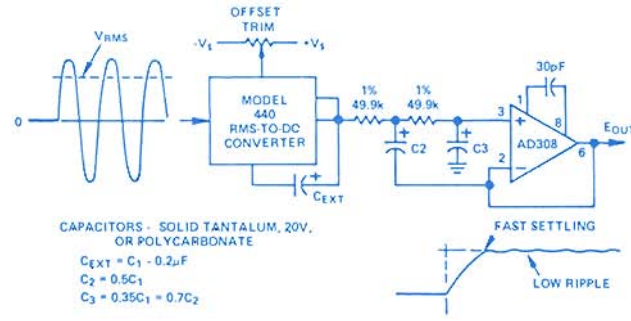

Figure 2. Using an external 2-pole filter to reduce ripple and response time. The text shows how to determine the capacitance, C_1.

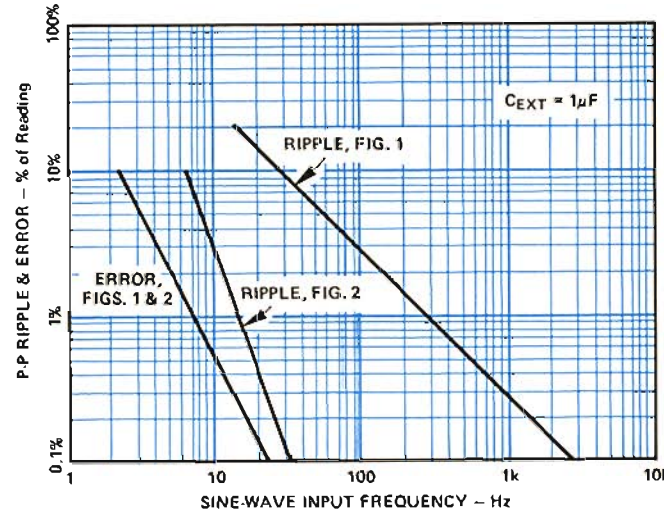

Figure 3. Ripple and error of the 440 and 441 rms-to-dc converters for C_{EXT} = 1.0μF in Figures 1 and 2.

DESIGNING FOR LOW RIPPLE

Figures 4 and 5 make it easy to determine the capacitance values and settling time to <1%, for a desired percentage ripple and a given lower input-frequency, f_L. These curves can be applied directly to designs for symmetrical input signals with crest factors less then 2, such as pure or distorted sine waves, triangular waves, or square waves. The same circuit is also very effective with higher-crest-factor signals (C.F. from 2 to 10), such as pulse trains, if the capacitance values are increased by a factor of 8.

Here is the design procedure:

1. Determine the lowest frequency, f_L, (reciprocal of the longest period) for which the rms converter must filter to 1% or 0.1% ripple.

2. Referring to Figure 4, find the value of capacitance C_1 as the ordinate corresponding to the intersection of f_L and the 1% or 0.1% ripple lines for Figure 2. (Data for Figure 1 is also included for the sake of comparison.)

3. Referring to Figure 2, calculate the values of C_{EXT}, C_2, and C_3.

4. To find the settling time to <1%, use f_L corresponding to 1% ripple for the chosen C_1, and consult Figure 5. Find the value for settling time at the intersection of f_L and each direction of input-rms change (increasing and decreasing).

Example 1. Let f_L = 10Hz for $\rho < 1\%$ p-p ripple (% of reading). Then C_1 = 1.7μF, C_{EXT} = 1.5μF, C_2 = 0.85μF, and C_3 = 0.6μF. The settling times are t_{si} = 0.2s, t_{sd} = 0.4s. By comparison, the circuit of Figure 1 would have $C_{EXT} \cong 30\mu F$, t_{si} = 3s, t_{sd} = 7s for f_L = 10Hz!

Example 2. Let f_L = 20Hz for $\rho < 0.1\%$ p-p ripple. Then, C_1 = 1.7μF, C_{EXT} = 1.5μF, C_2 = 0.85μF, and C_3 = 0.6μF. To determine the settling time to <1%, find f_L for C_1 = 1.7μF and 1% ripple (10Hz), then use Figure 5 to find t_{si} = 0.2s, t_{sd} = 0.4s.

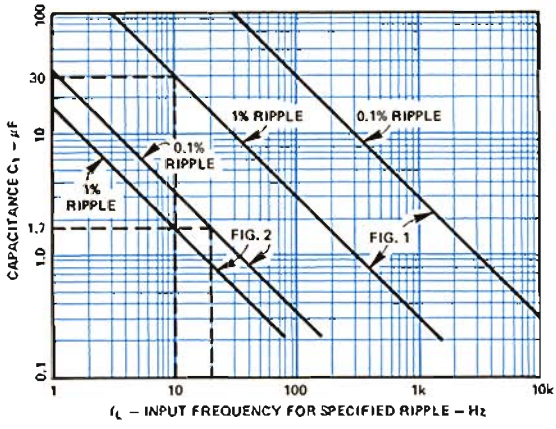

Figure 4. External capacitance (C_1) as a function of f_L, for 0.1% and 1% pk-pk ripple, for both Figure 1 and Figure 2. Dashed lines are for examples in text.

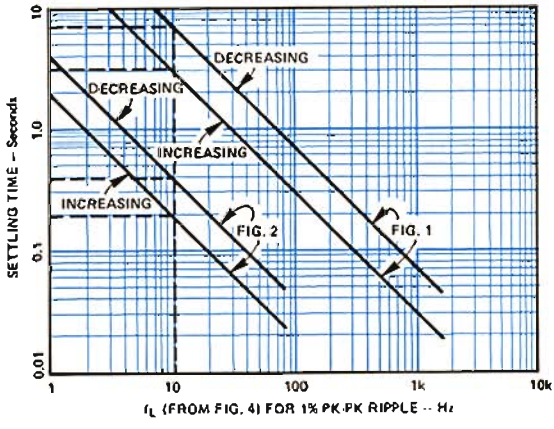

Figure 5. Settling time to 1% of step change of rms for the circuits of Figures 1 and 2, as a function of f_L.

References

Cate, T. and Handler, H. "True-rms Voltage Conversion . . .", *Electronic Design* 4, February 15, 1974.

Sheingold, D. (Editor), *Nonlinear Circuits Handbook*, 1974, Analog Devices, Inc., $5.95.