Add-on oscilloscope waveform store

2 — Control circuitry, setting-up and operation

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Digital storage techniques allow an ordinary dual-channel oscilloscope to function as a storage type. The input signal to the oscilloscope is extracted, converted to digital form, stored, converted back to the analogue form and displayed on the oscilloscope screen. A useful feature is that the waveform before the trigger pulse can be displayed. Circuitry is included to remove the "steps" in the waveform which would ordinarily be the result of a sampling process.

Control circuitry These circuits seen in Fig. 7 are operated from a 15V supply and consist of the sync counter, blank-length counter, store read/write bistable, roll read/write bistable and store-full bistable. "A" and "B" gate-level shifters, sync + and blank buffers are also part of these circuits but are not described in detail.

Sync. counter. This consists of three MC14510 decade counters, the input being derived from the e.o.c. pulse via IC_{31} in Fig. 5. The last stage (100's) is preset to the number of divisions required for pretriggering, i.e., 2(200) for two divisions pretrig. The terminal count from pin 7 of IC_{12} is used to flip over bistable flip-flops when the memory is "full". It is also used, after being delayed for one count, as a sync pulse.

Blank-length counter. One half of a 4013 dual "D" type flip flop, IC_{13} and a 4024 seven stage binary counter, IC_{14}, are used in this part of the circuit. Its function is to count the number of "divisions" after the tenth division displayed in order to reset the blank bistable. The count length is determined by the number of divisions the scope continues to sweep after the tenth division before flyback. The counter length is set by diodes and may range from 2% to 2.55 divisions. A length of 1.5 divisions is selected in the circuit diagram.

Store read/write bistable. When in the store mode, the outputs from this bistable, half a 4013, IC_{16}, opens or shuts the gates at the input of the memory. These outputs, when selected by IC_{15}, are labelled Read and Write for the Q and $\bar{Q}$ outputs respectively. When Read is high and Write is low, the gates, $IC_{6\text{-}7}$ in Fig. 2, are enabled to allow the data from the memory output to flow to the memory input, hence allowing it to recirculate. Simultaneously, Write is low and this closes the gates from the a-d convertor to the memory input. When the Write button is depressed, the outputs reverse allowing the memory to be "written". This condition is once again reversed when the sync counter terminal count goes high.

Roll read/write bistable. The function of this circuit, IC_{16}, in the roll mode, is similar to that described previously, except that it is controlled by the sync counter. The effect is to change the read/write lines once per sweep for one sample, i.e., the waveform is sampled once in a thousand. This bistable is also used to delay the sync pulse by one "sample" to allow for the analogue delay in the step eliminator. When in the roll mode the Q output inhibits the counter for one count, causing it to count 1001.

Store-full bistable. This is made up from two sections of a 4011, IC_{17}, to form a bistable. When in the store mode, its function is to inhibit the sync counter between the time that the write button is depressed and the scope's sweep being detected (A or B gate going high). It is also used to preset the sync counter at the beginning of the write cycle.

Interfacing
This unit has been designed and built around the Tektronix 465 oscilloscope. For it to operate with other instruments the inputs and outputs of the unit may need to be interfaced with those of the oscilloscope.

Feeding the output waveform into the second channel of the oscilloscope should present no problems, as the output voltage has been selected so that the waveform may be expanded and compressed and at 2V/div most instruments should be able to do this. However, if desired, the gain of IC_{28}, the output buffer, may be altered as required by altering the feedback resistor.

The sync + output also should present no problems. If the 0 to +15V edge is too high for the oscilloscope to trigger on reliably, a simple potentiometer divider may be placed across the output and the sync signal taken from the junction of the two resistors. The pull up on Tr_4 emitter should not be increased, as the increased capacitive effect between base and emitter will reflect back into the high impedance c.m.o.s. logic. This may cause trouble when in the roll mode.

The blank signal, fed into the Z mod. or axis input of the oscilloscope, has an output of 0 to +15V, the output being at +15V during the blank period. If inversion is required to give 0V during the

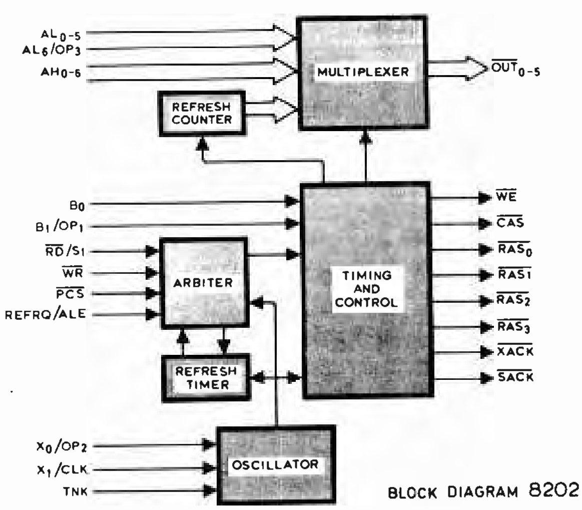


Fig. 7. Control circuit

blank period, Tr_3 base could be taken to the Q output of the blank bistable. Again, if the levels present a problem, a simple potentiometer divider could be used, as for sync +.

Due to the very large number of oscilloscope models, it is impractical to go into detail when describing the pick-off points for "A" trig, "B" trig and waveform in. All instruments of worth have trigger and blanking circuits, the former being derived from the input amplifier, via a buffer, and the latter from the sweep controlling logic.

Minimum interference is caused to the operation of the oscilloscope by taking the "waveform in" signal via an interface buffer from the "trigger buffer". This buffer can be some form of operational amplifier in the non-inverting mode (high impedance) or a simple emitter follower. The sweep waveform is usually obtained from an integrator, whose input is a step derived from the trigger circuit. Also from this circuit an unblanked signal is derived which enables the "trace" during sweep. Either of these two signals may be buffered and used for the A and B trig. Care should be taken to ensure that they are clean, and the signal does not have "chopped blanking" waveforms superimposed on it, or that the A sweep signal does not have B sweep signals (or vice versa) mixed with it. For correct blanking circuit operation within the storage unit, the "A" trig should stay high for at least 10 divisions (10 × storage unit store time/div setting) and is independent of "B" timebase which may be a positive pulse.

Some scopes have A and B gate outputs using higher output levels. In these cases R[illegible], R_{63} are changed so that Tr[illegible] base voltages are a little less than the "high" input voltage.

Practical considerations

Care should be taken when mixing analogue and digital circuits and it is recommended that the impedances around the input amplifier should be kept low to reduce adjacent track crosstalk. It was found that the wire from the position pot to the non-inverting input of the input amplifier had several microvolts of hum induced in it by the mains transformer. To stop this being superimposed on the output of this amplifier, a capacitor C, has been added from the non-inverting input to 0V. The storage capacitor, C_{28}, in the sample-and-hold section of the step eliminator is floating when the analogue switch is off, and therefore board leakage should be reduced as far as possible to prevent discharge (or charge) of this capacitor. Also the tracking to and from this capacitor should be kept as short as possible to reduce hum pick up. It has been found that slight amounts of "tilt" and hum on the integrator input have negligible effect on its output even on low displayed time/div settings.

Setting up

Only two adjustments need to be made, the first being to null the offset voltages of the d-a and output stages. This is achieved by selecting R_{14} so that with B1 only present the "waveform out" is 0V. The second adjustment is to set the gain of the input amplifier so that when a voltage proportional to ±3 divisions is fed into the unit, an output of ±6V or ±3 divisions is obtained.

To null the offset voltages first disconnect the +15V supply to the store/roll switch. This disables the read/write lines which in turn disables the read/write gates. Bits 1-8 at the memory input will now be low. Disconnect B1 to the memory input and connect it to +5V, The d-a convertor will now only see B1, and R_{14} may now be selected so that the output of the unit is as near as possible to 0V. The offset voltages of the d.a.c., step eliminator, and output buffer have now been nulled. Reconnect up the supply to the switch and B1 to the memory output.

Setting up the gain is accomplished in the following way. Connect up the inputs and outputs between the oscilloscope and unit. If a single time-base instrument is used connect the "B" trig input to 0V. Set both oscilloscope and unit to 1ms/div, the oscilloscope to "A" timebase only, and Auto trig on Ch1. Set the unit to Store mode and "B" trig, and press the Write button. The write indicator should come on and stay on. Feed into the Ch1 input of the oscilloscope a sine wave of approximately 500Hz and ±3div in amplitude (symmetrically about 0V). Ch2 should be displaying the processed waveform and the gain control RV_2, in conjunction with theposition control RV_1 may be adjusted to give a unit output of ±6V (about 0V). If the input is increased above ±3 div the output should saturate at ±6V. In the above, it is assumed that the channel whose output is used as the input to the unit is Ch1.

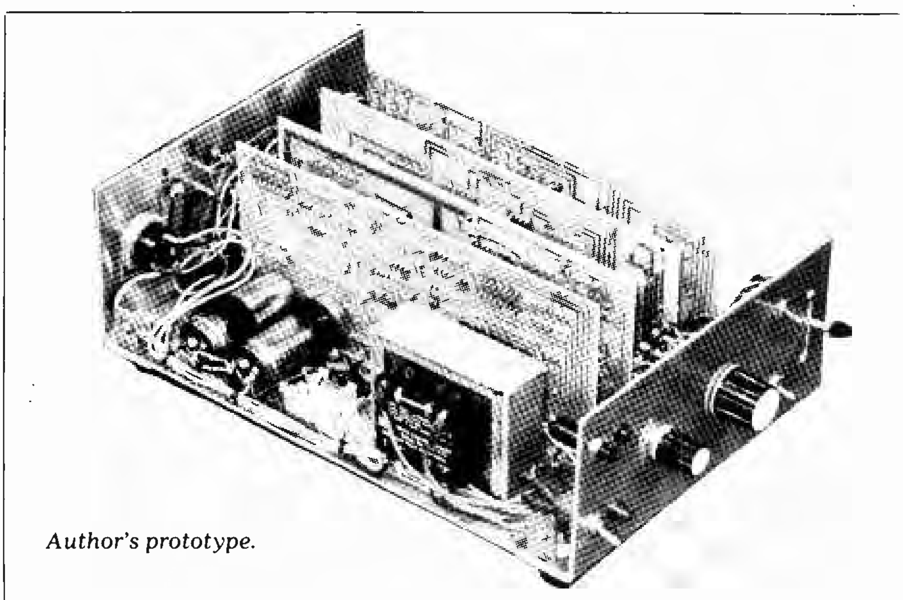
The maximum position voltage required is a little more than the maximum input voltage. If the input voltage is 50mV/div for 6 div, this gives an input voltage V_A of 300mV, and the position voltage V_B will also be around 300mV. A value for R_5 of 47kΩ satisfies this requirement.

Operation

Store mode. The oscilloscope is operated normally in either the single-sweep or normal trigger mode. So that the displayed waveform is stored as originally displayed, the time/div switches of the oscilloscope and unit should be set to the same positions. When storage is complete the oscilloscope should be triggered from the unit sync output.

The Write button is depressed before the oscilloscope triggers; this resets the store read/write bistable and causes the Write indicator to light and the data from the a-d converter to be gated into the memory. The Store Full bistable will be reset by IC_{16}, pin 12 and its $\overline{Q}$ output on pin 3 is gated with IC_{16}, pin 12 in IC_{17}, pin 4. The output of the gate is inverted by IC_{18} and the resulting high output is fed to the chip enable input of IC_{10}, inhibiting it. The circuit remains in this state, i.e. Write high, sync counter disabled and the unit waiting for the oscilloscope to be triggered.

When the oscilloscope triggers, the A gate will go high, indicating that the sweep has commenced. This high is level-shifted to +15V and IC_{17}, pin 10 goes low, setting BS_2, BS_2 Q output is fed into a pulse-forming circuit which produces a positive-going pulse of approximately 3μs duration. This pulse presets the sync counter to 200 if 2 divisions of pretrigger has been selected. The $\overline{Q}$ output of BS_2, causes IC_{17} pin 11, to go high. This, via IC_{18}, pin 3, enables the sync counter, which proceeds to count up a further 800 samples to 1000. At the count of 1000 IC_{12} terminal count goes high clocking BS_1 and setting it. "Read" will now be high and the gating is enabled to allow the data in



Author's prototype.

the memory to recirculate. Since the a-d converter was operating prior to the oscilloscope triggering, the data in the memory will consist of 200 samples, which have not been displaced by new data, and the 800 samples fed into the memory after the oscilloscope triggered. Hence, 2 divisions pretrigger and 8 posttrigger. The counter is preset in a similar manner for each of the other pretrigger positions.

Also, at the instant the terminal count goes high, BS_3, the roll read/write bistable, is reset. The $\bar{Q}$ output clocks BS_4, the blank bistable, so setting it. This has two effects: the first is to cause Blank to go high, blanking the oscilloscope's trace. The second is to inhibit Clock 1 to the memory, Clock 2 to the sync counter and Enable to the blank-length counter. These two actions result in the unit locking up, with the oscilloscope in a blanked condition, for the duration taken for the blank-length counter to time out. When the desired count (selected by diodes) is reached BS_4 is reset, re-enabling the sync counter and memory. During the blank period the memory presents the first sample to be displayed at its output. This is done so that the step eliminator can ramp the "false sample" between the end and the beginning of the stored waveform, (i.e. sample 1000 and sample 1) whilst the trace is blanked. The first clock pulse after the blank phase clocks BS_3, setting it. Sync goes high which, if the oscilloscope were set to ext. trig. would trigger the oscilloscope at the start of the stored waveform. Thus the complete store cycle is: Write button depressed-unit locks up waiting for the oscilloscope to trigger; oscilloscope triggered; counter preset; counter counts up the number of "divisions" required; terminal count reached; unit "switched" into Read; oscilloscope blanked and unit "locked up" with the first sample at the output of the memory; oscilloscope ends sweep and flyback; blank circuit times out allowing the stored waveform to be displayed. The oscilloscope trigger source is set to external so that it triggers from the unit. Triggering the unit from the "B" timebase allows delayed storage to take place.

The unit can be used to store a peak level, whilst observing the incoming waveform, by setting the oscilloscope to "A Intens by B" and setting the "B" trigger level to the peak level to be detected/stored. For example, if the normal input waveform level to the scope is ±15 divisions, the "B" timebase may be set to trigger at +1.6 div. Thus, if the input goes above +1.6 div the unit will store the waveform around this point (store peak detected).

Role mode. This extends the oscilloscope's lowest range from 0.5 s/div to 500 sec/div. The waveform appears to move from right to left, in similar manner to a paper strip recorder, with the latest level appearing on the right. When 0.5 sec/div is selected, the waveform is displayed at 0.5ms/div whilst "moving" from right to left. This provides a display that is easy to view since the whole waveform can be seen instead of a moving dot. Switching the unit to 'store' holds the waveform. The Roll mode is achieved by inhibiting the sync counter for one count, causing it to count to 1001, which means that the oscilloscope triggers on successive samples. Hence, the waveform then appears to roll round. Whilst the counter is inhibited, the read/write lines change over so that the sample before the oscilloscope triggers is "up-dated" and appears at the end of the sweep.

At the count of 999, IC_{12}, pin 7 (terminal count) is low and the unit is in the Read mode. BS_3 $\bar{Q}$ is low, the sync counter is enabled and Sync+ is high. On the next clock pulse (1000)IC_{12}, pin 7 goes high and the previous low terminal count is clocked through BS_3. This inhibits the sync counter via BS_3 $\bar{Q}$ and causes the unit to go into the Write mode. The next clock pulse (1001) again clocks the previous high terminal count state through BS_3. Sync + goes high, triggering the oscilloscope, and the sync counter is again enabled. The unit goes into Read mode for the next 999 clock pulses. In this roll mode the unit does not lock up during the blank phase, and the oscilloscope triggers on alternate sync pulses, i.e. the sync pulse follows immediately after the end of 10 divisions.

It is regretted that it is impracticable to publish the printed board design for the storage unit, but *Wireless World* can supply photocopies (made on a rather better machine than in the past) to readers who send a stamped, addressed envelope to their offices.

Circuit elements

Qty	I.cs
2	CD 4010 hex. non-inverting buffer/convertor
6	CD4011 quad 2-input Nand gates
1	CD4012 dual 4-input Nand gate
2	CD 4013 dual "D" type flip-flop
1	CD 4016 quad analogue gate/switch
3	CD 4019 quad And-Or-Select gates
1	CD 4024 7-stage binary counter
1	CD 4029 presettable binary/decade up/down counter
5	MC 14510 presettable decade up/down counter
1	MC 14559 successive-approximation register
2	MC 1408-L8 8-bit digital-to-analogue convertor
1	MC 1407 a-d control circuit
4	NE 531 high-speed differential op-amp
16	NE 2528 dual 250-bit shift register
1	LM 302 voltage follower

Transistors

1	BSX19 n-p-n
3	2N2906 p-n-p
3	BC107 n-p-n

Diodes

35	1N4148 general-purpose
1	BZY 88 C4V7 Zener
1	1.8 MHz crystal (for oscilloscopes scopes with 10 horizontal divisions)

Resistors

1	470R	½w 2%
2	560R	
1	820R	
5	1k	
1	2k	
3	2k2	
1	3k	
2	5k1	
1	9k1	
10	10k	
1	11k	
8	15k	
2	18k	
1	30k	
2	33k	
3	47k	
15	100k	
1	18M	½w 5%
1	1k pot.	
1	47k trimpot	

Capacitors

1	15p tubular ceramic	
1	20p	
2	22p	
2	39p	
4	100p	
1	120p	
3	270p	
1	470p	
1	680p	
16	100n	disc ceramic
1	470p	1% mica
1	1n	
1	2n2	
1	4n	
1	10n	
1	22n	paper, polyester, etc
1	47n	
1	100n	
1	220n	
1	470n	
1	100µ	electrolytic 10V

Switches

1	3-pole	10pos. rotary
1	1-pole	2-throw toggle
2	1-pole	2-throw toggle
1	1-pole	push button
1	1-pole	4-pos. lever

Specification

The unit gives a storage area of 6 divisions vertical and 10 divisions horizontal.

Input from oscilloscope:
+300 mV for all positive storage
−300 mV for all negative storage
± 150 mV for bipolar storage
The input levels are easily adjusted to suit the oscilloscope and the 0V position is adjusted by a control on the front panel.

Time/div. ranges:
Store mode 500, 200, 100, 50, 20, 10, 5, 2, 1, 0.5 ms/div.
Roll mode: 500, 200, 100, 50, 20, 10, 5, 2, 1, 0.5 s/div.
Thus the range is from 0.5ms/div to 500 s/div in 19 ranges.

Waveform output to oscilloscope:
± 6V (2V/div)-irrespective of input polarity; i.e. 0V appears as −6V for all positive storage,
+6V for all negative storage,
and 0V for bipolar storage.
The output levels are easily adjustable.

Sync to oscilloscope
0 to +15V edge at the start of the stored waveform. This is fed into the Ext Trig input of the oscilloscope.

Blanking to oscilloscope:
+15V level after the tenth division the length of which is selected to suit the oscilloscope.

A-Gate from oscilloscope:
+5V logic level, going high at the start of "A" timebase sweep. Level must be maintained for at least 10 divisions during display stored waveform period.

B-Gate from oscilloscope:
+5V logic level or pulse going high at the start of "B" timebase (approx 10µs min).

Acknowledgements

The author would like to acknowledge his indebtedness to Gould Advance Ltd, whose OS4 oscilloscope gave rise to the ideas of roll, pre-trigger and step-elimination, although it should perhaps be pointed out that the design of the present instrument was started three years ago – before the OS4000 was made public. Thanks are also due to Tektronix, who lent a C-5A camera for the screen photographs.