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TIME-FREQUENCY MEASURING SYSTEM DESIGN THEORY PART II AND CLOCK

This is the second of a three-part series describing the design theory of a time/frequency measuring system for a well equipped amateur radio station and workshop. The heart of the time base is the master oscillator. For the expected accuracy and stability, a crystal oscillator, with the crystal in a temperature-controlled oven, is necessary and sufficient. A crystal oscillator not using an oven might be made to hold to within one part in 10^6 with careful temperature compensation and a bit of experimentation, but remember that that is the very worst stability we can use. A simple crystal oven, and reasonable care in construction of the oscillator, can achieve stabilities better than one in 10^7, which is consistent with our goals. More exotic techniques, with double ovens (one around the whole oscillator), can yield crystal oscillators with stabilities measured in parts in 10^9, but these are beyond the needs of most amateurs.

Any oscillator consists of an amplifying element and a feedback element, as shown in Fig. 2. The amplifying element must have a stable gain great enough to provide a usable output power without loading the feedback element, and the feedback element must put just enough of the amplifier's output back to the input to sustain that output, but only at the desired operating frequency. The multiple-amplifier integrated circuit packages provide the most convenient way to get the stable forward gain needed. The RTL and DTL circuits are intended for digital applications, but when biased into their linear operating regions make good high-gain linear amplifiers. The more popular TTL circuits tend to be unstable as amplifiers but work ok as oscillators. I used a quad NOR gate in this application because I happened to have one, but other gates might work.

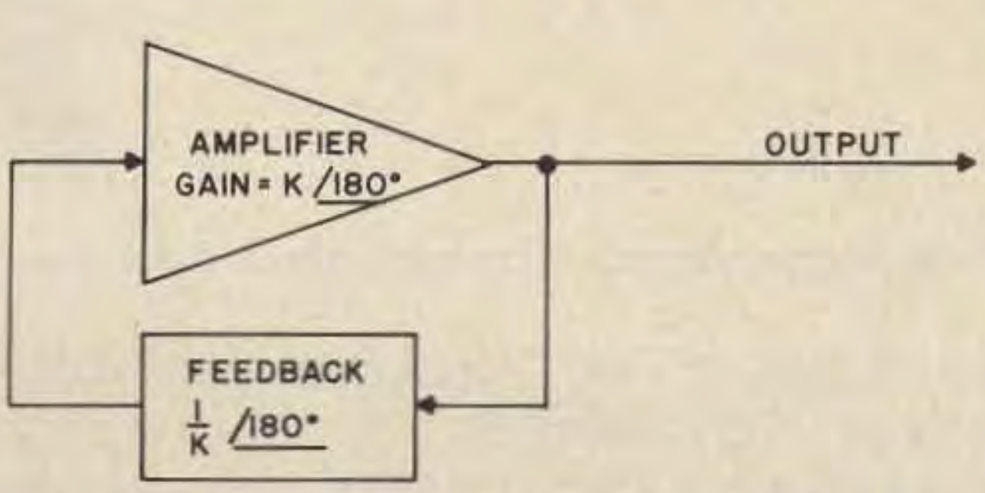

Fig. 2. Oscillator block diagram.

The feedback element is, of course, the crystal, operating as a parallel resonant filter. I chose an operating frequency of 1 MHz, because I happened to have a crystal for that, but a crystal on any frequency between 1 and 10 MHz designed for a stability of one part in 10^6 per week over the temperature range provided in the chosen oven will be adequate. It is difficult to get crystals of the necessary stability lower in frequency than 1 MHz, and the cost is much higher below about 5 MHz. The chosen frequency should be a multiple of only the numbers 2, 5, 6, and 10 (like 4 MHz = 2 x 2 x 10^6, or 5 MHz = 5 x 10^6), otherwise the dividers will have to be specially designed.

A fine trimmer adjustment must be provided on the oscillator with a no-backlash calibrated vernier control. Because adjustments will be made to the oscillator that will not show up until a week later, the operator must be able to tell exactly how far and in what direction he is adjusting. The calibrations don't have to be in Hz, but do have to be in linear repeatable units so that if, for

example, a correction of one unit reduces the drift from 0.5 to 0.4 seconds per week, then four units of correction in the same direction should put the oscillator right on. I used a vernier control giving 100 divisions for 1/2 turn of the trimmer capacitor, and about a five-to-one speed reduction from the knob.

Divider Chain

The oscillator is tied to the clock through a divider chain, as shown in the time base/clock diagram, Fig. 3. The purpose of this chain, of course, is to divide the oscillator frequency until it has a frequency useful for the devices to be connected to it. Integrated circuits are available for dividing by 2, and multiples of 2, 5, 6, or 10. Other division ratios may be implemented, but not as conveniently. The 7490 decade divider IC chosen for my project has two independent dividers, a by-2 and a by-5. These are normally cascaded, or the signal run through both, to get divide-by-10. If it is being used as a counter, the signal must go thru the by-2 first and then the by-5 to make the numbers run in the right order, but if it is only being used as a divider, the signal may go thru the by-2 last. This has the advantage that the output signal is a symmetrical square wave, which is a little nicer for use as a clock signal.

Line Drivers

The output signals from all of the above mentioned divider IC's are zero and four volt logic levels, which may be driven directly into any of the other IC's. If these signals are to be transmitted via coaxial cable outside the unit, however, some buffering must be done. The reason for this is that the low impedance of standard coaxial cables places too heavy a load on the IC circuit. Even if they could drive the load, a four-volt swing on a 50Ω cable is an unecessarily large amount of power to use just to transmit a clock signal. To mitigate these conditions, I use 90Ω RG-62 cable for all interconnects, and extra gates for signal isolation.

Clock Speed Control

In order to set the clock to the correct time and synchronize the change of seconds with standard time, some sort of clock control must be provided. The most convenient system to use requires a full set of digit switches and parallel-load button, plus an interrupt control to stop the clock. In use, the operator sets into the digit-switches a time that is coming up, stops the clock, and loads the set time into the clock. At the instant the selected time occurs, he restarts the clock, and it is synchronized. Unfortunately, the digit-switches are bulky and expensive, so I did not use this method.

The system I used is less convenient to use, but then the clock does not need to be set very often. I provided a rotary selector switch which selects clock speeds of Off, Normal, and up to 10,000 times normal speed. This fastest speed will run the clock through its full 24-hour range in 8.6 seconds. In use, I set the clock by running it at high speed until it gets to the time I want, switch to OFF to wait until that time comes up, then switch to NORMAL speed. The switch is controlling the 10 Hz point in the divider chain, so the clock can be synchronized to within 100 milliseconds.

Clock Counters

As may be seen in the clock diagram, Fig. 3, a separate counter IC package is used for each digit of the clock, except the tens of hours. A 7490 decade counter is used for the units of seconds, units of minutes, and units of hours digits, all of which count modulo-10 (0 to 9, then back to 0). The leftover divide-by-2 parts of the 8288's are combined to make a 2-bit divide-by-4 for the tens of hours decade. This makes a basic 40-hour clock.

To make the clock recycle at 24 hours, that time is recognized by a detector gate, which then resets (clears) the clock to zero. Actually, most of the clock is already zero, so only the tens-of-hours 2, and the units-of-hours 4 need to be reset. A *nand* gate toggle buffer (simple flip-flop) is used to store the reset signal until it is itself cleared four seconds later. This storage is necessary because the reset signal is removing the signals which cause it by resetting the clock, and a race around the loop would occur without the storage. The four seconds is purely arbitrary. I used the units of seconds 4 line because it was handy; any signal that switched on between midnight

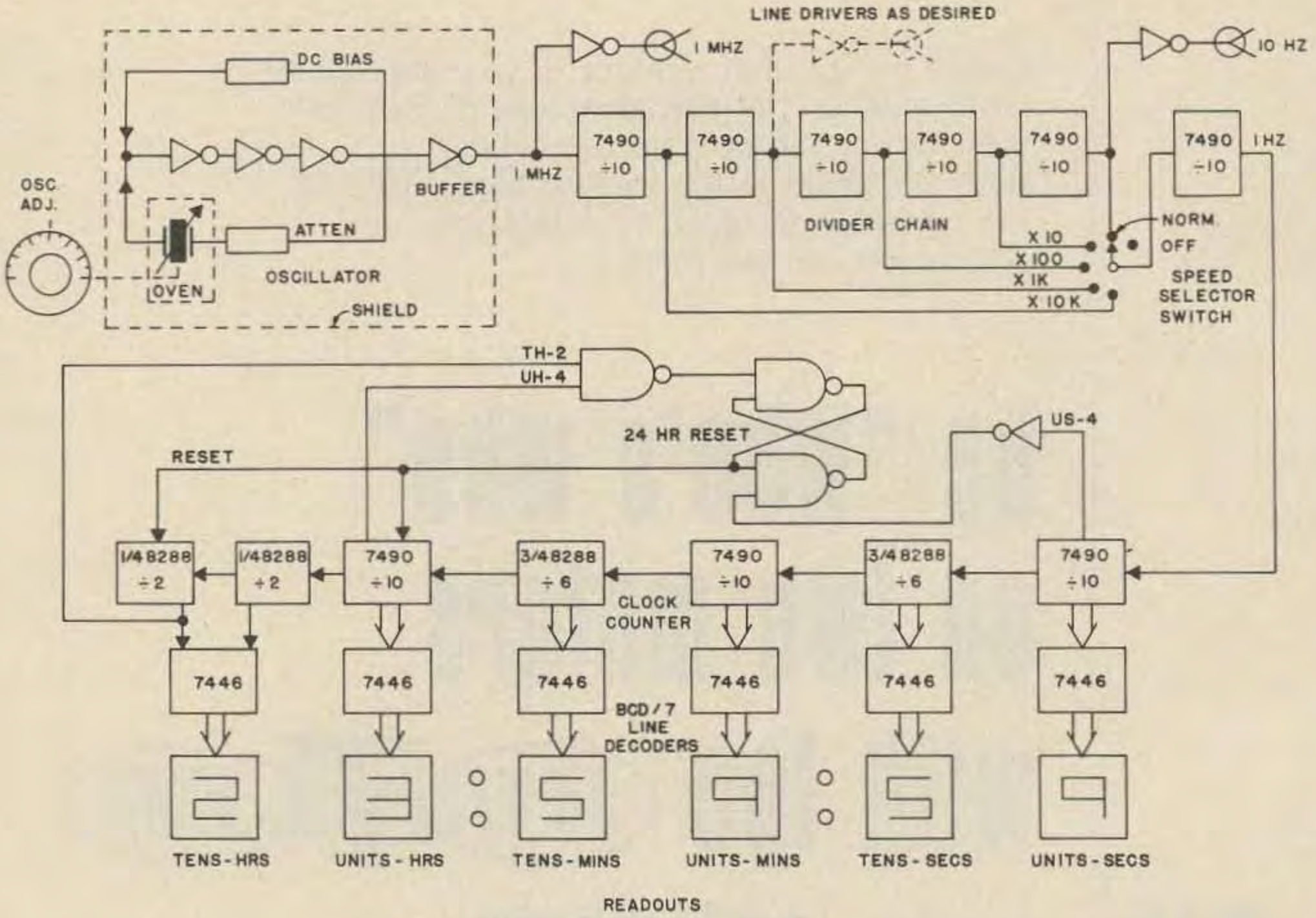

Fig. 3. Clock/time base block diagram.

and ten seconds later would have worked. The reset signal must be cleared within ten seconds because the reset for the tens of hours 2-bit is also holding down the tens of seconds digit, which shares the same 8288 IC.

Decoders and Readouts

The decoders must be chosen to drive whatever readout the builder chooses. Seven-segment readouts such as I chose are the most economical incandescent readouts, but the builder may have other kinds from surplus sources. Nixie tubes are also economical, but require a high voltage power supply.

The 7446 decoders I chose match the seven-segment readouts with 24 volt incandescent bulbs that I used. These decoders will stand 30 volts and switch 40 mA. I run the lamps with 12 volts; they are bright enough to read easily and the life of the bulbs is extended greatly. If the builder used lower voltage bulbs, he may use the 7447 decoder, which has a 15 volt rating. However, if the lamp current will exceed 40 mA per lamp, it will be necessary to use the 7448 decoder (which pulls up instead of down at the output), and a buffer transistor in the line to each lamp. This can be any cheap NPN such as a 2N5129. The connection for this is shown as an alternate on the schematic.

If the builder uses ten-line rear-projection readouts, which are sometimes available as surplus, he will need 7442 decoders. If he uses Nixie tubes, he will need 7441 decoders.

Power Supply

The circuitry used draws a substantial amount of current at 5 volts dc, plus an even larger amount for the readout lamps, which may also be 5 volts, plus power for the oven heater. All of these loads are varying; each number showing on the display uses a different number of lamps, and the various counts that appear from time to time in the counters draw different currents. A good voltage regulator can eliminate any problems arising from this, and I would not suggest that anyone consider getting by without one. IC regulators are available for a few bucks with all the features one would want (voltage regulation, current limiting, short circuit protection, etc.) from several manufacturers, including National and Fairchild.

The National LM 309K I used, for example, is in the standard diamond power transistor case, takes in 6.5 to 35 volts or wave forms with ripple between those limits, puts out 5 volts at up to 2 amp., is short-circuit-proof, and just bolts directly to any grounded heat sink. All that costs around $4, and no one can affort to design and build a regulator with that kind of thing available.

The rest of the power supply is a transformer-rectifier to supply 12 volts dc for the regulator, a lamp supply, and a shunt regulator for the standby batteries. My lamp supply is very simple, being just another set of rectifiers from the same power transformer, because I used 12V lamps. If other voltage lamps are used, a separate transformer will probably be necessary, but separate rectifiers should be used in any case, to prevent the heavy lamp current from loading the filter capacitor. The lamp power does not need to be filtered.

The standby batteries are connected in parallel to float across the unregulated 12 volt line. This simple connection would be adequate to keep the batteries charged and provide standby power for the 5 volt regulator, except that the voltage can rise high enough to overcharge the batteries. The simple shunt regulator I used limits the peak unregulated voltage to about 14 volts, which a 12 volt storage battery can stand almost indefinitely.

Batteries

The floating-battery scheme used here is appropriate for lead-acid type batteries. I use a motorcycle battery, which has the capacity to run the clock for several hours. It has the drawback of having the acid fume and spillage worry of that type of battery. A better choice would be a sealed battery of the type made by Centralab under the name GelCel. The Nicad batteries look very attractive, although high-priced, but they require a different charging scheme than I have provided here, that is, constant current instead of constant voltage.

RFI Considerations

Digital circuitry of the type used in this unit generates large amounts of wideband, high-frequency noise. The reason for this is the very thing that makes TTL logic so good: it works very fast. Whenever a gate switches, the resulting square voltage waveform has harmonics spread out well into the VHF region. For this reason, all digital devices to be used near radio equipment should be built in shielded enclosures, at the very least an all-metal cabinet, and all wires leading in or out should be shielded or filtered. Normal techniques for TVI-proofing a transmitter will serve here.

Three of the NOR gates in the LU380A package are connected in cascade to form the amplifier portion of the oscillator, as may be seen in the Time Base Schematic, Fig. 4. The input to this amplifier is pin 10, and the output is pin 2. The last gate is used as an output buffer, from pin 4 to 3. There are two feedback paths, one for dc stabilization, and one for the rf signal. R4 and R3 provide enough negative feedback bias to stabilize the amplifier in its linear region. R3 is to be adjusted to get a symmetrical square wave from pin 3. C8 bypasses the rf to ground so that only dc is fed through this path.

The crystal Y1 and capacitors C3, C4 and C7 are connected to form a 180° phase shift and voltage step-down network, as used in a Colpitts oscillator. C4 is a fine trimmer across the high-impedance side of the network to adjust the frequency, and is the Frequency Adjust Control mentioned in Part I of this series The amplifier output is attenuated by R2 and C6, then lightly coupled to the high-impedance side of the crystal network through C5 to keep the crystal voltage as low as possible. The output from the low impedance side of the crystal network is connected back to the amplifier input to complete the loop. The amplifier output is to be coupled as lightly as possible (smallest value of C5) and still maintain oscillations.

You might get by without shielding the oscillator, but I consider it a worthwhile precaution to isolate the oscillator from outside influences. I enclosed the whole oscillator in a brass strip fence, as can be seen in the photo. All the capacitors associated with the crystal network (C3, 5, 6 & 7) must be high quality stable types such as silver mica. C4 must be a good grade VHF type trimmer.

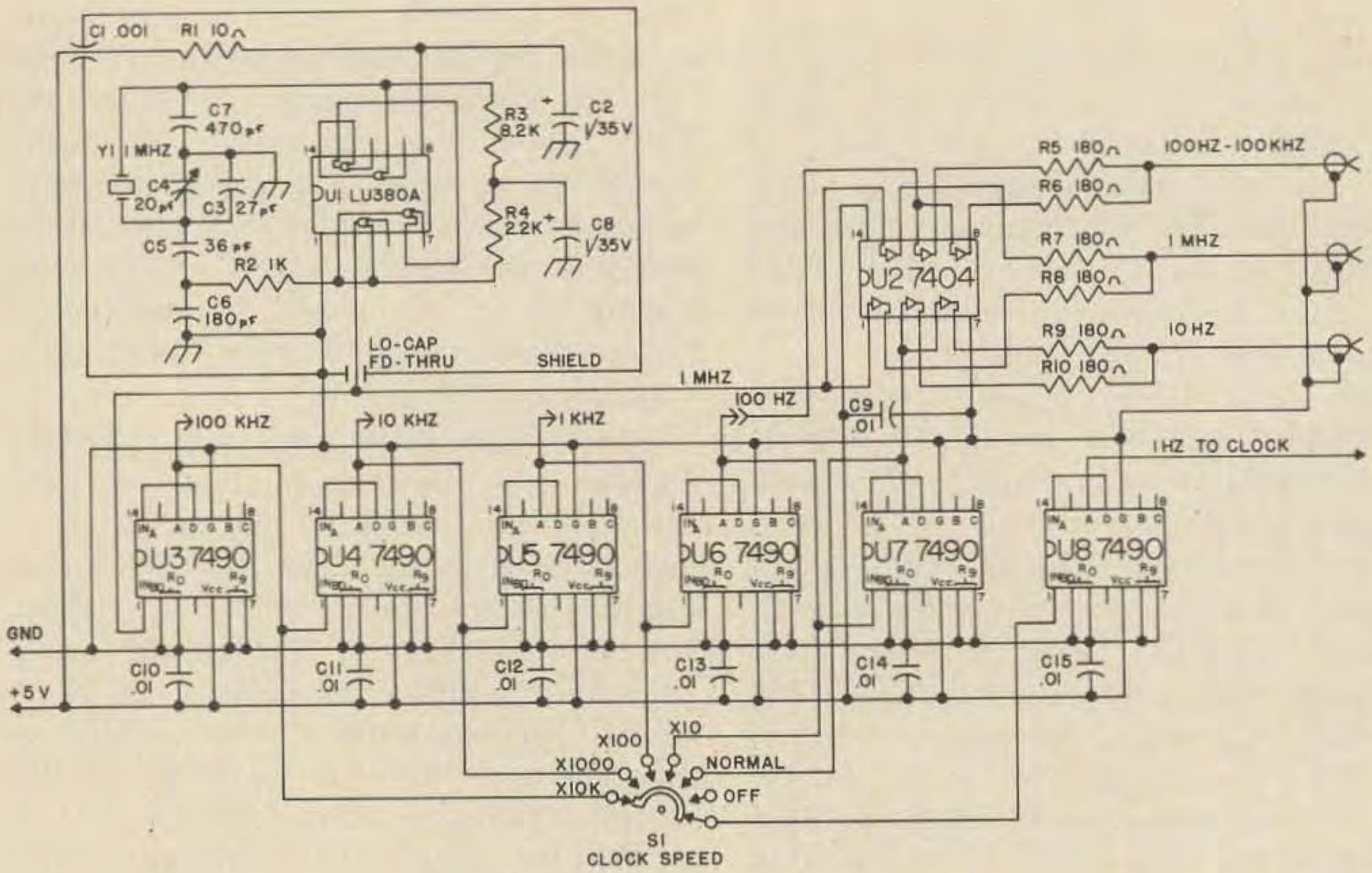

Fig. 4. Time base schematic diagram.

Divider Chain

The divider chain consists of a string of decade dividers, each reducing the operating frequency by a factor of ten. Each is connected with the divide-by-five ahead of the by-two portion to give a square wave output. The input signal enters at the divide-by-five trigger port (labeled IN_{BD}). The output of this section (labelled D) is connected to the trigger of the divide-by-two section (labelled IN_A). The output labelled A is then the square wave.

The B and C outputs are not used and are left open. The reset-to-0 and reset-to-9 inputs are not used in the divider chain and are grounded. Inputs left open will assume a logic 1 (high) state, which in this case would hold the counters in reset (0) state.

The A output of each divider goes to the IN_{BD} input of the next divider in each case, except the 10 Hz line between U7 and U8. This line goes through the Clock Speed Switch S1 in the NORMAL position. In other positions, the input to U8 is tapped from the output of dividers running at higher frequencies to speed up the clock, as explained previously.

Bypass capacitors C9–15 are required because of a characteristic of the TTL IC's used; these devices draw a large amount of current for a very short period of time while they are changing state, appearing as a current spike on the Vcc line. Due to the inductance in even a short piece of wire feeding the supply voltage to the IC, this current spike can produce bad voltage surges. The cure is simply a small capacitor directly across the supply terminals of each device. This is a small price to pay for the high performance of the TTL logic family.

Line Drivers

U2 is a hex inverter used as an isolation amplifier for driving coaxial lines. Two amplifier sections are used in parallel to drive a 90Ω coaxial line (RG-62 cable) through isolation resistors. These 180Ω resistors in parallel give an effective 90Ω output impedance and keep the load on each amplifier within its 10 mA rating. One IC provides three output lines. 10 Hz is needed for frequency counter, 1 MHz is a useful output for initial oscillator checks, and the other line may be connected to whatever frequency is desired between 100 Hz and 100 kHz. To bring out all the possible frequencies would require additional hex inverter packages.

Clock Counters

The clock counters consist of a divider IC for each digit of the clock except the tens of hours, with a 24-hour reset circuit to switch the clock back to zero every midnight, as may be seen in the Clock Schematic Diagram, Fig. 5.

The units of seconds (U14), minutes (U12), and hours (U10) counters are decade dividers connected in the standard manner for this device. That is, the input signal triggers the divide-by-2 A section first, and then the by-5 BCD section to produce the standard binary-coded-decimal (BCD) counting sequence for which the decoders are designed. Therefore, the ABC & D outputs are connected to the ABC & D inputs of the decoders respectively, The D, or last, output drives the input of the following stage.

All the reset inputs on the units digits are unused and grounded, except the reset-to-zero for the units of hours. This is connected to the reset line, as shown in Fig. 3, to clear the four in the twenty-four hours.

The tens of seconds and tens of minutes digits use the divide-by-six BCD sections of U13 and U11 IC's respectively. Because these represent the ABC bits of a modulo-six digit, the BCD outputs of these counters are connected to the ABC inputs respectively of the corresponding decoders, U19 and U17. The reset-to-zero input of U13 is connected to the reset line, all others being grounded.

The leftover divide-by-2 A sections of U13 and U11 are used to make the two-bit tens of hours digit. The U11 A section is the TH1 bit and the U13 A section is the TH2 bit. Therefore, the D output from U10 drives the A input of U11, and the A output of U11 drives the A input of U13. These two A sections are connected to the A & B inputs of the tens of hours decoder U15, representing a two-bit number to that decoder. The other decoder inputs are grounded.

The quad *nand* IC U9 is connected to implement the 24-hour reset logic, which may best be seen on Fig. 3. The number 24:00:00 is recognized by the gate at pins 8, 9 & 10 by the presence of the TH2 and UH4 bits in the high state, which then sets the *nand* toggle made up of the gates at pins 1 through 6. The toggle puts a high state on the reset line from pin 3, which resets to zero U10 and U13. The next US4 bit is inverted by the gate at pins 11–14 of U9 and then used to clear the *nand* toggle.

Decoders and Readouts

The common terminal of the readouts is connected to the lamp voltage from the

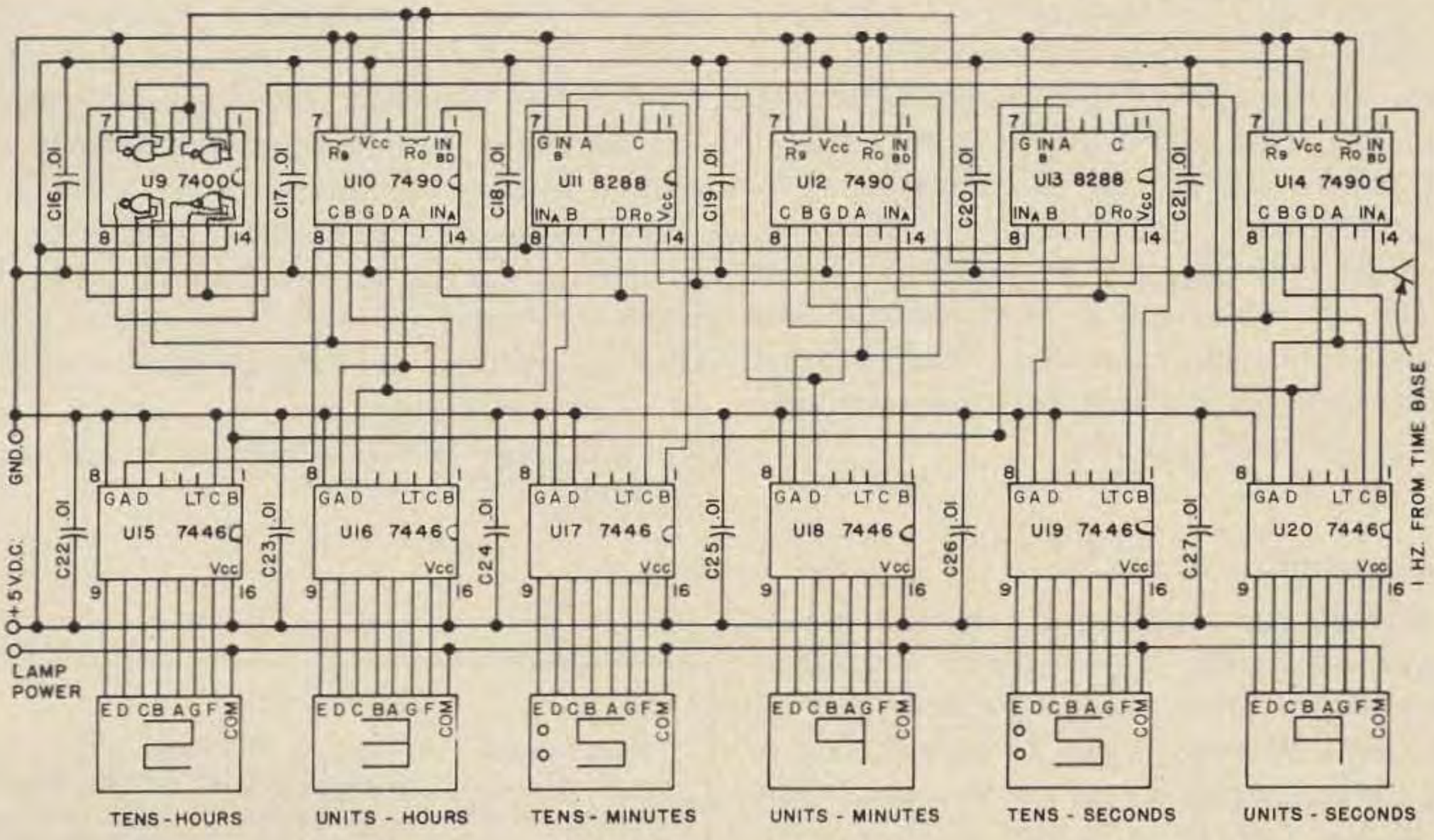

Fig. 5. Clock schematic diagram.

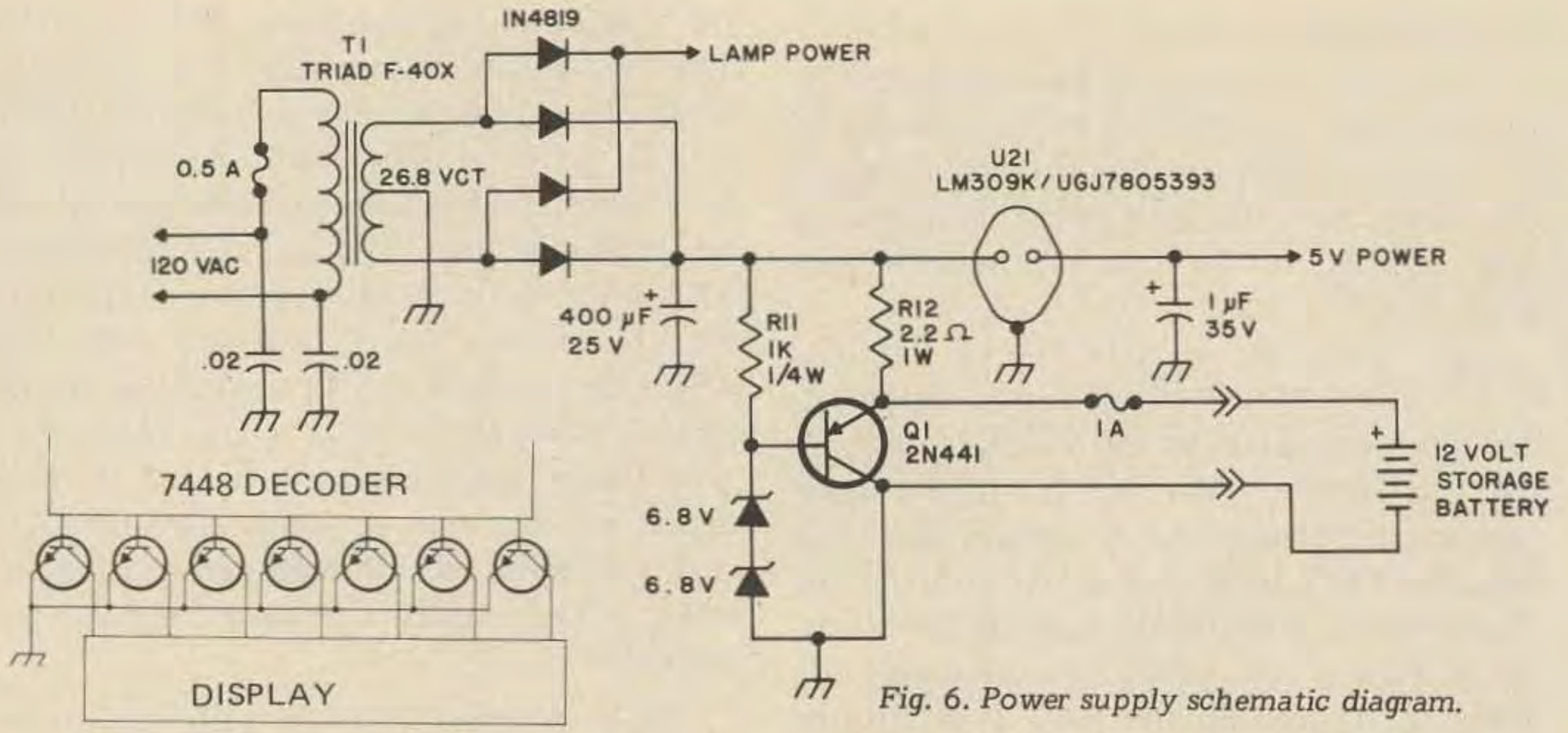

Fig. 6. Power supply schematic diagram.

power supply, and the lamp of each segment in the display lights as its line is grounded by the decoder. The decoder lights the combination of lamps making the numeral corresponding to the binary code fed to it from the counter.

The pin 4 & 5 connections to the decoder are for blanking of unused numbers and have no function in a clock. Because they are active in the low state, they may be left open to be inactive (high).

The input at pin 3 of the decoders is for lamp testing. I didn't use this, but one could tie all these pin 3's together to a bus line and ground it with a push-button to make all 8's appear in the display, thus testing all display segments. This would not be a very useful frill, but it wouldn't cost much either.

An alternate connection for lamps drawing more than 40 mA is shown in the corner of Fig. 6. This uses a 7448 decoder and seven NPN switch transistors. The 7448 has output pull-up resistors for direct connection to the transistor base.

Power Supply

The power supply for the IC's uses a transformer with center-tapped secondary, full-wave rectifiers, and capacitor filter of the simplest type, as can be seen in Fig. 6. The filter capacity shown allows several volts of ripple and is thus very easy on the rectifiers, but the regulator IC U21 changes this to as pure dc at 5 volts as one could desire. About one μF of filter capacity should be on the output of the regulator, but this can be at the load, or almost anywhere on the 5 volt bus, as it is to bypass low-frequency transients.

The lamp power is derived with a separate set of rectifiers to prevent loading the filter capacitor with the relatively heavy lamp current.

The shunt regulator I used is fairly crude and non-adjustable, but is doing its job quite adequately. The two 6.8 volt zener diodes provide a 13.6 volt reference voltage for the base of shunt regulator Q1. Whenever the emitter of this PNP transistor exceeds 0.3 volts higher than this, or about 13.9 volts, the regulator begins to shunt current to ground to hold the voltage at that level. The 2.2Ω resistor R12 is chosen to limit charging current to the battery to about 1/2 ampere when the battery is low, i.e., about 11 volts terminal voltage. R11 is not at all critical, and only provides some keep-alive current for the zener diodes when Q1 is not conducting.

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YOUR CALL

Please check your address label and make sure that it is correct. In cases where no call letters has been furnished we have had to make one up. If you find that your label has an EE3*&* on it that means we don't know your call and would appreciate having it.