PLL performs accurate phase measurements

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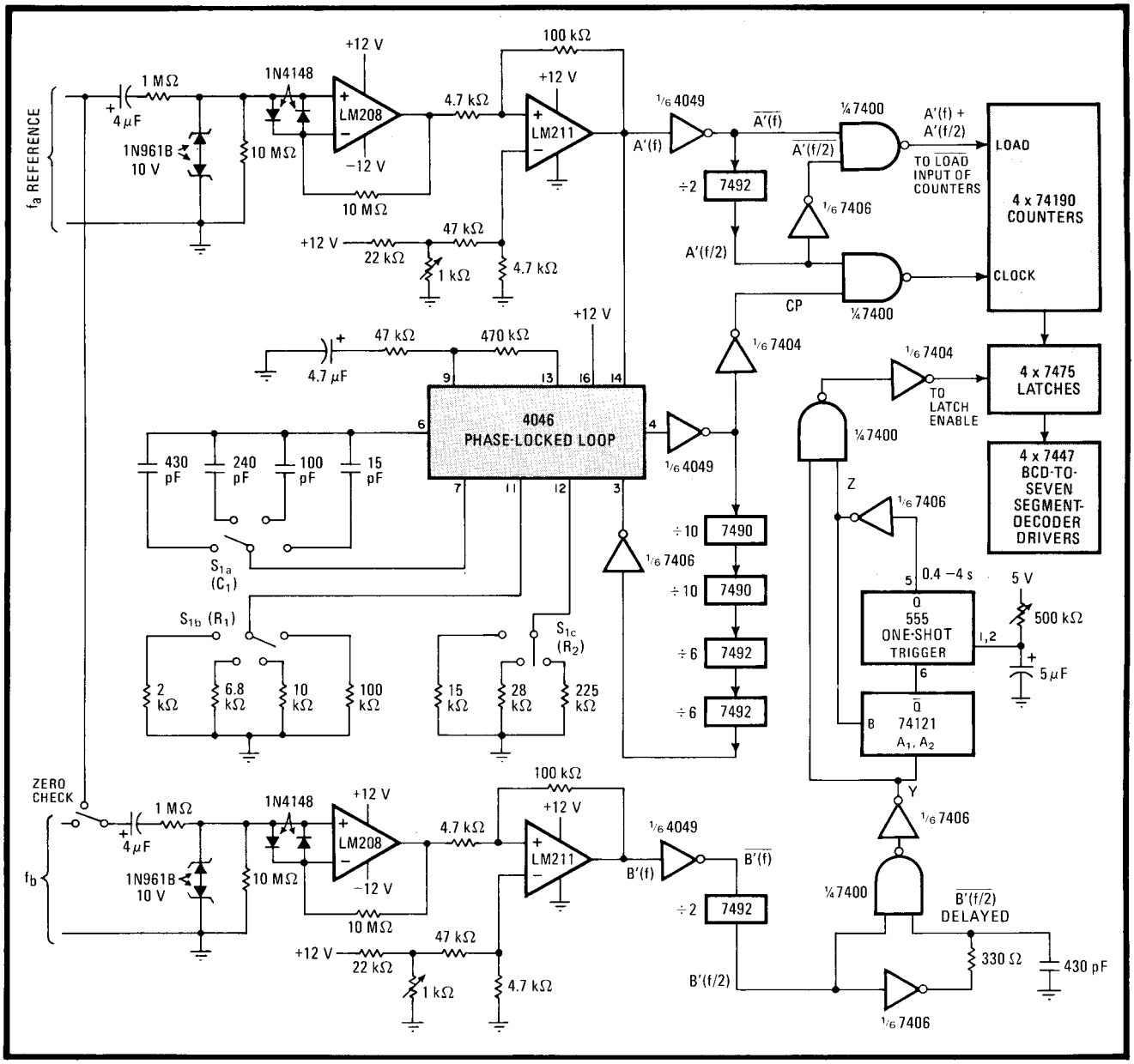
The excellent tracking ability inherent in a phase-locked loop is utilized in this meter to measure phase differences accurate to 0.1°. Although intended for use in the dc-to-1-kilohertz audio-frequency range, the upper limit of the unit can be extended by suitable selection of a high-frequency PLL and appropriate circuitry to reduce phase jitter.

The reference and the signal to be measured, f_a and f_b respectively, are applied to the LM208 operational amplifiers, which form the isolating stages. The LM211 comparators that follow provide a rise time of less than 100 nanoseconds and a phase-shift equivalent time between points A′(f) and B′(f) of less than 20 ns. A



Angular accuracy. Meter utilizes tracking ability of PLL to perform phase measurements accurate to 0.1°. 4046 delivers clock signal equal to 3,600 f_a to conventional display (not shown), where count time is determined by f_b. Thus phase angle of f_b with respect to f_a is displayed.

PHASE METER'S RANGING COMPONENTS				
Frequency (Hz)	C_1 (pF)	R_1 (kΩ)	R_2 (kΩ)	Jitter (ppm)
1 – 10	430	100	∞	15,000
10 – 100	240	10	225	10,000
100 – 300	100	6.8	28	8,000
300 – 1,000	15	2	15	5,000

zero-phase check switch is provided so that the reference may be applied to both channels simultaneously. This allows the user to minimize the aforementioned offset time with channel B's 1-kilohm potentiometer, which is located at the input of its corresponding LM211 comparator.

The reference waveform is then applied to the 4046 PLL, which has a 3,600:1 frequency divider in its feedback loop. The output of the 4046 is thus 3,600 f_a and is virtually in phase with the incoming signal. In order to reduce the phase jitter to a minimal value, the PLL is operated over four ranges selected by means of switches S_{1a} to S_{1c} (see table).

The output of the 4046 serves as the clock for driving a four-digit display circuit, which can be made up conventionally with cascaded sections of 74190 synchronous up/down counters, a set of 7475 4-bit bistable latches, 7447 BCD-to-seven-segment decoder/drivers and suitable displays. (The one-chip ICM7217 provides the counter, latch, and decoding functions and could conceivably be used to reduce the chip count, but requires multiple supply voltages.)

The count is initiated on the rising edge of f_a and is terminated by the leading edge of a pulse from channel B. Pulses are counted on alternate cycles of the incoming wave, to minimize control circuitry. Because the circuit is designed for steady-state phase measurements, there is no loss in accuracy. The (lagging) phase angle of f_b with respect to f_a is then displayed. The 74190 counter circuitry may be simply modified to preset the counters to 360 in the countdown mode, instead of counting up from 0, so that the phase of f_a with respect to f_b may be shown. Flicker is eliminated by appropriate selection of the 555 one-shot's timing components. □