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dual slope dvm

A design is described here for a basic 2½ digit digital voltmeter using the dual-slope integration principle. The DVM has a full-scale sensitivity of 199 mV, but may be extended at the constructor's option with multiplier resistors and shunts to measure other voltages and current.

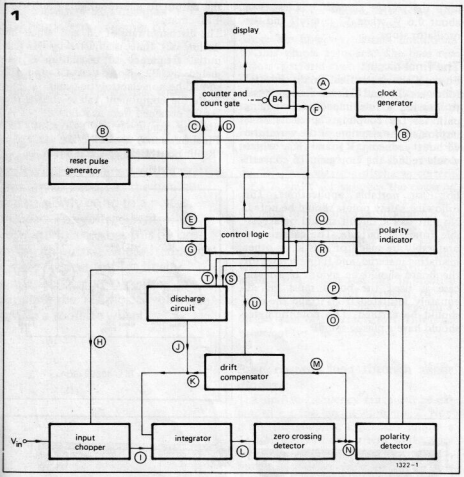


Figure 1. Block diagram of the complete DVM. The arrows in the various connections indicate the direction of action.

Figure 2. The input voltage applied.

Figure 3. The time axis. The time t_1-t_2 is the charging time, t_2-t_3 is the discharge time, and t_3-t_0 is the display time.

Figure 4. Output voltage of the reset pulse generator.

Figure 5. The input voltage to the integrator.

Figure 6. The discharge current of the integrator.

Figure 7. The output voltage of the integrator.

Figure 8. The output voltage of the zero-crossing detector.

Figure 9. The clock pulses applied to the counter. They first consist of 100 reference pulses, which determine the charging time, followed by a number of pulses proportional to the voltage of the input signal. The frequency of these pulses can be assumed to be constant during the time t_1-t_3.

Figure 10. The clock generator. Via line A the pulses go to the count gate, whilst via line B the reset pulse generator is driven.

Figure 11. The reset pulse generator. This supplies reset pulses to the counter (via C and D), and a start pulse to the control logic (via E).

The dual-slope technique is one of the simplest and most reliable DVM systems. The voltage to be measured is fed to an integrator for a fixed period of time. The current into the integrator, and therefore the charge on the integrator capacitor at the end of this period, is proportional to the input voltage. The capacitor is then discharged at a (known) constant current and the time taken for the capacitor to completely discharge is measured. Since the discharge current is constant the time taken to discharge is proportional to the original charge, which in turn is proportional to the input voltage. The discharge time is measured by feeding clock pulses from an oscillator to a digital counter until the voltage on the capacitor reaches zero. The same oscillator is used to determine the original charge time. This means that any long-term variations in the oscillator frequency are unimportant since they will affect both the charge time and the measured discharge time equally. The long-term stability and absolute frequency of the oscillator are thus unimportant. The only reference standard in the DVM is the constant discharge current, which must be stable.

Looking at the system mathematically: Current into integrator $I_1 = V/R$, where V is voltage to be measured and R is integrator input resistor.

Charge on integrator capacitor at end of charge period Δt_1

$$Q = I_1 \Delta t_1 = \frac{V}{R} \cdot \Delta t_1 :$$

Time taken for capacitor to discharge at constant current I_2

$$\Delta t_2 = \frac{Q}{I_2} = \frac{V \Delta t_1}{I_2 R} .$$

Since Δt_1 and Δt_2 are derived from the same oscillator it can be seen that a variation in oscillator frequency will affect both Δt_1 and Δt_2 equally, and the final result will remain the same, provided I_2 does not change and R is fixed.

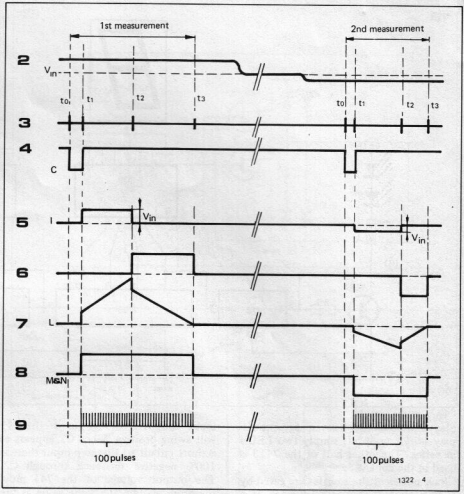
The block diagram of the DVM is given in figure 1 and an operational timing diagram in figures 2-9. The timing diagram is drawn for both a positive and a negative input voltage.

The sequence of operation is as follows: the input chopper applies the input voltage (figure 2) to the integrator for a fixed time t_1-t_2 (figure 3). The chopped input to the integrator is shown in figure 5. During this time the integrator output rises linearly as the capacitor charges (figure 7). The step in the integrator output waveform at the beginning and end of the charge period is explained in the detailed description of the integrator later in the text.

At the end of the charge period the integrator is disconnected from the input voltage and is connected to the discharge circuit. The integrator capacitor discharges linearly during the period t_2-t_3 (figure 6). During the whole period t_1-t_3 the output of the zero-crossing detector (figure 8) is positive. When the voltage on the integrator capacitor reaches zero the output of the zero-crossing detector falls to zero. This is used to control the clock pulses to the counter (figure 9). The operation is effected by the control logic in the block diagram. Before each measuring period the counter and control logic are reset by a pulse from the reset oscillator (figure 4).

Measurement of a negative voltage is performed in a similar manner. The only differences are that the output of the zero-crossing detector is negative. This is detected by the polarity detector and is used to reverse the polarity of the constant current from the discharge circuit. (Otherwise the integrator output, being already negative, would simply become more negative and would never cross zero.)

A refinement is incorporated in the form of a drift compensator circuit, which nulls out the effect of zero drift in the integrator and zero-crossing detector.



Circuits in the DVM

Clock Generator

The clock generator, which provides drive pulses for the counter, is shown in figure 10 and consists simply of a two-transistor astable multivibrator with a frequency of approximately 15 kHz. As stated earlier, the long-term stability of this oscillator is unimportant.

The Reset Pulse Generator

This circuit is shown in figure 11 and is based on a programmable unijunction transistor, T14. The gate of this device receives a D.C. bias from R42 and R43. Pulses from the clock generator are applied to point (B) and charge up C7 through D10 and R41. When the unijunction fires C7 discharges through the unijunction and R44, and the voltage across R44 causes T10 to turn on. This causes T11 to turn off. A negative-going pulse is therefore available at the collector of T10 and a positive-going pulse is available at the collector of T11. The time between reset pulses is determined by the time constant R41 x C7, and in this case is one second. The interval between reset pulses determines the measurement repetition rate and also the time for which each reading is displayed. It may be altered to suit personal taste, provided it is longer than the measuring period t_1-t_3.

C7 should be a low-leakage type, preferably tantalum.

The Counter

The counter circuit (figure 12) consists of two 7490 decade counters and a JK flipflop (half of a 7473). The 7490's count the two least significant decades and drive 7447 seven segment decoders and LED or Minitron displays. The JK flipflop counts the 'hundreds'. Since the maximum display is 199 only a one need be displayed by the hundreds dis-

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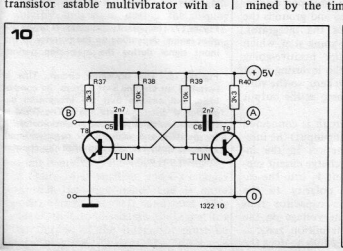

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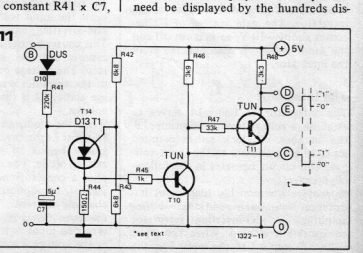
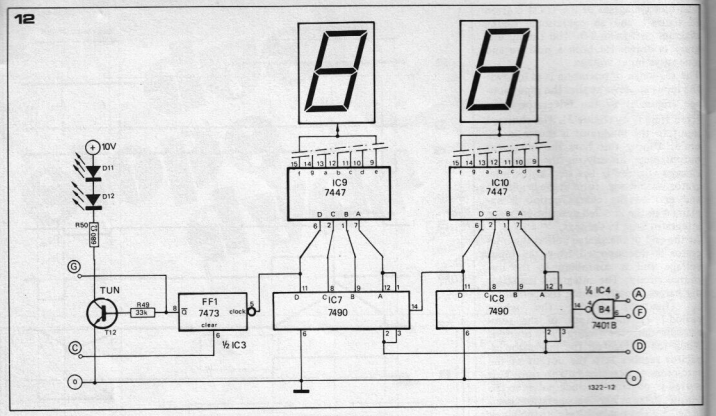




play. For economy, a seven segment display is not used but simply two LED's in series. The other half of the 7473 is used in the control logic.
Clock pulses to the counter are gated by a two-input NAND-gate (quarter of a 7401).

Input Chopper

The input chopper (figure 13) connects the input voltage to the non-inverting input of the integrator during the charge period, t_1-t_2. For the rest of the measurement cycle it grounds this input. The circuit functions as follows:
during the interval t_1-t_2 point H is at logic '1' (+5 V) so T1 is turned off. T2 is also turned off. The gate of F1 is held at about −10 V so F1 is cut off. The gate of F2 is held at about −1.2 V, so F2 is turned on. The input voltage therefore appears at point I via the FET F2, and is thus fed to the input of the integrator.
At time t_2 point H becomes low, so T1 and T2 are both turned on. The gate voltage of F1 becomes about −2 V, so it conducts and grounds the input of the integrator. The gate voltage of F2 becomes about −10 V, so it is cut off and the input voltage is disconnected from the integrator.

The Integrator

The integrator of figure 14 serves to establish a voltage-time relationship, i.e. the number of clock pulses counted must be proportional to the input voltage. The circuit operates in the following manner:
to achieve a reasonably high input impedance without additional buffer amplifiers a non-inverting integrator configuration is used. When the input voltage is applied to the input I by the input chopper, the output of the 741 will swing positive. Since C2 appears as a short circuit to this step input there is 100% negative feedback through C2. The output voltage of the 741 must therefore assume the same value as the voltage on the inverting input (pin 4), which by definition is the same as the input voltage on pin 5. The input voltage thus appears at the output as a positive-going step. Since there is now a voltage across R12 a (constant) current flows through it which is proportional to the input voltage. Since no current can flow into the inverting input of the 741 this current must flow into C2. Since the current is constant the charge on the capacitor, and therefore the voltage across it, increases linearly. The capacitor is allowed to charge for a period of 100 clock pulses. The voltage across C2 is then

$$V = \frac{I_1 \cdot \Delta t}{C_2} = \frac{V_{in} \cdot \Delta t}{R_{12} \cdot C_2}$$

where Δt represents the time interval t_1-t_2.
At time t_2 the input chopper disconnects the input voltage and grounds the non-inverting input of the integrator. This causes a negative-going step, which cancels out the earlier positive-going step. The voltage on the inverting input of the amplifier is now zero, so the voltage across C2 is the same as the output voltage.
When the discharge circuit is connected to point J (the inverting input) the integrator begins to function in the inverting mode. The discharge circuit supplies a constant current I_2 into the capacitor of opposite polarity to the charging current. The capacitor thus discharges linearly. The voltage on the inverting input is, by definition, zero, so as the voltage across C2 falls so does the

Figure 12. The counter. C and D are reset inputs, A is the count input, F the driver for the count gate. Output G supplies a pulse to the control logic at the one hundredth count pulse.

Figure 13. The input chopper. It is driven via line H, and during the time t_1-t_2 it passes the input signal on to the integrator (via line I).

Figure 14. The integrator. I is the input and L the output. The lines J and K, come from the discharge circuit and the drift compensator, respectively. C2 is the integration capacitor. P1 serves for zero-adjustment: with input I to earth and the lines J and K interrupted, the output L must be adjusted to 0 with this potentiometer.

Figure 15. The zero-crossing detector. It amplifies the output voltage of the integrator (line L), and drives the drift compensator and the polarity detector (via M and N).

Figure 16. The polarity detector. This is in fact a three-position switch: for input voltages higher than +600 mV output 0 is 'low' and P 'high'; for voltages between +600 mV and −600 mV both outputs are 'high'; whilst for voltages below −600 mV 0 is high and P is low.

Figure 17. The polarity indicator. It drives the pilot lamps, depending on the polarity of the input signal during the measuring period.

Figure 18. The discharge circuit. This is switched on via line S or T from the control logic, and ensures that the integration capacitor is discharged via line J. The DVM is calibrated with adjustment potentiometer P2 for positive, and with P3 for negative input voltages. Both are adjusted until the counter indicates one unit per millivolt.

741 output voltage (which is identical). During this time the counter is counting clock pulses, until the zero-crossing detector monitors zero volts on the output of the 741. The discharge time Δt_X is given by:
voltage on C2,

$$V = \frac{I_1 \cdot \Delta t}{C_2} = \frac{I_2 \cdot \Delta t_X}{C_2}$$

therefore

$$\Delta t_X = \frac{I_1 \cdot \Delta t}{I_2}$$

but

$$I_1 = \frac{V_{in}}{R_{12}}$$

therefore

$$\Delta t_X = \frac{V_{in} \cdot \Delta t}{R_{12} I_2}$$

Since Δt, R12 and I_2 are all fixed Δt_X is proportional to V_{in}.

The Zero-Crossing Detector

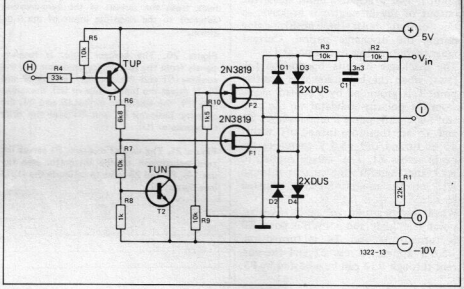
This circuit also uses an op-amp (figure 15), but in this case a 709 is used which has a greater slew-rate than the 741. The circuit has a high gain, about 70 ×, so a small swing of the input voltage positive or negative will make the output swing hard over to plus or minus 10 V. D5 and D6 provide input protection by limiting the voltage on pin 5 of the IC to about ±0.2 V maximum, and R23 limits the current through the diodes. C3 and C4 are included to keep the 709 stable.
The output of the zero-crossing detector is connected to the input of the polarity detector (figure 16). For outputs from the zero-crossing detector greater than +0.6 V T6 is turned on and T7 is turned off, while for outputs more negative than −0.6 V T7 is turned on and T6 is turned off. For voltages between −0.6 V and +0.6 V both transistors are turned off, thus providing a zero indication.

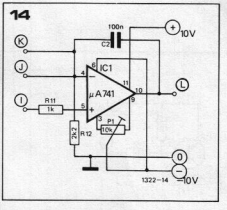
Polarity Indicator

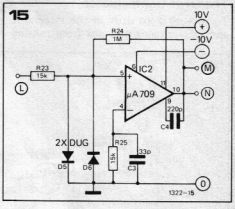
This consists of two high power NAND-gates (7440), connected as a set-reset flipflop (figure 17). During the measuring period this flipflop is either set or reset by the polarity detector depending on the polarity of the measured voltage and the appropriate LED is lit. The flipflop is necessary to store the polarity indication during the display period, when the output of the integrator (and hence of the zero-crossing detector) is zero.

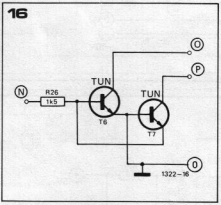
The Discharge Circuit

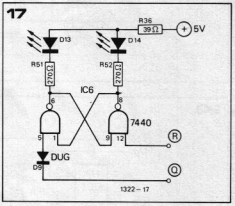
There are in fact two discharge circuits, one of which is used depending on the polarity of the input signal. The circuit is shown in figure 18. When the input signal is positive, the output of the 741 in figure 14 is positive, and C2 charges so that the 'right-hand' end is more positive than the 'left-hand' end. This means that to discharge the capacitor the output of the integrator must be negative-going during the discharge

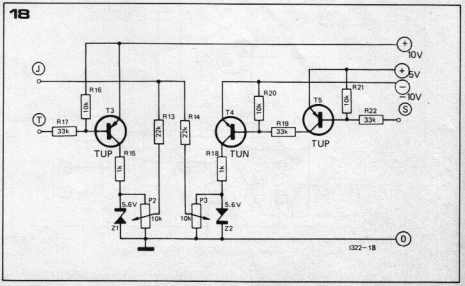












period. Current must therefore flow into point J. For a negative input signal the output of the integrator is negative, so the output must be positive-going during the discharge period. Current must therefore flow out of point J.

The discharge circuits operate as follows: when the input signal is positive point T is grounded by a control signal from the polarity indicator via the control logic while point S remains high. T4 and T5 are therefore turned off, whilst T3 is turned on. +5.6 V therefore appears across Z1. The voltage applied to R13, and therefore the current through R13 into the integrator, can be adjusted by P2.

When the measured voltage is negative, point T is 'high' and point S is 'low'. T3 is turned off and T4 is turned on. −5.6 V appears across Z2 and the current through R14 can be adjusted by P3.

The Drift Compensator

To prevent zero drift in the integrator and zero-crossing detector from causing inaccuracies feedback is applied round these circuits during the display period. During this time point U is low, so T13 is turned on and hence F3 is conducting (figure 19). Points M and K are connected to the output of the zero-crossing detector and the inverting input of the integrator respectively, so any voltage offset on the output of the zero-crossing detector will be integrated, which will tend to null out the offset.

During the measuring period point U is 'high', and the drift compensator is switched off so that the integrator and zero-crossing detector can function normally.

Figure 19. The drift compensator. It is switched on via line U, and provides a feedback from the output of the zero-crossing detector to the inverting input of the integrator.

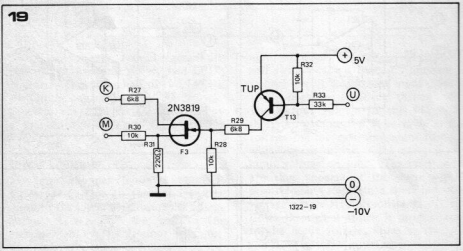
Figure 20. The control logic. It receives signals from the reset pulse generator (E), the counter (G) and the polarity detector (0 and P). It drives the input chopper (H), the count gate (F), the discharge circuit (S and T), the polarity indicator (Q and R) and the drift compensator (U).

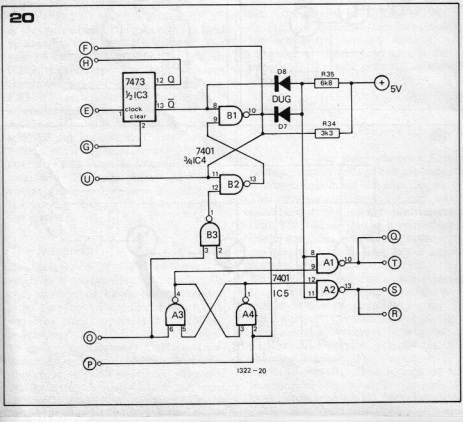
Figure 21. The overall diagram. P1 serves for zero adjustment of the integrator (see figure 14). P2 and P3 serve to calibrate the DVM (see figure 18).

Control logic

The measurement sequence timing is performed by the control logic, the circuit of which is given in figure 20. The measurement sequence starts with a positive pulse from the reset pulse generator, which resets the counter via point D (figure 12). This pulse is also applied to point E of the control logic, and on the trailing edge of the pulse the JK flipflop (½IC3) is set. The Q output connected to line H switches on the input chopper, whilst the $\bar{Q}$ output goes 'low' and sets the set-reset flipflop consisting of two NAND-gates. Output F thus goes 'high', opening the gate to the counter, so that it begins to count clock pulses. The drift compensator is also switched off via line U. A negative going pulse presets FF1 in figure 12 via line C. The $\bar{Q}$ output of the 7473 holds the inputs of gates A_1 and A_2 low via D8, which holds both inputs to the discharge circuit (S and T) high. The discharge circuit is therefore inoperative.

When 100 clock pulses have been counted (time t_2) output G in figure 12 goes 'low', resetting the JK flipflop (½IC3). The input chopper is now switched off via line H. In the meantime the flipflop comprising A_3 and A_4 has been either set or reset by the polarity detector. Since the $\bar{Q}$ output of the 7473 is now 'high' the outputs of A_3 and A_4 can be gated through A_1 and A_2 to set the polarity indicator via lines Q and R, and also to enable the appropriate part of the discharge circuit. The counter continues to count clock pulses. Note that it is not necessary to reset the counter at time t_2, as at the hundredth pulse it has reached zero! When the output of the integrator reaches zero the output of the zero-crossing detector is also zero. Both outputs of the polarity detector go 'high', so the output of gate B_3 goes low, resetting the flipflop (B_1 and B_2), which disables the discharge circuit via D7 and A_1, A_2. The counter gate is closed via line F so the count ceases. The display now indicates the measured value of the input voltage until the next reset pulse.





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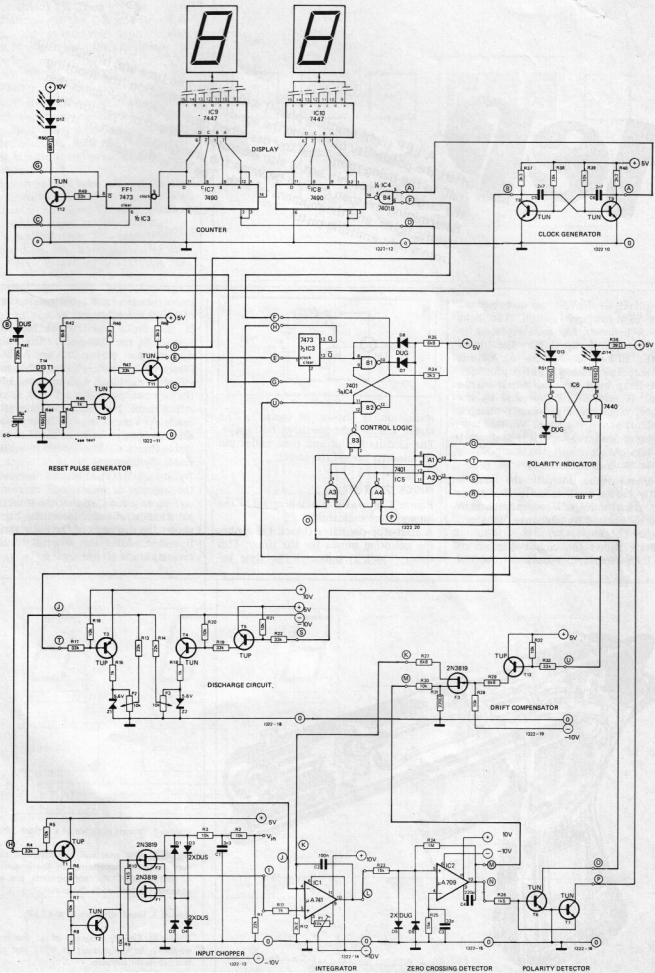
DISPLAY
COUNTER
CLOCK GENERATOR
RESET PULSE GENERATOR
CONTROL LOGIC
POLARITY INDICATOR
DISCHARGE CIRCUIT
DRIFT COMPENSATOR
INPUT CHOPPER
INTEGRATOR
ZERO CROSSING DETECTOR
POLARITY DETECTOR