An AM/FM/CW S
RF Signal Genera

This low-cost, easy-to-build and user-friendly RF signal generator covers from 100kHz–50MHz and 70–120MHz, and is usable up to 150MHz. It generates CW (unmodulated), AM and FM signals suitable for a wide range of tests. Its output level is adjustable anywhere between -93dBm and +7dBm and it has an accurate frequency display. It also includes a scanning function for filter alignment.

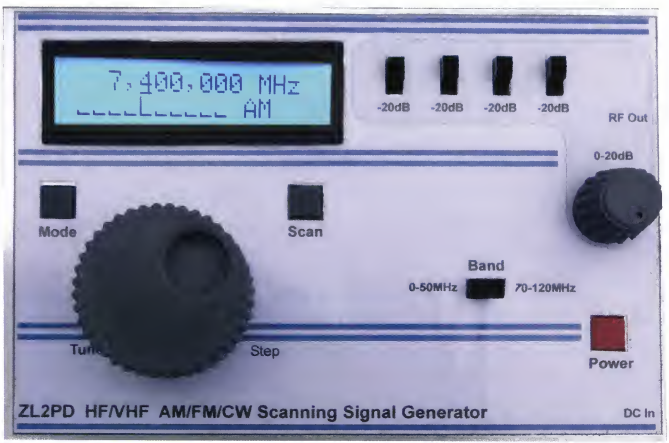
I've always wanted a *good* AM/FM HF/VHF signal generator. I have tried to meet that need with a variety of designs over the years, some analog, others using DDS chips.

More recently, I have tried low-cost fractional-N oscillator chips, including the Si5351A. These were only suitable in specific circumstances, and did not make for a good general-purpose test instrument.

Obviously, it's possible to purchase an RF signal generator, new or used, but I couldn't afford the price of a good one. Cheap signal generators lack adequate performance and useful functions. Those with adequate performance are usually too expensive for most hobbyists or are unreliable and difficult and/or expensive to maintain.

I have seen some designs published, but these are typically simple analog LC-based designs with coverage up to around 150MHz, in a series of five or six switch-selected bands.

Most lack accurate frequency readouts or adequate stability. Spurious



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Part 1

by Andrew Woodfield, ZL2PD

and harmonic outputs can also be a problem.

(See the list of references at the end of this article for three such designs that I considered and rejected).

Table 1 (overleaf) shows what is available at the moment. I rejected all of these options for one reason or another – inadequate performance, lack of features, high price or unreliability.

With few exceptions, the output levels of most of these generators are quite limited. Those with a variable output level typically use a simple potentiometer, with little regard to varying output impedance or accuracy.

Output levels are also often too low for use in many typical applications.

Modulation, where available, is often limited. And, finally, some otherwise useful digital-based designs are now difficult or impossible to build due to obsolete parts or unavailable software or PCB layouts.

Basic analog and digital PLL-based RF signal generators are available between about $200 and $300. The analog generators offer basic CW, AM or FM modulation. Output level and modulation depth on the low-cost analog generators are typically controlled via internally mounted trimpots adjusted through small holes in the panel.

The low-cost digital signal generators only offer FM and appear aimed at the two-way radio industry.

These instruments are all perfectly functional, but for hobbyists, these features are too limited. To use them effectively, you would also need extra equipment such as a frequency counter, attenuators, amplifiers and a level meter. It's far easier to have these features built into the generator.

As Table 1 shows, moving up in the market significantly increases the price. Used equipment is available at lower cost, but many otherwise excellent instruments have recognised spare parts or reliability issues as the equipment ages.

So I needed to come up with my own design that would tick all the boxes, and that is just what I have done. See the table below which lists its features and performance figures.

Features and specifications

	Specification	Comments
Coverage	100kHz-50MHz, 70MHz-120MHz	Usable up to 150MHz
Tuning Steps	10Hz to 1MHz in decade increments	User-selected
Accuracy & stability	Within 150Hz at 30MHz (typical), 0-40°C, 0-80% humidity	Can be enhanced with software calibration
Output level	-93dBm to +7dBm (approximate)	50Ω termination
Attenuation steps	0-80dB in 20dB steps (switched) + 0-20dB (variable)	
Output socket	SMA	
Spurious and harmonics	Typically better than -30dBc	Within specified coverage frequency range
AM	30% modulation @ 1kHz	
FM	NB (12.5kHz spacing), 1.75kHz deviation @ 1kHz (60%)	
	WB (25kHz spacing), 3kHz deviation @ 1kHz (60%)	
	BC (12.5kHz spacing), 50kHz deviation @ 1kHz (60%)	Suitable for standard broadcast FM receivers
Scanning	Programmable start and stop frequencies	1kHz resolution
	10, 20, 50, 100, 200 or 500 steps/sweep	Auto step size calculation
Display	16x2 alphanumeric LCD	
Power control	Soft on/off switch	
Controls	Two knobs and eight switches	
Power supply	9-12VDC at 250mA	
Dimensions	160 x 110 x 25mm (excluding knobs)	
	160 x 110 x 45mm (including knobs)	
Weight	~250g	

PRODUCT	TYPE	PRICE BAND ($US)	FREQUENCY COVERAGE	OUTPUT	MODULATION	FEATURES
Generic brands	Analog	$150–$200	100kHz–150MHz in six bands	0–100mVpp	Basic AM, FM	Analog dial, internal presets for user controls
Generic brands	Digital PLL#	$150–$200	500kHz–470MHz	–132 to –70dBm	CW, FM	2 line x 16 char LCD display
RF Explorer	PLL and dividers	$200–$300	24MHz–6GHz	–40 to 0dBm	None	Sweep functionality
ERAsynth	PLL, controlled by user PC or smart device	$950	250kHz–6GHz	–60 to +15dBm	AM, FM, pulse via external apps	Software apps control functionality
Digimess SG200	Digital	$2500	9kHz–450MHz	–127 to +13dBm	AM, FM, FSK, PSK	Sweep functionality
Used signal generators, eg Marconi 2022, HP8640	Digital/PLL	$500–$1000	10kHz–1000MHz	–127 to +13dBm	AM, FM, FSK, PSK	Excellent performance, but some models have recognised maintenance issues
Keysight, R&S, Tektronix, IFR, TTi, Rigol, Grotten, etc.	Digital	$3000–$20,000+	10kHz–15GHz (depends on model)	–140 to +20dBm, typically	All (AM, FM, PM, FSK, QPSK, etc.)	Extensive array of features and functionality

Table 1: I looked at a range of currently available commercial equipment, both new and used. However, for anything that had better-than-mediocre performance, that third column definitely caused me some heartache! I estimate the instrument described here could be built for not much more than $75.00, plus case.

Design goals

This design represents the outcome of an extended period of development and testing over the last few years.

This signal generator provides basic CW (unmodulated) signals, plus AM and FM modulation functions, primarily across the high frequency range from 100kHz to 30MHz, with a continuously variable output level suitable for most requirements.

This frequency range includes most common IFs (intermediate frequencies) such as 455kHz, 465kHz, 470kHz, 10.7MHz and 21.4MHz.

Coverage extends to 50MHz, with another range covering 70-120MHz. Coverage actually extends up to 150MHz with some limitations, to permit limited use in the popular 2m amateur radio band as well as parts of the widely used international 138-174MHz land mobile band.

Key design objectives included low cost, ease of obtaining parts and ease of construction.

Special parts such as chip-based attenuators, for example, were avoided in favour of the low-cost combination of slide switches and standard resistors.

The generator's RF output is designed for applications requiring relatively high RF levels.

These include testing double-balanced diode mixers in high-performance receivers and for testing multi-stage passive filters, where stopband attenuation measurements require relatively high signal generator outputs.

Lower RF output levels are also useful, eg, for receiver sensitivity tests. The minimal useful level is mostly determined by the limitations of low-cost shielding and simple hobbyist construction methods used.

If an enclosure was carefully milled from a 25mm thick metal billet with shielding slots for flexible conductive inserts, the lower limit could be extended significantly, but relatively few hobbyists could achieve this. So I've used simple shielding and a basic DIY folded aluminium sheet metal box. This is reflected in the modest lower output specification limit of around -90dBm.

Achieving that performance, however, still requires moderately careful enclosure construction.

By using commonly available parts and low-cost modules, I have been able to keep the overall cost low. I estimate the cost to build this signal generator currently at around $75.

Design approach

As shown in Fig.1, a modern signal generator consists of five functional blocks: the RF oscillator, the modulator, RF buffer amplifier, a variable attenuator to control the output level, and some control electronics. The logical implementation of the control electronics is based on a microcontroller. The final block is the power supply, either battery-powered or mains-powered (or both).

The oscillator is a key element of any signal generator. An analog-based wide-range oscillator and modulator involving sets of inductors and a tuning capacitor is impractical and cannot provide the desired functions and performance required at a modest cost.

The cheapest digital options include the powerful Silicon Labs Si5351A device or widely available direct digital synthesis (DDS) modules based on chips such as the Analog Devices AD985x (see our article on the AD9850 in the September 2017 issue; siliconchip.com.au/Article/10805).

Other digital options include PLL chips such as the Maxim MAX2870. While it is possible to generate sinewaves from both the Si5351A and the MAX2870, the additional circuitry required to obtain low harmonic content output signals coupled with the challenges of adding modulation make them less attractive.

AD9850 DDS modules (as shown in the photos overleaf) are available from sources like ebay and AliExpress at reasonable prices.

The instrument's display requirements are modest, so I decided to use a common 16x2 character alphanumeric LCD. These are easy to read and drive from a micro.

A rough outline of the design began to take shape and, adding up processor pins required, the very common

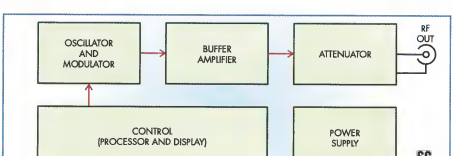


Fig.1: the basic arrangement of a modulated signal generator with adjustable output level. Our design follows this configuration.

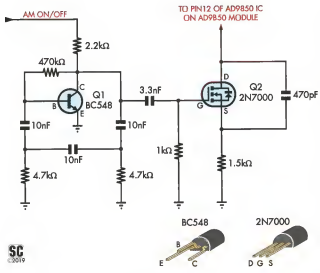


Fig.2: a typical example of how you can apply amplitude modulation to the output of an AD9850-based signal generator module using discrete components. In the end it was decided to abandon this idea in favour of a PWM-based microcontroller approach.

ATmega328P 8-bit microcontroller appeared suitable. While an Arduino was briefly considered, I would need to use practically every pin on the device, and I wanted to keep the instrument compact, so I decided to use a stand-alone ATmega328 processor.

The RF buffer amplifier requires only modest gain. It must handle the somewhat unusual 200Ω output impedance of the AD9850 module and the following 50Ω attenuator stages and 50Ω output. Another consideration is that the buffer should not be overloaded by the sometimes high output swing of the AD9850. Numerous designs published on the internet suffer from this problem.

The buffer should also maintain its gain across the design frequency range. And the buffer should be able to work into a reasonable range of loads and survive typical bench treatment.

I've used MMIC amplifiers such as the ERA-series devices from Mini-Circuits to buffer AD9850, AD9851 and AD9854 DDS chips in the past. These drive 50Ω loads with good performance.

However, in testing this signal generator with a wide variety of filters, amplifiers, receivers, transmitters and other loads, several MMICs suffered early deaths. These were probably due to the very low impedances presented by some of the test filters.

The search for a more suitable buffer stage was ultimately concluded with the inclusion of a traditional single-stage buffer amplifier using a robust 2N4427 VHF transistor. It is widely available at low cost, as is its near-equivalent, the 2N3866. It proved more than adequately robust over many months of use. The TO-39 case of the transistor becomes warm during use, but a heatsink is not required.

The design of the attenuator stage also posed some challenges. Recently, PE4302 30dB step attenuator chips have become popular. While only relatively new devices, these have recently been listed by the manufacturer as obsolete. The replacement devices, while having improved performance, also come at a substantially increased price.

Relay-controlled fixed attenuators can be used, but with an eye on cost and simplicity, I decided to use inexpensive slide switches instead. Experience has shown these to perform adequately for this type of application. However, these limit the attenuator steps to specific attenuation values. Ideally, the generator should have a fully variable output level.

So I decided to build and test a Serebriakova attenuator as an alternative to a more costly PIN diode-based design. This configuration is shown in the lower right-hand corner of Fig.4, the circuit diagram.

It's a simple passive resistor network which acts as a variable attenuator, well suited for basic designs like this. Apparently of Russian origin, the attenuator network uses a 500Ω linear potentiometer to give a 20dB variable attenuation range. It works well into mid-VHF frequencies.

The input impedance is maintained reasonably close to the desired 50Ω across the adjustment range of the potentiometer, so the attenuation is predictable. The output match to 50Ω as the potentiometer is adjusted

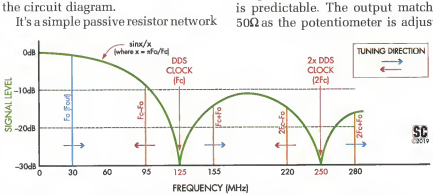


Fig.3: the output of a DDS signal generator module contains the wanted frequency plus a number of alias frequencies. These are normally filtered out but it is possible to instead filter out the fundamental frequencies and keep one of the higher alias frequencies to extend the signal generator's range.

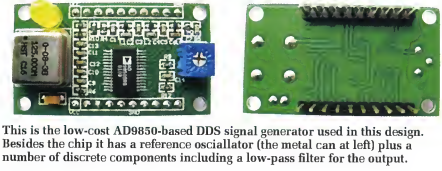
What is Frequency Modulation (FM)?

With frequency modulation, the audible tone of (say) 1kHz results from the carrier frequency of the signal generator being instantaneously shifted (or "deviated") from its nominal frequency in proportion to the amplitude of the modulating tone.

As the amplitude of the tone increases, at that 1kHz rate, the carrier frequency of the generator proportionally increases. Similarly, as the 1kHz tone's amplitude decreases, the carrier frequency is proportionally decreased. It is proportional because the extent of the carrier frequency shift, or deviation, depends on the signal bandwidth required.

For broadcast radio FM, the peak deviation is ±75kHz. The resulting signal fills the standard FM broadcast channel bandwidth of 200kHz. Traditional VHF FM two-way radio transceivers used for amateur radio or commercial/government mobile radio use a much smaller ±5kHz deviation, and these signals occupy 25kHz channels.

More modern so-called "narrow-band" amateur FM transceivers typically use ±2.5kHz deviation, and these use more densely-packed channels spaced apart by 12.5kHz.



This is the low-cost AD9850-based DDS signal generator used in this design. Besides the chip it has a reference osciallator (the metal can at left) plus a number of discrete components including a low-pass filter for the output.

is not perfect, but it's an acceptable compromise for this design.

Amplitude modulation with the AD9850

A key objective of the signal generator was to deliver both amplitude (AM) and frequency modulation (FM) as well as providing an unmodulated RF signal.

Amplitude modulation with the AD9850 is well documented. Analog Devices, the chip's manufacturer, helpfully published an application note (AN-423) which describes adding a small signal NMOS FET and a few additional parts to do this. A quick test confirmed that it works as described.

Most signal generators use a 1kHz modulation tone, which can be produced in several ways. One approach is to use the ATmega328 to generate a 1kHz square wave using one of its internal timers and then filter this to give a 1kHz sinewave. But extensive filtering is required to obtain a suitable tone. That involves quite a few extra parts.

A second, similar approach is to use the ATmega328's counter/timer in its pulse-width modulated (PWM) mode. The resulting waveform is closer to a sinewave but still requires some filtering to remove the 31kHz PWM frequency. Usefully, that filter is far less complex given the much higher clock frequency compared to the 1kHz tone.

A third option is to build a discrete 1kHz sinewave oscillator and just use the ATmega328 to turn it on and off as required. At first glance, the discrete oscillator approach is attractively simple and uses relatively few components, so I tested this out, using the circuit shown in Fig.2.

It works quite well. The 3.3nF capacitor value can be adjusted to give the required modulation level at the AD9850's RF output. This works by replacing the fixed resistor ("RSET") on pin 12 of the AD9850, typically 3.9kΩ, with the variable resistance of Q2's channel. This resistance sets the AD9850 digital-to-analog converter (DAC) current and, subsequently, the AD9850 RF output level.

By varying the gate voltage of the 2N7000 at 1kHz using the voltage from the collector of audio oscillator Q1, the AD9850 RF output is amplitude modulated.

However, this analog tone is not precisely 1kHz. Its frequency is determined by the passive components around Q1. To give a more accurate (and potentially adjustable) modulation frequency, the PWM-based approach was used in the final circuit. See the section of Fig.4 labelled "OUTPUT LEVEL CONTROL".

Pin 11 (output PD5) of IC1 produces the 1kHz sinewave as a 31kHz PWM square wave, or potentially at other frequencies by changing the software. This is filtered and used to control a current sink made using standard NPN transistors. An extra 100nF bypass capacitor was added to pin 12 to the final PCB to address AD9850 module stability.

The 31kHz pulse width modulated 1kHz signal is produced by the ATmega328 from its 8MHz internal RC oscillator. The variable DC voltage of 0-5V arriving on the base of Q1 is converted to a variable collector current in Q1 of 0-700μA, the maximum current value being set by its 1kΩ emitter resistor. This figure was selected to exceed the 625μA maximum current sink range required by the AD9850.

This approach is not perfect. Using the RSET pin and the standard unbalanced RF output from the AD9850 module, the typical approach used in these low-cost modules, the output modulation produced is asymmetric. In practice, however, this does not matter terribly.

This simple circuit delivers clean-sounding amplitude modulation with the AD9850 and uses fewer components than the other options. It also allows other modulation tones to be added in future if required. Finally, this approach also adds another important feature – reasonably accurate linear control of the AD9850 RF output level.

Note though that this approach requires the removal of that 3.9kΩ resistor from the module as supplied, and the addition of a wire to control pin 12 from Q1 to one of its pads. This change will be described in more detail later.

Frequency modulation (FM)

Again, there are several options to produce FM with the AD9850. One approach would be to externally modulate the AD9850's separate 125MHz reference crystal oscillator. Frequency and phase modulation could be both implemented this way. Unfortunately, the 125MHz reference oscillator in the low-cost modules is inside a sealed metal can.

There is no external voltage tuning input which might otherwise be pressed into use to produce FM. It's possible to replace the reference oscillator module with a discrete oscillator to allow for external modulation, but that takes some effort.

It is also possible to use the AD9850 internal phase modulation register but resolution is too limited (4 bits).

Another Analog Devices application note (AN-543) suggests a solution. It describes a powerful Analog Devices DSP chip which samples incoming stereo audio at 48ksamples/sec and then sends a stream of 40-bit frequency-setting words serially at very high speed to the AD9850.

Each of these 40-bit words programs the AD9850 to a new instantaneous frequency, which is necessary to emulate a stereo FM signal (including the 19kHz and 38kHz pilot tones).

With some care and a few lines of assembly code for speed where necessary, the ATmega328 can modulate the AD9850's output frequency in this manner. Sadly, the resulting modulation sounds pretty average. The problem is the time required by the ATmega328 to send the serial string of 40 bits to the AD9850 each time its frequency has to be updated for frequency modulation via the typical 3-wire interface.

The poor result is not surprising. With the conventional serial load

method and our 8MHz, 8-bit chip, it is (just!) possible to load four modulation samples per 1kHz cycle into the AD9850. A four-point sinewave is actually a triangle wave, which is full of harmonics!

Closer study showed that there is another way to communicate with the AD9850 chip. Almost every AD9850/51 based design uses the three-wire serial bus to send 40-bit control words to the AD9850 each time the frequency needs to be updated.

However, the AD9850 can also be controlled using a parallel interface. This requires sending five 8-bit words in quick succession to the chip, along with some control signals via two or three additional pins. The only published example I could find is based on a PIC processor.

There is a considerable advantage in this method. Rather than taking about 250µs for the ATmega328 to load each 40-bit word serially, the parallel approach can reduce this to as little as 2.5µs.

With the parallel loading method, it is possible to send 20 samples per 1kHz cycle without any trouble at all, even with the (relatively) slow 8MHz clock in the ATmega328. This is much closer to a proper sinewave. The difference is clearly audible in an FM receiver. The parallel method gives a demodulated signal that sounds very clear and clean, just like a sinewave should.

So for FM, the 20-point sampled waveform is created by calculating the required AD9850 output frequency every 50µs and sending that data over the fast parallel interface.

The FM deviation is controlled by changing the magnitude of the frequency changes which occur 20,000 times per second (20 points x 1kHz).

Selecting narrow band FM (the LCD shows "FM-NB") on this generator for 12.5kHz spacing FM two-way radios produces ±1.5kHz FM; selecting wide-band FM, for older 25kHz channel spaced two-way radios, gives ±3kHz FM ("FM-WB"), while selecting broadcast FM produces ±50kHz FM signals ("FM-BC").

Frequency scanning

A further feature of this signal generator was added for testing and aligning filters. For example, while designing this Signal Generator, I was also building a 9-band HF transceiver. Its receiver front end features nine sets of coupled tuned circuits, each requiring careful alignment, with three or four adjustments per set.

In the scanning mode, the generator briefly produces a signal on a series of discrete frequency steps across a defined range. For the transceiver example, the signal generator could be programmed to produce signals across each of the nine bands used for the bandpass filters being tested.

By monitoring the amplitude of the resulting output from each filter on an oscilloscope, it is possible to quickly align each filter while seeing the impact of every change. This forms, in effect, a 'poor man's spectrum analyser'. This saves considerable time and effort over manual alignment methods.

The start and stop frequencies can be set anywhere across the range of the signal generator. Since filters are generally fairly broad, a 1kHz step size for setting the start and stop frequency is acceptable.

I decided to add a SCAN pushbutton to the design, to enable this mode. As I had run out of pins on the ATmega328, I used two diodes (D1 & D2) so that pressing this button is effectively equivalent to pressing the two existing buttons (MODE and STEP) simultaneously. The micro can detect this as a press of the SCAN button – see Fig.4.

Expanded frequency coverage

Typical AD9850 modules are fitted with a 125MHz reference oscillator. DDS oscillators deliver clean sine outputs up to about 30% of the reference frequency; in this case, say 40MHz. Increasing but acceptable levels of aliasing products are present in the output spectrum up to 45% of the reference frequency, say 50MHz.

Beyond this, as the output frequency approaches the Fourier limit of about 60MHz, spurious products render the output unusable.

The cheap modules are usually supplied with an onboard elliptical low-pass filter with a cutoff frequency of 70MHz to maximise the output frequency range. In fact, these modules have three outputs. The first is the filtered output as described. It appears on my module on the pin labelled "SINB".

An adjacent pin, "SINA", might appear to be similar. However, this signal comes directly from the AD9850 DAC. It is a 180° phase-shifted (inverted) version of the signal at SINB but without any additional low-pass filtering.

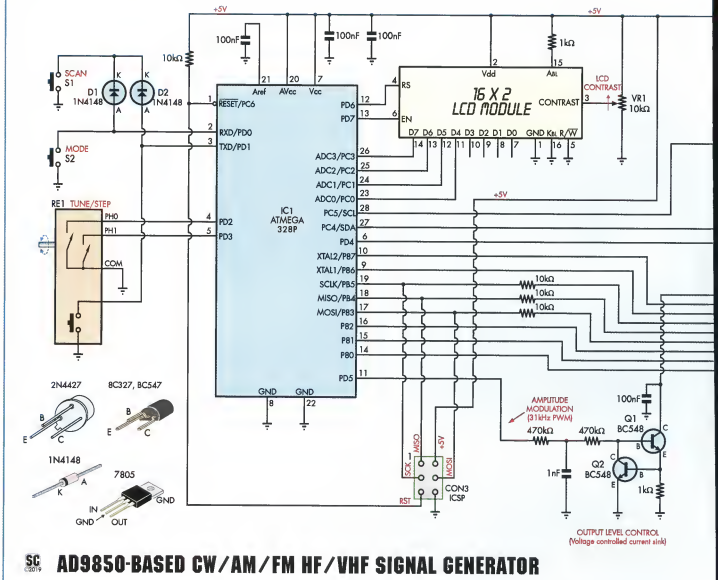
The third available output comes from an internal comparator in the AD9850. It produces a square wave version of the output. This is output level dependent, the duty cycle being set by adjusting a miniature trimpot on the module. If it is adjusted for a good 50% duty cycle output at a lower frequency setting, it tends to be less accurate at higher frequencies.

There is little difficulty in obtaining reasonably clean filtered signal generator outputs up to 50MHz from the filtered (SINB) pin. Some testing showed that output was acceptable down to 100kHz. That's useful for covering receiver intermediate frequencies (IF) and IF filters between 455kHz and 470kHz, for example.

Looking more closely at the module, the second SINA output looked potentially useful too. Because this output is not filtered, the full set of DDS alias frequencies are available here.

In one example, illustrated in Fig.3, the "wanted" output (labelled Fout) is at 30MHz. As the user increases this frequency, tuning towards 35MHz for example, this output frequency increases, shown by the blue arrow.

At the same time, the AD9850 (like



AD9850-BASED CW/AM/FM HF/VHF SIGNAL GENERATOR

Fig.4: along with the 16x2 LCD module, the ATmega328P microcontroller (IC1) drives the AD9850 signal generator module using an 8-bit parallel bus plus three control lines. This allows it to modulate the output frequency at 20kHz which results in clean 1kHz frequency modulation. Amplitude modulation is applied using PWM from pin 11 of IC1, which is filtered and then controls a current sink comprising transistors Q1 and Q2. The resulting current flow controls the signal generator output level. The output signal is buffered by transistor Q3 and then passes four switched 20dB attenuators and then a 0-20dB variable attenuator (VR2) which gives a 100dB overall output range. Q4 and Q5 form a "soft power" switch for the circuit, which is controlled by pushbutton switch S3.

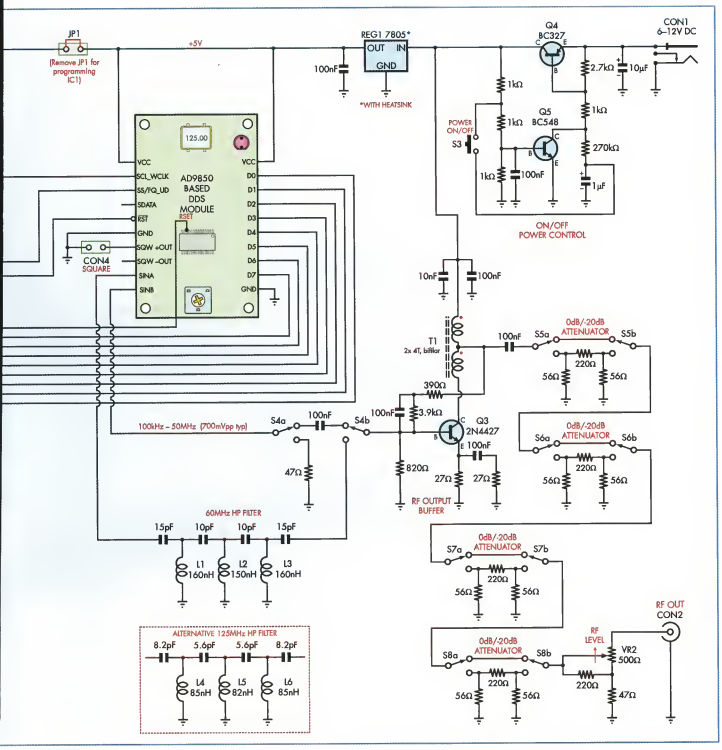
all DDS chips) also produces "alias" frequencies. These are shown in orange. The nearest is at 95MHz, ie, the clock frequency of the DDS (125MHz) minus 30MHz. It decreases in frequency as the user tunes from 30 to 35MHz, ending up at 90MHz (ie, 125-35MHz).

There are many other alias frequencies which are produced simultaneously, the next nearest being at 155MHz (the clock frequency of 125MHz plus 30MHz), with others at 220MHz, 280MHz and so on, theoretically continuing forever. The direction these alias outputs tune can be seen by the direction of the arrows, some rising while others reduce in frequency as the primary frequency is increased.

The amplitude of all of these signals follows a strict mathematical relationship, called the "sine x upon x" curve. That's shown in green on the figure. There's about a 10dB level difference between the 30MHz output and the 95MHz alias signal, for example.

That's the reason for the substantial onboard filter on the AD9850 module. It's a low-pass filter designed to cut off at 70MHz, so the majority of these aliased products do not appear at the SINB output. However, since there is no similar low pass filter on the SINA output, these alias signals are all usefully present, in full, at this pin.

As the user continues to tune the AD9850's output upwards in fre-



quency, the 'wanted' and first 'alias' output ultimately coincide and pass each other at Fout=62.5MHz.

A few tests using this SINA pin suggested that the usually unwanted alias frequencies above 65MHz could be obtained from the module using an external high-pass filter (HPF). That would allow the signal generator to provide useful outputs from, say, about 70MHz up to about 120MHz. With additional filtering, still higher aliasing products could be filtered out and amplified.

This permits the generator to produce signals across the 2m amateur band or across part of the 138-174MHz land mobile bands. As it turns out, useful outputs across these bands could be obtained just from using a single HPF, and the maximum tuning frequency for the signal generator was therefore set at 150MHz. Those wanting other bands or fewer aliasing outputs can modify the HPF to suit individual requirements.

Detailed circuit description

The final circuit arrangement is shown in Fig.4.

While it may appear complex at first glance, this design uses remarkably few components given the range of modulation modes and coverage it provides. Some of the complexity is hidden in the software for IC1.

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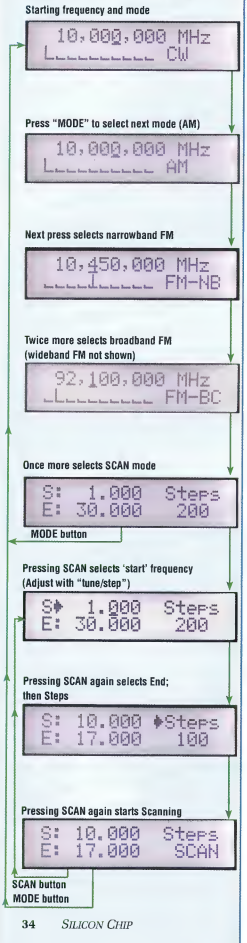


To enable the frequency modulation described above, the AD9850's 8-bit data port (pins D0-D7) is connected to micro IC1's PORTB digital outputs (PB0-PB7). The three 10kΩ series resistors have been added so that IC1 can be reprogrammed in-circuit (via ICSP header CON3) while IC1 is still connected to MOD1.

MOD1 is also connected to 5V power (VCC) and GND, plus the slave select (SS) and reset ($\overline{RST}$) pins, which go to digital I/Os PC4 and PD4 on IC1 respectively.

Its two output signals are fed to the HPF and switch S4, while the square wave output goes to CON4, although the signal which appears there is of limited use, as its duty cycle varies with frequency.

With switch S4 in the position shown, the lower frequency (100kHz-50MHz) signals pass through S4a, the 100nF coupling capacitor and S4b directly on to the buffer amplifier (the base of transistor Q3).

For higher frequency signals, S4 is moved to the alternative position where the buffer amplifier is fed from the output of the HPF, which receives its input from the unfiltered DDS output pin.

The HPF is a standard seven-pole Chebyshev filter. Elliptical filters provide a faster pass-to-stop band cut-off, but the resulting spurious and harmonic rejection is less effective compared with the Chebyshev type.

The filter was optimised to suit standard leaded components and home-made inductors.

For best performance, the coupling between the coils must be minimised. The PCB layout provides for small tin plate shields to be fitted between filter stages, a simple and effective solution.

The alternative HPF shown could potentially shift the 70-150MHz upper output range to 125-187.5MHz with appropriate software changes.

RF buffer amplifier

As noted earlier, the buffer amplifier is a robust discrete design, based on NPN transistor Q3. This is a well-known single transistor broadband arrangement providing about 15dB gain along with good dynamic range. Gain is necessary to provide the required maximum output level for the signal generator and to compensate for the insertion loss of the Serebriakova attenuator.

Alternative discrete buffers seen in other AD9850/51 based designs lack sufficient gain across the output range and/or frequently overload with the typically higher module output levels present below 10MHz.

By contrast, this buffer amplifier's gain is relatively flat and only reduces above 50MHz. This is acceptable given the application and circuit simplicity.

If you find the 2N4427 transistor difficult to source, you may be able to find a 2N3866 instead, although the gain may reduce by several decibels.

The output of the amplifier is taken from the centre tap of autotransformer T1 and coupled to the output attenuator by a 100nF capacitor.

The attenuator consists of four identical 0/20dB switched attenuators, followed by the aforementioned 0-20dB Serebriakova attenuator, giving an overall range of 0-100dB. This allows you to adjust the output from about -93dBm to +7dBm.

As mentioned earlier, this range is limited by shielding effectiveness and RF signal leakage across the attenuator sections.

Better shielding between sections is likely to allow another 20dB fixed attenuator to be added, significantly improving its utility for small signal work. Further improvements would likely require considerable additional design efforts around the power supply and control sections.

User interface

IC1 updates the 16x2 LCD using a typical 4-bit interface. The lower four bits of PORTC on IC1 (pins 23-26) drive the four upper LCD data pins, while pins 12 and 13 (digital outputs PD6 & PD7) drive the RS and EN control lines of the LCD.

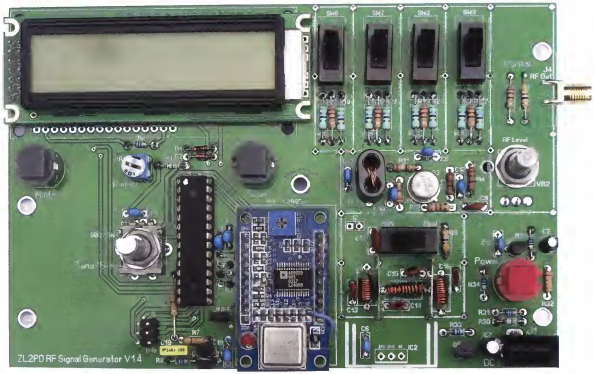
The backlight brightness is fixed using a 1kΩ resistor, with the backlight powered whenever the device is on, and trimpot VR1 provides contrast adjustment.

The Grey code pulses from the rotary encoder are sensed using IC1's PD2 and PD3 digital inputs (pins 4 & 5), while presses of the encoder's integral pushbutton and the SCAN and MODE pushbuttons (S1 & S2) are sensed using digital inputs PD0 and PD1 (pins 2 and 3).

These have internal pull-ups enabled so that they are held high when no buttons are being pressed.

As mentioned earlier, diodes D1 and

To whet you appetites for part 2, the construction details (scheduled for our July issue) here is the author's completed prototype PCB. As you can see, despite its complexity and performance, there really isn't all that much to building it!



D2 have been added to allow presses of three buttons to be sensed using the two available pins.

Jumper JP1 and ICSP header CON3 have been provided to allow IC1 to be re-programmed in situ. Removing JP1 prevents the programmer from trying to power the RF circuitry. CON3 has the standard Atmel 6-pin programmer pinout.

Power switching

The external power supply, nominally 12V DC, directly powers the output buffer. The buffer can operate down to 9V although harmonic distortion at full output increases by about 6dB at 9V compared to 12V.

The 12V supply is also regulated down to 5V by REG1 for the AD9850 module and the ATmega328 processor. Since the AD9850 module is current-hungry, REG1 requires a heatsink.

Dissipation losses would be reduced by using a switchmode regulator but this can introduce switching noise inside the signal generator, and could potentially modulate the output buffer output signal.

As it turns out, the metal signal generator case forms an effective heatsink for REG1, and this avoids the need for additional hardware.

The signal generator will continue to operate with a supply voltage down to 6V; however, its performance degrades significantly below 9V. By 6V, the maximum output falls by 10dB and harmonics are only suppressed by 10dB due to the reduced dynamic range in the buffer stage.

So, operation at 6V is possible but not recommended.

A 'soft switch' circuit has been added to allow the use of a momentary pushbutton (S3) as a power switch.

The circuitry to provide this function is shown at the upper right of Fig.4. It was initially described by Zetex in their February 1996 Design Note 27, for use as a relay driver.

However, several problems were encountered with that design, including some curious component choices and overheating. A minor redesign and the use of a higher-gain switching transistor solved them all.

When the supply is initially connected, the voltage appears on the emitter of Q4 and the 1µF capacitor charges via the three series resistors (2.7kΩ, 1kΩ and 270kΩ). However, Q4 cannot turn on until momentary switch S3 is pressed and no current is drawn from the supply.

When S3 is pressed, current is supplied to the base of Q5, which switches it on, and it in turn sinks current from the base of PNP transistor Q4, switching it on also and bringing up its collector voltage.

Current can then flow from Q4's collector to Q5's base via the two 1kΩ series resistors, so Q5 remains on and so does Q4.

However, the 1µF capacitor discharges because Q5's collector is now being pulled low, to 0V. So if S3 is pressed again, Q5's base goes low, switching it off, and in turn switching off Q4, so the circuit is back in the initial off-state.

References

1. **Gary McClellan, Programma-II synthesised signal generator**, *Radio-Electronics* magazine, Aug & Sept 1981 (300kHz to 30MHz CW/AM signal generator, 10kHz tuning steps, 10-300mV output)
2. **G. Baars, PE1GIC, DDS RF Signal Generator**, *Elektor*, October 2003 (50Hz to 70MHz, CW/AM/FM, 1Hz to 1MHz tuning steps, 0 to -127dBm out)
3. **Ian Pogson, Solid state modulated RF test oscillator**, *Electronics Australia*, May 1979 (455kHz to 30MHz in four ranges, approximately 100mV output)
4. **http://lea.hamradio.si/~s53mv/dds/theory.html**
5. **www.picmicrolab.com/ad9850-pic16f-interface-parallel-data-load/**

Part Two, next month

Next month's article will have the parts list, details of PCB assembly, case construction, programming IC1 and how to use the RF Signal Generator. We'll also have performance data, including spectrum plots. SC