ROBERT G. BROWN

BUILD A HIGH-PERFORMANCE LOGIC ANALYZER

Turn any computer into a high-speed, high-performance, expandable logic analyzer that can grab samples at up to 40 million per second!

One of the most useful tools for anyone working with digital electronics is a logic analyzer. Of course, a logic analyzer is also very expensive. There have been several designs for personal-computer-based logic analyzers that connect directly to the computer's printer port. While those devices are very useful and low in cost, they suffer from a fairly low sampling rate and a limited number of channels that can be sampled.

The PC-based logic analyzer presented here, although a bit more expensive then those other units, has most of the features of the even more expensive commercial units. It features a 40-MHz maximum sampling rate with ten clock-speed selections—eight that are internal and range from 40 MHz to 312.5 kHz, and two external inputs. A total of 16 channels can be sampled simultaneously. The triggering is controlled by an 8-bit trigger word that includes high-level triggering, low-level triggering, and "don't care" states for each channel. A total of three triggering modes are provided. The sampled data is stored in a 2048-word memory buffer that is transferred to the PC after the sampling is completed.

In addition to those basic features, the logic analyzer is designed to be expandable. Other features and devices can be plugged into the logic analyzer for uses that a logic analyzer can not be used for by itself. For example, a future article will describe how to build an expansion module that will turn the logic analyzer into a full-featured digital-storage oscilloscope!

Theory of Operation. In general, a logic analyzer works by taking a sample of a set of digital signals at set time intervals after a certain triggering condition appears on the inputs. When the analyzer is triggered, the samples are read and stored for later viewing. The analyzer board has five main functional blocks: the PC interface, clock generation, data storage, trigger control, and 5-volt power supply. The schematic diagrams in Figs. 1 and 2 show how the circuit is put together. In order to keep the PC Board size down, the circuit is designed around two programmable-logic devices. A Lattice Semiconductor ispLSI1016E Complex PLD (or CPLD) is used for IC1. The ispLSI1016E holds a lot of digital logic within its 44-pin PLCC package. The particular programming that is used in the logic analyzer design is equivalent to about a dozen standard TTL chips. An additional PLD is used for IC2. That chip replaces about 4 standard TTL chip's worth of logic. Those two PLDs handle most of the logic on the analyzer board. Since much of the logic is contained in IC1, it plays a part in most of the different functional blocks.

The PC interface connects to any standard printer port through J1; a bi-directional port is not needed. All 12 output signals (8 data lines and 4 control signals) on the port are used by the analyzer. Four of the five possible inputs to the PC are used to read data and status information from the analyzer circuit. Each signal is terminated using a resistor-capacitor pair to make sure that the signal does not become garbled in any way. The signals that are edge sensitive are further buffered by IC9, a 74HCT14 hex inverter. The 74HCT14 is a Schmitt-trigger device that has "hysteresis" on the inputs. That causes the outputs to "snap" on or off even if the inputs rise or fall slowly. That action cleans up any poor-quality signals.

The software running on the PC passes information to and from the logic-analyzer board using a simple addressing method. Three address

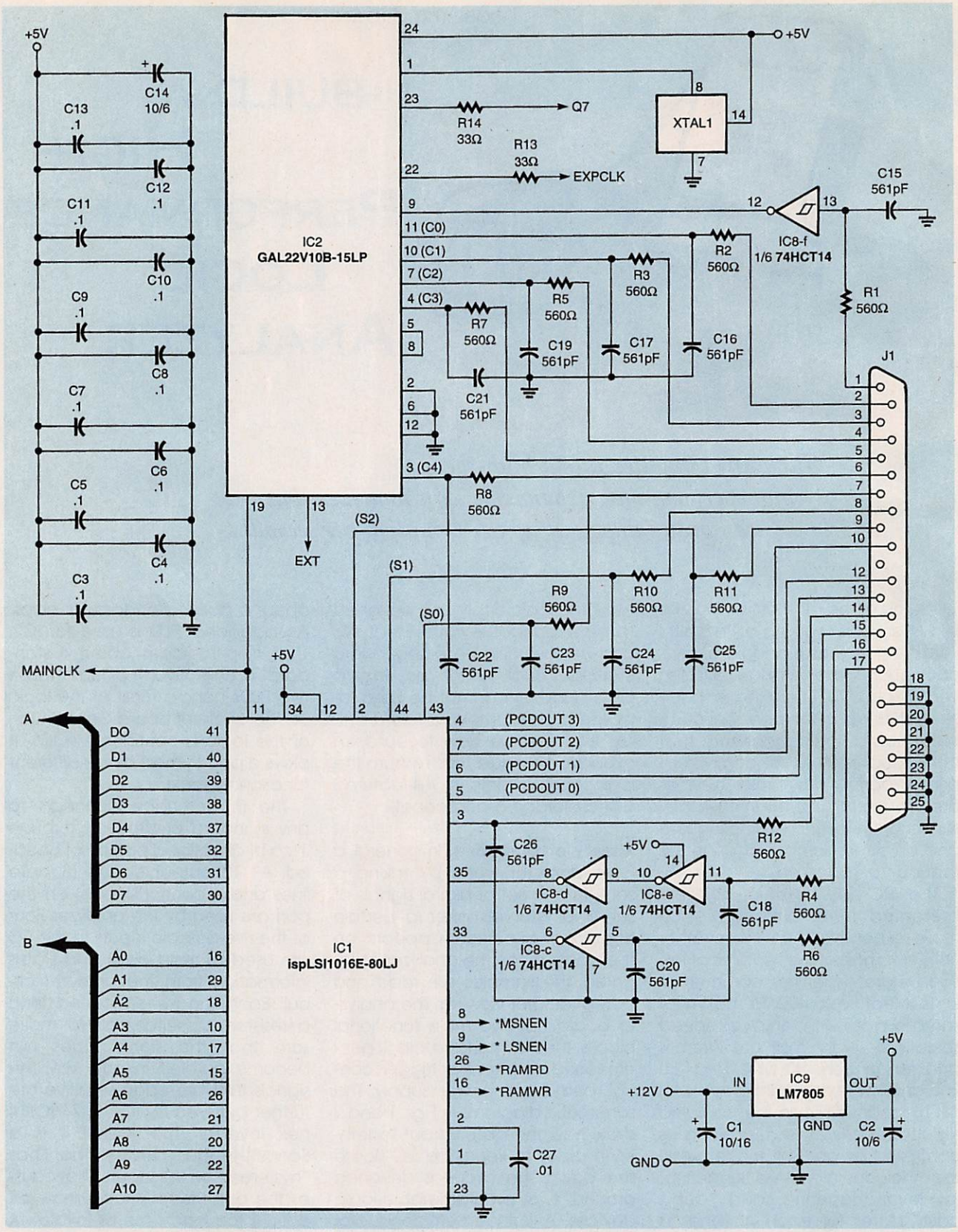


Fig. 1. The circuitry of the Alta Engineering Logic Analyzer is simplified by the use of programmable-logic devices (PLDs) that can replace a dozen or more individual integrated circuits.

signals are used to select one of eight address locations on the analyzer board. Once the address is set, the PC can read information from the signals PCDOUT0, PCDOUT1, PCDOUT2, and PCDOUT3 through the printer control register. Table 1 shows the different addresses and the information that is

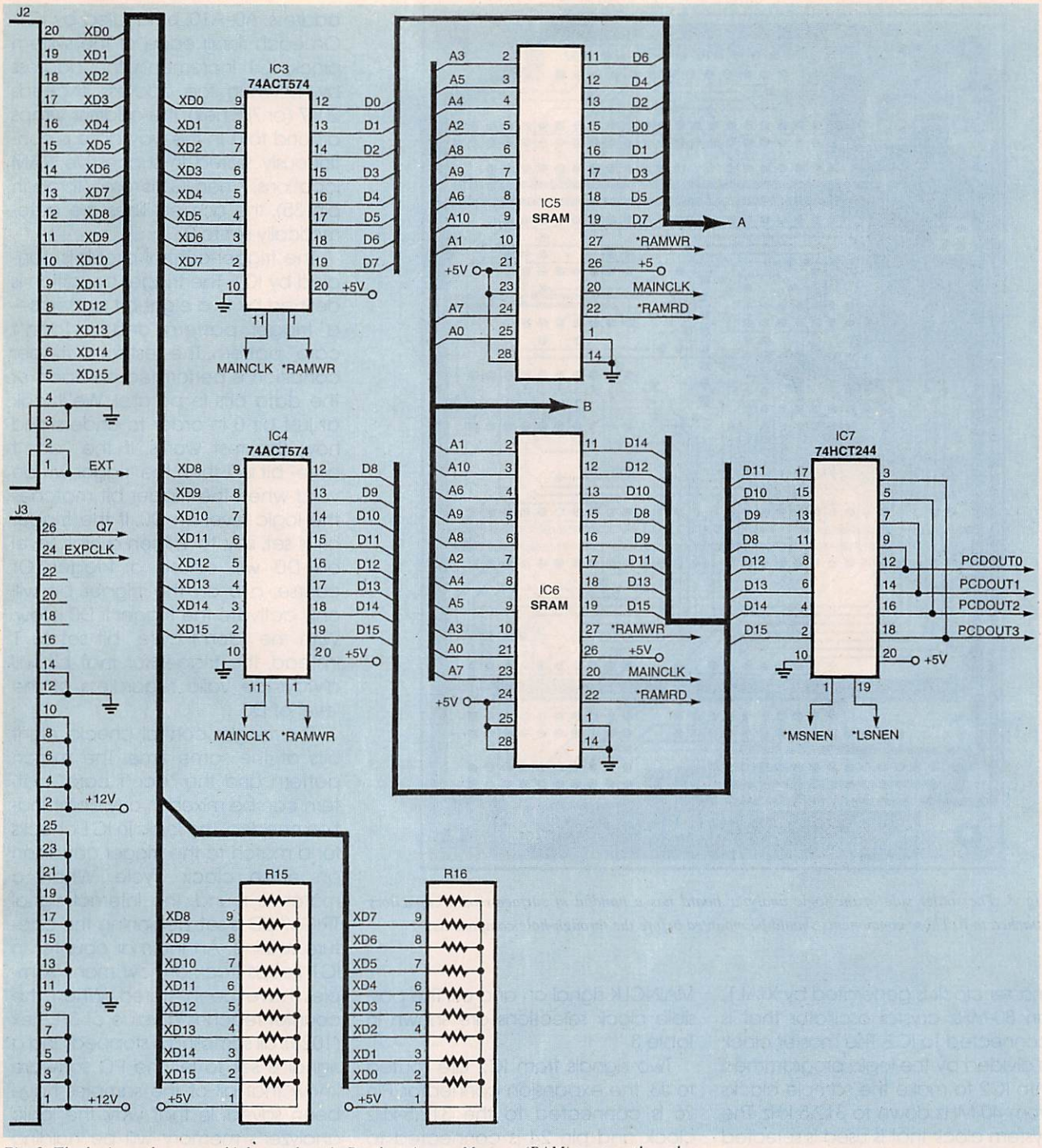


Fig. 2. The logic analyzer uses high-speed static Random-Access Memory (RAM) to store the collected samples at rates up to 40 MHz.

passed to the computer.

The signals D0–D7 and A0–A10 are the same signals indicated in Figs. 1 and 2. Those signals are routed through IC1. The T7, STOP, TRIGVALID, and WRAP signals are generated by IC1 itself. Signals D8-D15 are routed through IC7. The signals *LSNEN and *MSNEN are generated by IC1 to control the transfer of data through IC7.

For the PC to write data to the logic analyzer requires only a slightly more complex procedure. Again, the control signals S0–S2 are used to select the address according to Table 2. Once the address has been selected, the data is transferred serially one bit at a time. Each bit from the PC is placed on pin 3 of IC1. The transfer takes place on the rising edge of the clock signal on pin 33 of IC1. For example, the trigger data (T7–T0 and X7–X0) is loaded into IC1 by placing the value for T7 on pin 3 of IC1, and then toggling the clock line on pin 33. That procedure is repeated for T6, T5, *etc.* to T0, then X7, X6, and so on until X0 has been transferred.

One of the key parts of the logic analyzer circuit is the clock generator for timing the sample interval. The

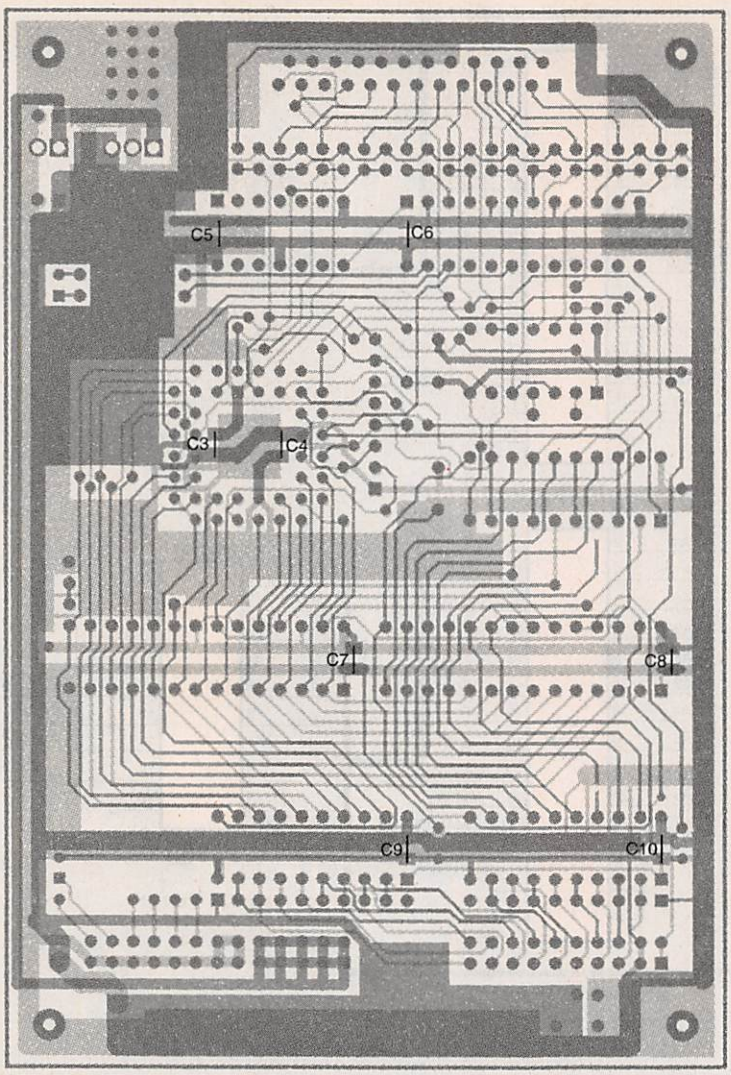


Fig. 3. The solder side of the logic analyzer board has a handful of surface-mount capacitors attached to it. Those components should be mounted before the through-hole components.

master clock is generated by XTAL1, an 80-MHz crystal oscillator that is connected to IC2. The master clock is divided by the logic programmed into IC2 to make the sample clocks from 40 MHz down to 312.5 kHz. The system clock that is used is selected by the signals C0–C4, which come from the PC. In addition to the internally-generated clock frequencies, the EXT signal can be a clock from an external source—usually from the system under test. An additional clock input from the PC to pin 9 of IC2 lets the software control the clock for retrieving data, control, and diagnostic functions. Regardless of the clock division selected by C0–C4, whenever the signal on pin 9 of IC2 is low, the MAINCLK signal is held low. That lets the PC turn the MAINCLK signal on and off. The possible clock selections are shown in Table 3.

Two signals from IC2 are routed to J3, the expansion connector. Pin 26 is connected to the 312.5-kHz clock and pin 24 is connected to the MAINCLK signal. Neither of those signals are used within the logic analyzer circuit, but will be used by future expansion modules.

During data capture, the outputs of IC3 and IC4 are enabled and data is strobed into the flip-flops from the probe assembly on the rising edge of the system clock. The system clock is also connected to the chip-select inputs of static RAMs IC5 and IC6. The captured data is written to the RAMs on the low half of the system clock cycle. The RAM address, A0–A10, is handled by IC1. On each rising edge of the system clock, IC1 increments the address by 1. When the address exceeds 2047 (or 7FF hex), the address wraps around to 0. In this way, data is continuously stored in successive RAM locations. When IC1 is reset (through pin 35), the address lines are automatically set to 0.

The trigger-control circuit is handled by IC1. The trigger condition is defined by two eight-bit patterns—a trigger pattern and a "don't care" pattern. The test for a trigger condition is performed on each of the data bits in parallel. We'll look at just bit 0 in order to understand how the test works. If the "don't care" bit is 0, then the trigger will be valid when the trigger bit matches the logic level on D0. If the trigger bit is set, say, to 1, then a high level on D0 will cause a trigger. Of course, a 0 on the trigger bit will only activate the trigger if D0 is low. With the "don't care" bit set to 1 instead, the trigger for that bit will always be valid regardless of the level of D0.

The trigger control checks eight bits at the same time. The match pattern and the "don't care" pattern can be mixed in any combination needed. The logic in IC1 checks for a match to the trigger condition on each clock cycle. When a match is found, the internal signal TRIGVALID is set, beginning the capture routine. An internal counter in IC1 keeps track of how many samples have been stored. When the counter reaches a value of 3FF hex (1023), all sampling is stopped and a signal is set to let the PC software know that all of the samples have been saved. In that way, the logic analyzer's memory will be holding 1024 samples before the trigger condition was met and 1024 samples after the circuit was triggered.

Once the data acquisition has stopped, the stored data must then be read from the logic analyzer to the PC. The PC reads the last address from the logic analyzer 4 bits at a time through the interface. The PC then resets IC1 and selects the PC-controlled clock on IC2. The RAMWR signal is cleared, which disables the outputs on IC3 and IC4, and puts the RAM ICs into the read

PARTS LIST FOR THE ALTA ENGINEERING LOGIC ANALYZER

SEMICONDUCTORS

IC1—ispLSI1016E-80LJ programmable-logic device, integrated circuit (Lattice Semiconductor)
IC2—GAL22V10B-15LP programmable-logic device, integrated circuit
IC3, IC4—74ACT574 octal flip-flop, integrated circuit
IC5, IC6—8K×8 static RAM, 12 nanosecond, integrated circuit
IC7—74HCT244 octal buffer, integrated circuit
IC8—74HCT14 hex Schmitt trigger, integrated circuit
IC9—LM7805 5-volt regulator, integrated circuit

RESISTORS

(All resistors are ¼-watt, 5% units unless otherwise noted)
R1–R12—560-ohm
R13, R14—33-ohm
R15, R16—1-megohm, 10-pin single-inline package, resistor network

CAPACITORS

C1—10-µF, 15-WVDC, electrolytic
C2, C14—10-µF, 6-WVDC, tantalum
C3–C10—0.1-µF, ceramic, surface-mount
C11–C13—0.1-µF, ceramic-disk
C15–C26—561-pF, ceramic-disk
C27—0.01-µF, ceramic-disk

ADDITIONAL PARTS AND MATERIALS

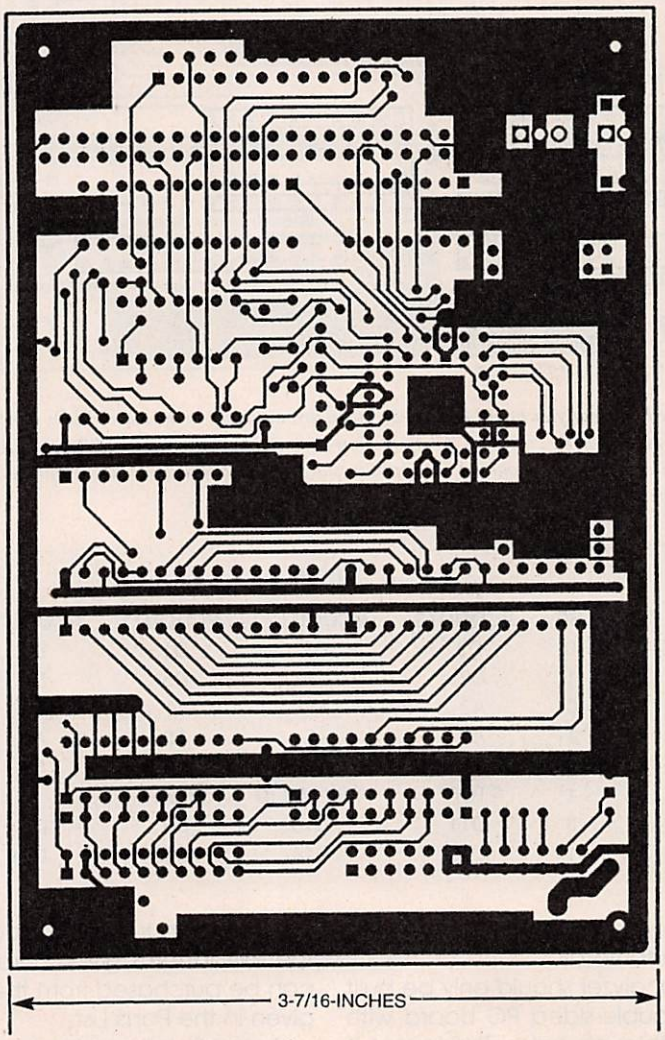
J1—DB25 female connector, PC-mount
J2—20-pin male header
J3—26-pin male header
J4—coaxial power jack
XTAL1—80-MHz oscillator
Heat sink for IC9, socket for IC1, 12-volt wall transformer, 20-conductor ribbon cable, 20-pin insulation-displacement connector, test clips, DB25 male-to-male cable, PC board, wire, solder, hardware, case, etc.

Note: The following items are available from: Alta Engineering, 58 Cedar Lane, New Hartford, CT 06057-2905; Tel: (860)489-8003; e-mail: alta@gutbang.com; Web: www.gutbang.com/alta: Software on 3½-inch diskette, $10.00; Blank PC board, $45.00; Complete board-only kit with software, $139.00; Complete board-only kit with case and software, $169.00; Complete kit with power supply, probe kit, and cable, $209.00. Please include $5.00 for shipping and handling within the US; $10.00 (US) for international orders. CT resi-dents should add appropriate sales tax.

mode. The data is then read 4 bits at a time from each address starting at 0. After the data at a given address is read, the PC pulses the diagnostic/control clock on IC2 in order to increment the address counter to the next location. Once all of the data has been read from all of the RAM addresses, the PC program can then display the data.

The final section is the power supply. A 12-volt DC wall transformer rated at 800 mA provides power for the unit. The logic analyzer uses about 450 mA of regulated 5-volt current. That is supplied by IC9, a 7805 regulator. A heat sink is needed on IC9 to prevent overheating of the device. The expansion connector also has connections for the unregulated 12-volt supply so that other expansion modules can be powered by the wall transformer.

Building the Logic Analyzer. Before building the logic analyzer, get a copy of the software from the Alta Engineering web site (www.gutbang.com/alta) or the **Electronics Now** ftp site (ftp://ftp.gernsback.com/pub/EN/altalog.zip). You will need the software for both programming the PLDs and testing the analyzer. The program also doubles as a demo so you can see the capabilities of the unit before actually building it. Also, any last-minute suggestions or details that do not



Here is the component side of the logic analyzer board. If you will be making your own board and you will not be plating the holes, you will have to solder the connections on both sides of the board.

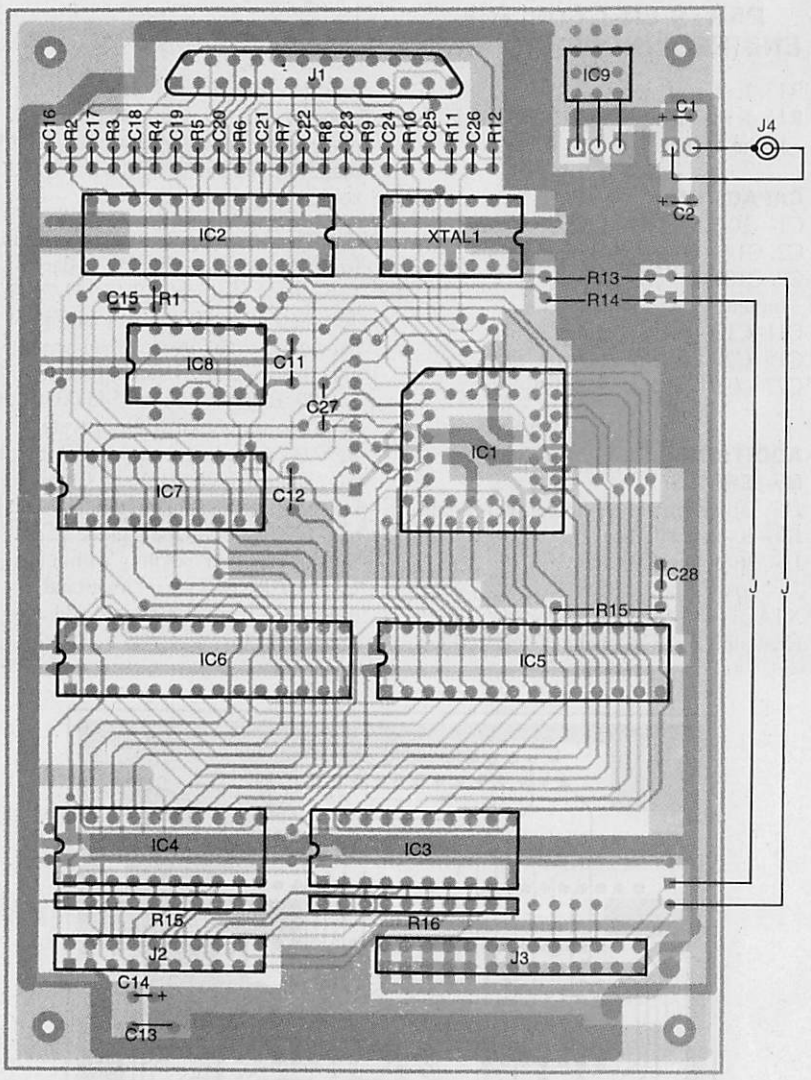


Fig. 4. The logic analyzer board has a neat, clean layout thanks to the use of PLDs to keep package count to a minimum. Be careful of IC orientation—some of the parts face in different directions. The jumper wires should be mounted on opposite sides of the board in order to minimize crosstalk between the signals they will be carrying.

Table 1

S2	S1	S0	PCDOUT3	PCDOUT2	PCDOUT1	PCDOUT0
0	0	0	D3	D2	D1	D0
0	0	1	D7	D6	D5	D4
0	1	0	A3	A2	A1	A0
0	1	1	A7	A6	A5	A4
1	0	0	T7	A10	A9	A8
1	0	1	STOP	TRIGVALID	WRAP	
1	1	0	D11	D10	D9	D8
1	1	1	D15	D14	D13	D11

make it into print will be included with the software.

The analyzer should only be built on a double-sided PC board with plated-through holes. The layout is very critical, so no other construction method is likely to work. You can make your own PC board from the foil patterns given here, or one can be purchased from the source given in the Parts List.

A small, low-wattage soldering iron should be used to assemble the board. Start by soldering the surface-mount capacitors onto the bottom of the board. The locations of those components are shown in Fig. 3. A simple method of soldering those parts is to first coat one of the pads with some solder. While holding the component in place with a small screwdriver, touch the same pad lightly with the soldering iron. The solder will re-melt and tack the capacitor in place. Carefully check the position of the capacitor to be sure it is properly seated on the pads. Now is the time to fix any alignment errors. If the part is properly aligned, solder the other end of the capacitor in place. Finally, go back to the first end and re-flow that solder joint. After each capacitor is soldered in place, use an ohmmeter to check between the 5-volt and ground traces to verify that it remains an open circuit. Checking for shorts each time will help catch and correct any errors. The rest of the remaining capacitors and the resistors can now be mounted using the parts-placement diagram in Fig. 4 as a guide. Most of the resistors must be mounted vertically to fit into the available space.

Before mounting IC9, slide the heat sink onto the regulator. Make a 90-degree bend in the leads at the point where they taper down. Mount the regulator so that the heat sink hangs over the end of the PC board. Once IC9 is soldered in place, connect a short pair of insulated wires and J4. Feed the wires through a rubber grommet if the unit will be mounted in a case. Before mounting any semiconductors, hook up the transformer and verify that 5 volts is present between the power and ground pins at each IC location.

The remainder of the parts can now be mounted. Although sockets are optional for the integrated circuits, a socket must be used for IC1. Be very careful about the location of pin 1 on all of the ICs—some components face in different directions on the board. The two jumpers should be installed on opposite sides of the PC board in order to reduce crosstalk between the signals that they will carry.

The Probe Assembly. While you can purchase the probe assembly

Table 2

S2	S1	S0	Function
X	0	0	Trigger data T7-T0 then X7-X0
X	0	1	Not Used
X	1	0	Trigger sequence/ length/mode

parts from the source given in the Parts List, it is a good idea to make your own probe assembly. That way, the assembly can be customized to your own requirements. Start by mounting a length of 20-conductor ribbon cable to an insulation-displacement connector. The cable should not be more then 18 inches in length; keeping the length as short as possible is better for both signal integrity and keeping the cables from getting tangled. If you are not sure what length you will be needing, 12 inches is a good starting point. A total of 18 clips will be needed—one for each data input, plus one for ground and one for the external clock signal. There are many choices for the clips—the ideal choice depends on the type of circuits that you will be testing. Several different probe assemblies with different lengths and probes can be made for different needs.

Following the diagram in Fig. 5, solder the clips to the ribbon cable. Split conductors 1 and 2 off from the rest of the cable. Solder both conductors 1 and 2 onto a clip and label that clip "CLOCK". Next, split wires 3 and 4 off and solder both of them onto a clip—that will be labeled "GROUND." Starting from conductor 20, separate each wire from the cable and solder it onto a clip. The labels will go from "0" to "15" (conductor 20 is labeled "0"). The cable should be split most of the way down the connector. If it is not split, the result will be crosstalk between the adjacent wires. Of course, the wires might become a tangled mess with use—just like an expensive analyzer. Unfortunately, there doesn't seem to be a good way to keep the probe wires neat without bundling them together and getting crosstalk.

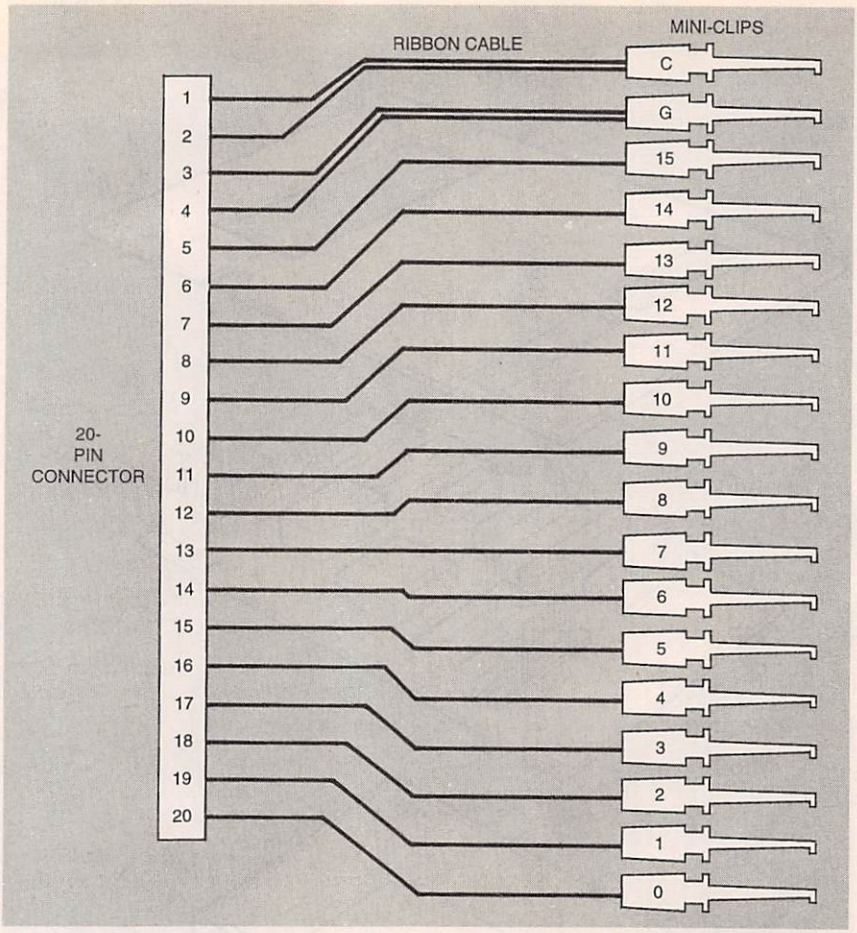


Fig. 5. The probe assembly is easily made from a length of ribbon cable and a handful of test clips. Note that two of the clips have two wires each attached to them.

Table 3

C4	C3	C2	C1	C0	MAINCLK
0	0	0	0	0	40 MHz
0	0	0	0	1	20 MHz
0	0	0	1	0	10 MHz
0	0	0	1	1	5 MHz
0	0	1	0	0	2.5 MHz
0	0	1	0	1	1.25 MHz
0	0	1	1	0	0.625 MHz
0	0	1	1	1	0.3125 MHz
0	1	0	0	0	EXT clock
1	0	0	0	0	EXT clock inverted
1	1	0	0	0	Software clock

Testing the Logic Analyzer. Double-check all of the solder joints and connections one more time. When you are completely sure about your work, plug in the power supply. Using a voltmeter, check to see that there is 12 volts at the expansion connector and that there is 5 volts between each IC's ground and power pins. Disconnect the power from the board. Connect the board to a printer port on a PC using a DB25 male-to-male cable with all conductors wired straight through (pins 1 to 1, 2 to 2, etc.). The cable should be 6 feet or less in length. Since there is a possibility that a defective logic analyzer could damage the printer port circuitry in the computer, you should not use a laptop computer with the analyzer until the analyzer has been given a clean bill of health. Start the computer and apply power to the analyzer board. Run the ALTALOG program. Select F9 to configure the program. Select the LPT port that the analyzer is connected to and then press any key at the prompt. The LPT port selection is stored in the config-

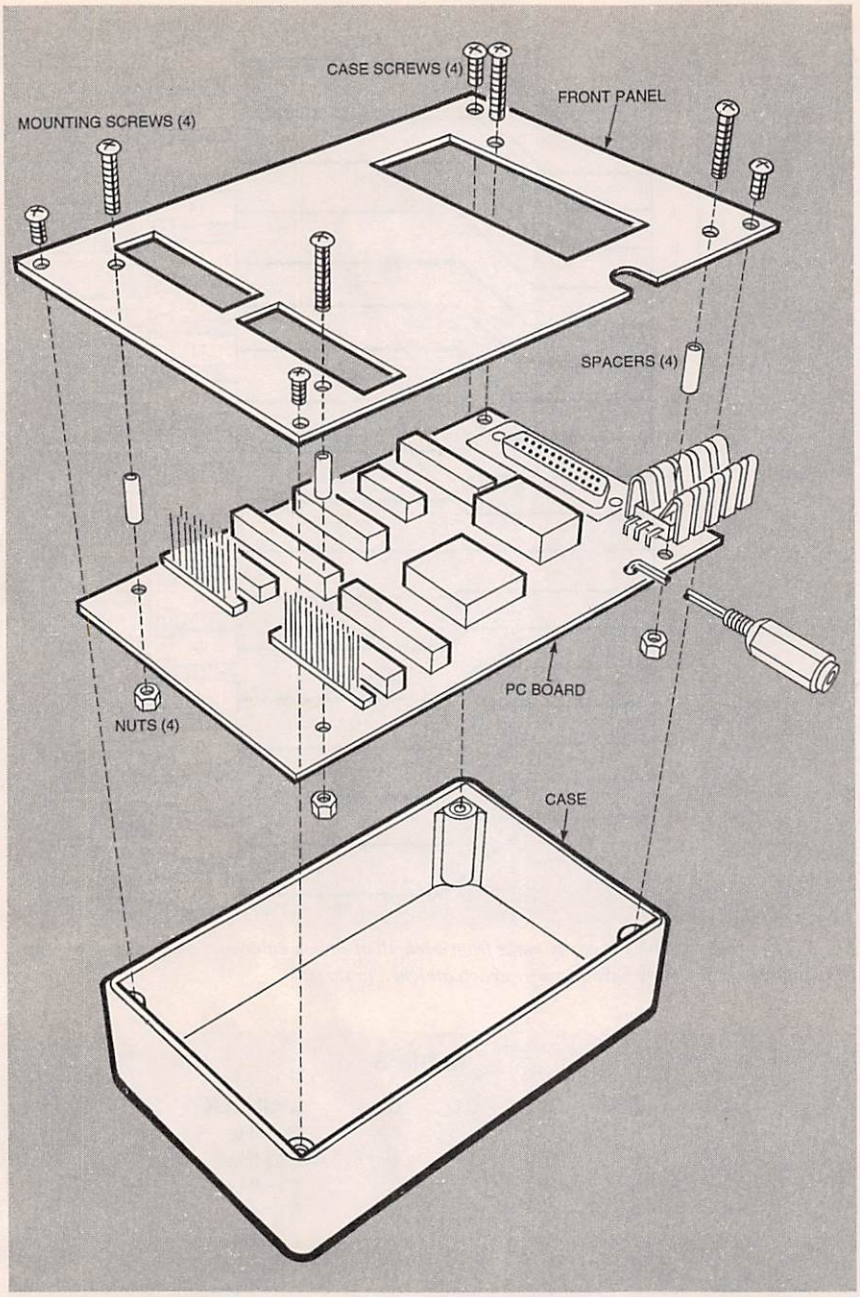


Fig. 6. Mounting the logic analyzer board in a suitable enclosure is very simple and straightforward. Don't forget to use a rubber grommet on the power leads if you are using a case with a metal front panel.

uration file ALTALOG.CFG.

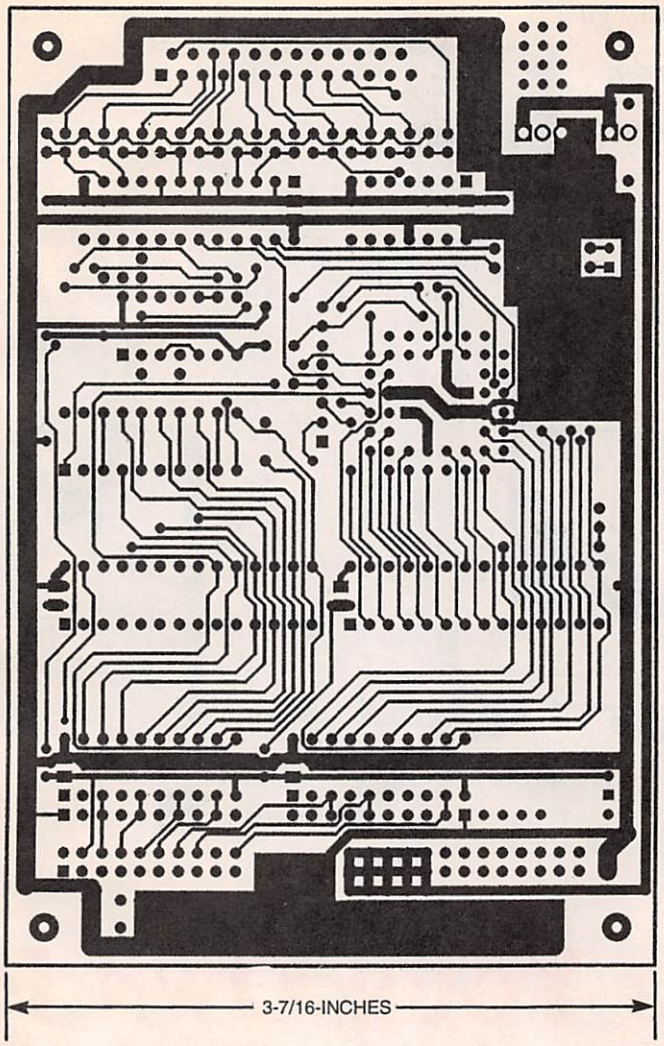
The logic analyzer will be tested by using it on its own signals. Connect probe 0 to pin 26 on the expansion connector, and connect probe 1 to expansion connector pin 25. Those pins are toward the outside edge of the board. Do *not* connect the probe to the expansion-connector pins on the inside of the board—those pins carry 12 volts and will damage IC3 and IC4. Press F5 on the computer keyboard to acquire data. In a few seconds, acquiring the data should be complete and the menu will return. Press F6 to look at the state display of the data. The data is shown in binary toward the right side of the screen. Bit 1 (second from the right) should read 0 all the way up and down the page. Bit 0 (all the way on the right) should alternate between 64 zeros and 64 ones. Use the PageUp and PageDown keys to scan through the data and verify that the data has been captured correctly. If that is correct, most of the logic analyzer is working. Additional testing will be done while learning how to use the analyzer. If you run into problems, you might have a cable problem, the wrong LPT port selected, or a board problem. The diagnostic program ALTADIAG that is described in the text file ALTADIAG.TXT will do some additional board troubleshooting. All of those files are included in the main file archive that was downloaded.

Once the logic analyzer passes its initial tests, the board can be mounted in a suitable enclosure. A method is shown in Fig. 6. Suitable holes are cut in the front panel for the three connectors and the power lead. The board is simply bolted to the back of the front panel using screws, nuts, and spacers. Any kind of labeling on the front panel to help identify the various pins and functions will help make the project more professional-looking.

Using The Logic Analyzer. There are a few non-obvious points that you should be aware of when using the logic analyzer. Always power up the logic analyzer before connecting the probes to the circuit under test. Hooking up a powered circuit when the logic analyzer is turned off can overheat and possibly damage IC3 and IC4. Another very important point is to make sure that there is no AC potential between the grounds of the circuit and the logic analyzer.

Like the initial test, we're going to use the analyzer on itself. Start the ALTALOG program and wait for the main menu to appear. As before, connect probe 0 to expansion connector pin 26 and probe 1 to expansion connector pin 25. This time, connect probe 2 to expansion connector pin 23 and probe 3 to expansion connector pin 21. We will not be needing the "ground" or "clock" probes.

Using menu choice F1, set the "A," or main, trigger to be XXXX XXX1, meaning that we want to trigger when probe 0 is high and we don't care about the state of the other bits. Press F2 to set up a "B" trigger condition and enter XXXX XXX0. With two different trigger conditions set, select the trigger mode with F3. The choices are



The solder side of the logic analyzer board has special pads for the surface-mount capacitors.

using the "A" trigger for one clock, the "A" trigger for two clocks, or the "A" trigger followed by the "B" trigger. For now, select the first option ("A" for one clock). We'll choose a 5-MHz clock rate with F4. Press F5 to start collecting data. Within a few seconds, the collection will be complete, and the program will return to the main menu.

Select F6 to view the data just gathered. For each clock cycle, the state display shows the clock-cycle number relative to the trigger point. The trigger point is clock-cycle zero; negative numbers are clock cycles before the trigger, and positive numbers are the cycles after the trigger. The next number is the time in microseconds relative to the trigger. The actual data is displayed two ways—first in hexadecimal and then in binary (remember, probe 15 is the most-significant bit, probe 0 the least). At the trigger point, we should see 0 0.000 XXX1 xxxx xxxx xxxx 0001 (the x is used to represent an unknown value because we did not connect probes 8–15). You can move forward or backward through the display by pressing various navigation keys on the keyboard. The Page Up and Page Down keys will move the display backward or forward one page at a time. The Home key will jump to the first data acquired and the End key will take the display to the last data acquired. The number 5 key on the numeric keypad (make sure that the number lock indicator on the keyboard is off) will bring you back to the trigger point.

A special feature of the software is search capabilities. By pressing the S key, the search menu will appear. Type in the data pattern you want to find. It is typed in the same way a trigger condition is set (1, 0, and X). After pressing the return key, select F for forward search or R for a reverse search. The program will search for data that matches the search pattern and display that location on the screen. Pattern searching is a very powerful feature because of the large amount of data in 2048 samples.

Press ESC to exit the state display. The timing display is entered by pressing F7. That display mode requires a CGA or better graphics card and monitor on the computer. The data will be displayed in timing-diagram format. A cursor is at the trigger point, and the state information from the cursor position is displayed at the top of the screen. The ESC, Page Up, Page Down, Home, End, numeric 5 key, and the search option work the same way as with the state display. In addition, the left and right arrow keys can move the cursor back and forth through the data to display the state information for any point. The data and setup information (trigger patterns, clock rate, etc.) can be stored and recalled by pressing F8. That will let you save any collected data and view it at another time.

In the sample we just took, the timing display should show that bits 1, 2, and 3 are always at logic zero. Bit 0 should alternate between 0 and 1 every 16 samples, which works out to 3.2 microseconds. At time 0 (the trigger point), bit 0 should be a logic one, which is what we assigned as the trigger. Using F3, change the trigger mode to be "A" then "B". Select a 10-MHz clock rate using F4. Use F5 to start a new data acquisition. When the new data samples are done, look at the timing display. It should show that bit 0 is now a logic zero at time 0. Bit 0 should be a logic one for 3.2 microseconds just before time 0. Since we doubled the sampling rate, 3.2 microseconds is 32 samples. With the trigger condition set to "A" followed by "B," the "A" trigger condition had to be met first, in which bit 0 is a 1. Once the first condition is met, the B trigger condition

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had to be met (with bit 0 at 0).

Experiment with the differen clock rates, trigger modes, and trig ger values. Also be sure to use all o the probes on signal Q7 in order t verify that all of the channels o the analyzer are working. One finc note concerning the "A" then "B trigger mode: only the lower 4 bit (0-3) of each trigger value ar valid. Once you have tried all th options, you are ready to use th logic analyzer on other circuits.

A logic analyzer is a very valu able tool for working with digit logic. It can be used to verify timin relationships or for troubleshootin digital logic. The author welcome any questions, comments, or sug gestions on this project. He can b contacted by e-mail at alta@gu bang.com, by telephone at (860 489-8003, or by visiting the Alt Engineering Web site at www.gu bang.com/alta.