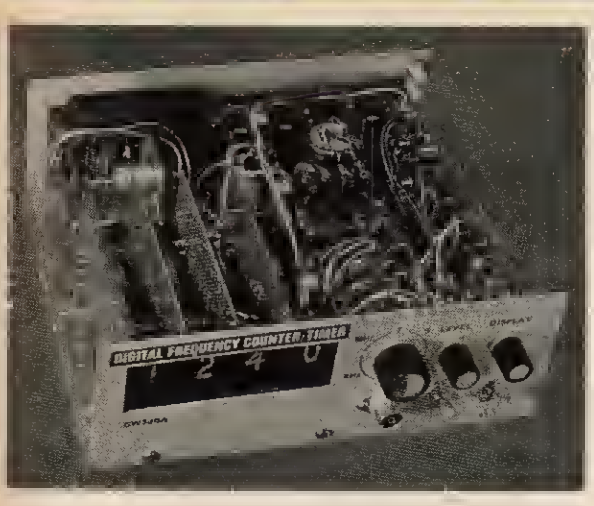
DIGITAL FREQUENCY COUNTER/TIMER



J. THORNTON-LAWRENCE GW3JGA

PART 4 *(continued from the November issue)*

Frequency measurement is the primary purpose of the instrument and although, on low and medium frequency signals of a reasonable amplitude, it is sufficient to connect the signal and read away, hetter results may he obtained particularly on the higher frequencies if the controls are set correctly.

It should be remembered that the purpose of the input clipping stage is to provide, from the input signal, a clean squarewave suitable for driving the signal gate and decade counters.

With the input switch in the "AC" position the input a.c. signal can be "slid up and down" the input characteristic of Tr1 by rotating the LEVEL control, so that symmetrical clipping takes place.

The smaller the input signal and the higher the input frequency the more important it is to set the LEVEL control correctly.

With the signal applied to the input and the function control set to a low frequency range, the LEVEL control should be carefully rotated from one end to the other and the range noted over which a steady reading is obtained. The correct setting is in the centre of this range (see Fig. 19).

The actual physical position of the control depends to a large extent on the individual characteristics of Tr1. (It may he possihle to suhstitute other types of f.e.t. in place of the 2N3823 hut the spread of characteristics may make the LEVEL control inoperative.)

It is assumed that normally the signal to be measured will be clean and free from hum and noise. However, if a large amount of hum (mains ripple) is present on the signal to he measured this may cause errors due to the clipper stage being saturated for periods of the hum waveform, as shown in Fig. 20.

A solution to this prohlem is to use a simple high pass filter, as shown, which will effectively remove the low frequencies whilst allowing the r.f. signal to pass through.

Assuming that the LEVEL control has heen set to its optimum position, the function switch should then he rotated to a position where the first digit of the displayed reading appears on tbe left hand tube.

Suppose that a signal of 7·054321MHz is being measured, the reading of frequency sbould be 7·054MHz. Setting the function switch to the highest frequency range will cause a reading of 07·05MHz to he displayed and ohviously the frequency is not heing measured as accurately as it can he.

Conversely, by moving the function switch the other way to a lower frequency range, the 7 disappears off to the left and a reading of 0543 is displayed.

This procedure may he repeated until in the Hz position the reading will be 4321, the right hand figure indicating cycles per second and the left hand figure indicating kHz.

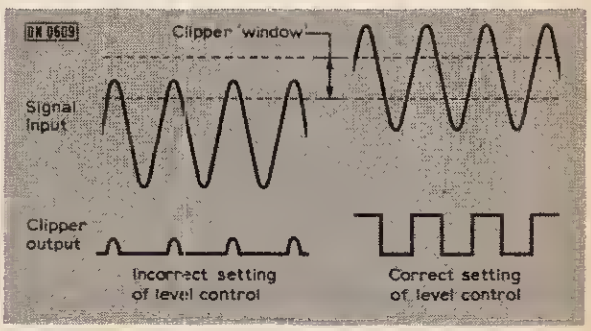


Fig. 19 : Waveforms showing correct and incorrect settings of the LEVEL control.

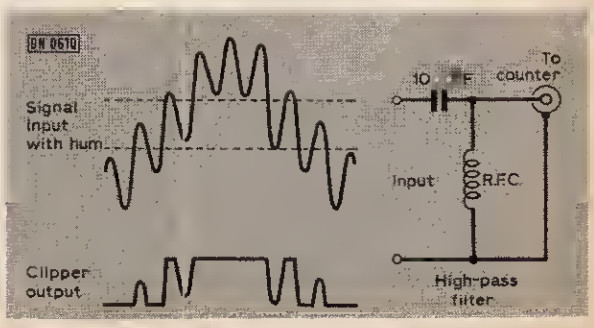


Fig. 20 : Effects of hum and noise on the input signal. A simple high pass filter is shown on the right.

This is a useful facility for measuring small changes in frequency, e.g. checking variable frequency oscillators, frequency modulation systems, and monitoring the frequency of a signal generator when aligning the i.f. stages of a receiver and checking crystal filters.

It is important to remember that whilst this measurement gives very high discrimination it is only a relative measurement of frequency and is not an absolute measurement to this accuracy. The stability of the internal crystal oscillator is insufficient for this to be so.

Calibration Outputs

The 100kHz, 10kHz and 1kHz outputs at the rear of the instrument may be used for calibrating receivers. This can be done by loosely coupling the appropriate output to the input of the receiver. A series coupling capacitor and resistor of about 1,000pF in series with 1kΩ should be used as each output is directly connected to the divider circuits and an accidental short to earth or worse still to a high voltage would upset the operation of the divider and may cause permanent damage.

Time and Period Measurement

The simplest time measurement for the instrument to make is in measuring the time of one cycle of a repetitive waveform. This is useful for frequencies below 100Hz as greater accuracy can be obtained.

On the time ranges of the instrument, the counting is initiated by the negative going part of a signal and stopped by the next negative going signal. The operation on various waveforms is shown in Fig. 21a, b and c.

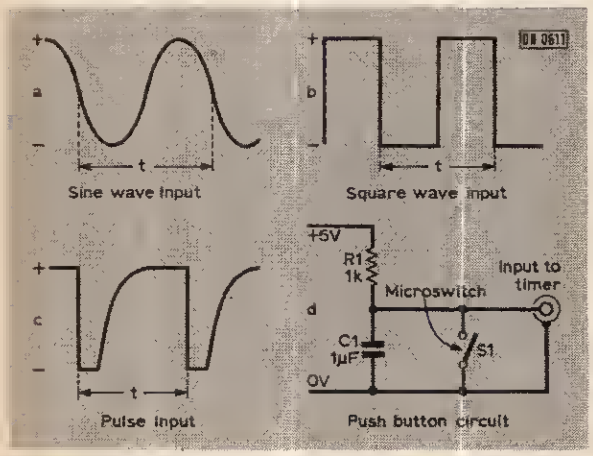


Fig. 21: Operation of various timing waveforms. Circuit on the right provides a fast negative going pulse when S1 is closed.

For the timing of events, as an electronic stop watch, it is necessary to provide a circuit which will generate a fast negative going pulse when a button is pressed. A suitable circuit is shown in Fig. 21d.

The 1μF capacitor C1 is normally charged to +5volts through R1. When the microswitch is pressed a sharp negative going voltage step is produced which starts the timer counting time. The switch is released and R1 recharges C1. When the switch is pressed for the second time the negative pulse stops the count and the total time between the two operations is displayed in mS or seconds depending on the setting of the function switch. The purpose of C1 is to prevent the contact bounce in S1 from causing false triggering of the instrument.

For automatic operation, two photocells may be used and a suitable circuit for timing the duration between two events is shown in Fig. 22.

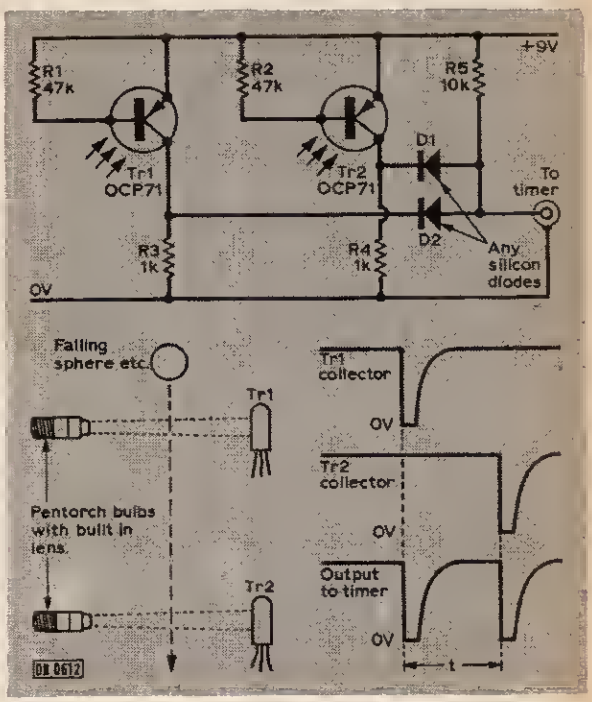


Fig. 22 : Circuit shown above is suitable for automatically timing the duration between two events.

An extension of this system with more powerful light sources may be used for race timing, horse trial events, etc.

In the above applications of start-stop pulses it is suggested that the input switch is set to the "AC" position and that the LEVEL control is adjusted to the position which gives reliable operation, this is usually slightly higher (clockwise) than the centre operating point used in frequency measurements.

Very Low Frequency Input Signals

For very low frequency signals where the input coupling capacitor may attenuate the signal severely the input switch may be used in the "DC" position. This may result in the LEVEL control having little or no effect. However, if the input signal has an amplitude of about 10 volts peak to peak about earth potential, reliable operation of the instrument should be obtained.

The integrated circuits used in the Digital Frequency Counter Timer are the 74 series of TTL (Transistor-Transistor Logic) in the 14 and 16 pin DIL (dual in line) package. The device operates from a supply of +5 volts (4·5V min., 5·5V max.).

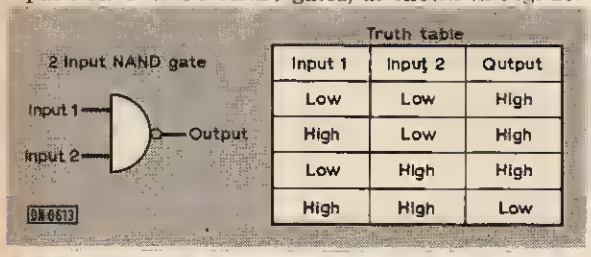
In the operation of the logic only two states are possihle, 0 and 1.

logic 0="low" =less than +0·8volts.

logic 1="high" =greater than +2·0volts.

7400N Quadruple 2 Input Nand Gate

This device contains four separate identical two input NAND (NOT AND) gates, as shown in Fig. 23.



Truth table

Input 1	Input 2	Output
Low	Low	High
High	Low	High
Low	High	High
High	High	Low

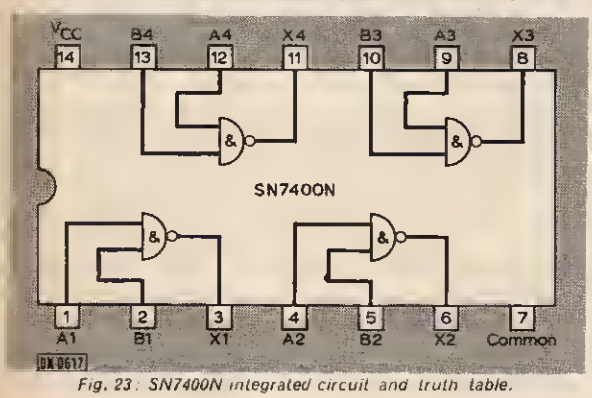
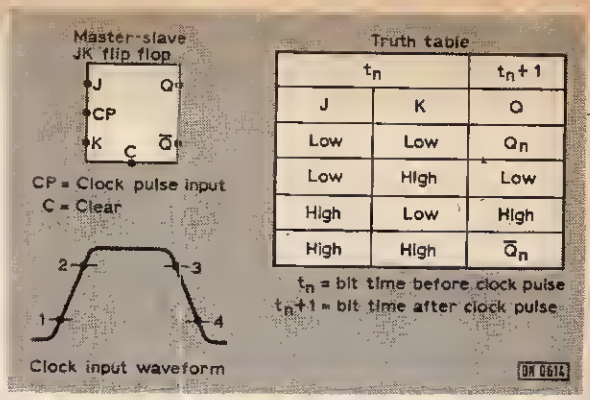


Fig. 23 : SN7400N integrated circuit and truth table.

Each gate has two inputs and one output and the operation is shown in the truth tahle. It can he seen that only when input 1 AND input 2 are high will the output NOT he high, i.e. low. In the circuit of the instrument some gates are shown with only one input and here the other input is left disconnected. This is equivalent to connecting it to a high input. In this condition the gate hecomes an invertor, the output condition is the inverse of the input.

7473N Dual Master-Slave J.K. Flip Flops

The SN7473N contains two Master-Slave J.K. Flip Flops, each flip flop contains a large numher of gates all internally connected to form a hi·stahle or flip-flop in which the state of the outputs for specific input conditions is clearly defined. This is shown in the truth tahle in Fig. 24. What this means is that if J and K are hoth low, no change takes place during the clock pulse. But if K is high and J is low the clock pulse will cause Q to go low and conversely if J is high and K is low the clock pulse will cause Q to go high. And finally if J and K are hoth high Q will change state at each appearance of the clock pulse. With J and K hoth high the circuit makes a divide hy two divider stage, the output from Q heing half the frequency applied to CP.



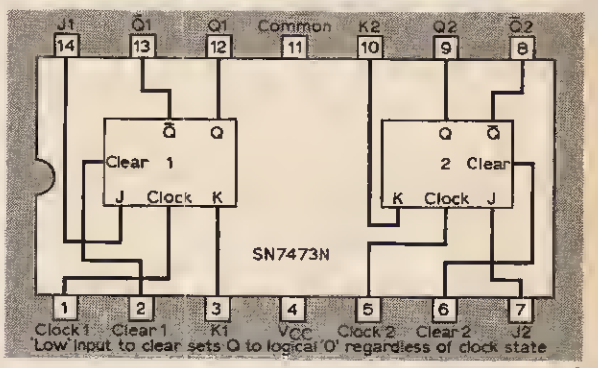


Fig. 24 : SN7473N integrated circuit and truth table. The sequence of operation relative to the clock waveform is also shown.

In the master-slave JK flip flop, the input to the master section is controlled hy gates operated hy the clock pulse. The clock pulse also regulates the state of more gates which connect the master and slave sections. The sequence of operation, relative to the clock waveform shown in Fig. 24, is as follows:

1. Isolate slave from master.
2. Enter JK input information into master.
3. Disahle input gates.
4. Transfer information from master to slave.

The input C is a direct clear input which restores Q to low irrespective of any other input signals.
opposite logic condition to Q.
instrument is in storing information and transferring this on the application of a pulse to the clock pulse
$\bar{Q}$ is the reciprocal of Q and always has the
The use of the Master-Slave JK Flip Flop in the input.

7490N Decade Counter

The SN7490N contains 4 flip-flops and 3 gates forming a divide by 2 stage and a divide hy 5 stage.

When used as a hinary coded decimal counter, the signal input goes to the divide hy 2 stage and from the output of this to the divide hy 5 stage. The hinary coded decimal output is then availahle as shown in Fig. 25.

When used as a frequency divider, as in the Crystal Oscillator divider panel, it is more convenient to feed the signal ioto the divide hy 5 stage nrst and then the divide hy 2 stage, this ensures a 1:1 square wave output which has certain advantages when used as a calihrator output. The other arrangement

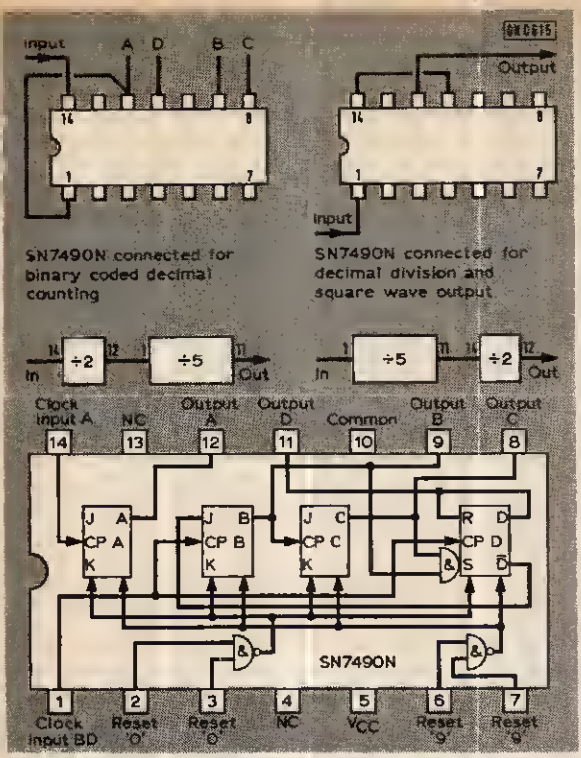


Fig. 25 : SN7490N integrated circuit used as a binary coded decimal counter.

will of course also divide by 10 hut the output waveform is far from symmetrical. The SN7490N has input connections for resetting to "9" or "0" and in the instrument only the reset to "0" is used.

74141N B.C.D. to Decimal Decoder Driver

This device contains a complex arrangement of gates terminating in ten high voltage transistors for driving the numeral indicator tube. The operation of this device was illustrated in Part II of this series (Fig. 9, page 480, October 1971 issue).

A number of queries have been received regarding the use of a SN7441AN device in place of the SN74141N. The SN7441AN was in fact used in the prototype and whilst a number of these functioned satisfactorily a few gave trouble by loading the decade counter excessively and causing an incorrect count.

The SN74141N is an improved version of the original SN7441AN. ■