The testing of digital circuits can be quite a headache. Our old faithful, the multimeter, is quite useless because of the operating frequencies: the logic levels change so rapidly — thousands or millions of times per second — that even a digital multimeter is unable to cope. This problem can be solved in two ways: buy a higher quality test instrument or lower the operating frequency of the circuit under test. If you opt for the last, you will find our digitester just the thing!

digitester with a difference

universal test aid for digital circuits

Digital circuits normally operate at speeds which make it impossible for normal test instruments to be used for checking or fault finding. For instance, in an analogue multimeter, the inertia of the pointer prevents the reading of the level of a pulse train. The normal digitester does not help here either; it may well give an optical indication of the logic level at the pin of an IC, but only as regards a static or slowly changing situation. When rapid changes occur, the digitester is also quite useless. This is, however, not because of inadequacies in the instrument, but rather because of the slowness of our eyes.
When an LED blinks at only 20 Hz, few of us see this as a series of light pulses: most will just see a continuous light.
It is by now evident that to test digital circuits or to be able to experiment with them it is necessary to slow down the speed of operation. The easiest way to do this is to disable the internal clock of the circuit and replace it by an external one operating at a much lower frequency. In some cases, it is even better to work with just one pulse at a time, instead of with a pulse train.

The circuit

Fewer ICs than shown in figure 1 are required to generate a single pulse or pulse train of low frequency. None the less, the additional ICs used here make for a more 'comfortable' circuit. So, let's see...
The generation of a single pulse is effected primarily by NAND gates N1 . . . N4. Gates N1, N2 form a flip-flop of which the logic level at outputs Q1 and $\overline{Q1}$ is dependent on the position of switch S1. As drawn, Q1 is logic low (0) while $\overline{Q1}$ is logic high (1). The high signal at $\overline{Q1}$ is indicated optically by LED D1 via gate N18. A second single pulse is generated by gates N3, N4: their logic levels at outputs Q2 and $\overline{Q2}$ are optically indicated by LEDs D3 and D4.
The two bistables, N1/N2 and N3/N4, debounce switches S1 and S2 which ensures that only one pulse is present at their outputs. This pulse can be used in the circuit under test as clock, counter, reset, and so on.
Apart from single pulses, there is, of course, a need for low-frequency pulse trains. The generator required for this is formed by NAND Schmitt trigger N9, resistor R13, and capacitor C1. With values shown, the frequency is around 50 Hz. A second pulse-train oscillator, formed by N10, R14, and C2, operates at the much lower frequency of 2 Hz, which is optically indicated by LED D5.
So much for the description of the required generators. But what if you want to apply a single pulse followed by a pulse train to a circuit? It would not do to have to change from one output to another. No, for this purpose we have added an electronic switching circuit consisting of S3, NOR gates N5 . . . N7, NAND Schmitt Triggers N8, N11, and NAND gates N12/N13 and N16/N17. The output, pin 8 of N17, depending on the setting of S3, is either the Q2, the 2 Hz, or the 50 Hz signal. The logic output level is optically indicated by LED D6:

- if D6 lights continuously and independent of the setting of S2, the output is a 50 Hz pulse train;
- if it blinks rhythmically, the output is a 2 Hz pulse train;
- if it lights depending upon the setting of S2, the output is the logic level of Q2.

All outputs are buffered, which enables up to 30 TTL circuits to be connected to them.
Finally, the function of switch S4. When this switch is open, the output of N17 is open, that is, it contains the signal selected by S3. If S4 is closed, however, the output of N17 is logic low and the signal selected by S3 is therefore not available at pin 8.

1

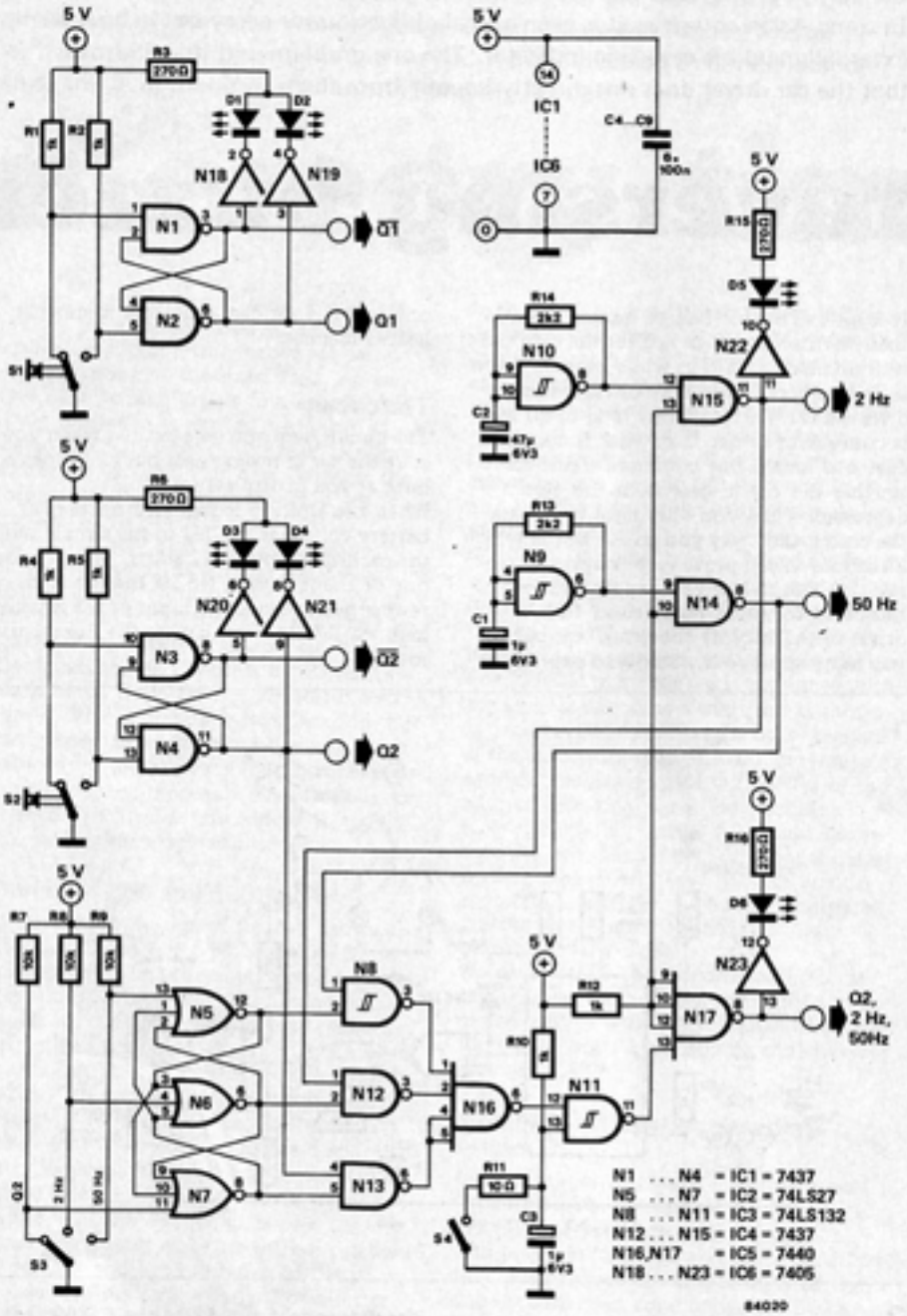

Figure 1. The digitester comprises five functional circuits: two single-pulse generators, two pulse-train oscillators, and an electronic switch.

Construction

As you have seen from the circuit diagram, the digitester needs a supply of 5 V. This is best obtained by means of a 5 V voltage regulator: a 500 mA type will do nicely. The supply voltage to each of the ICs should be individually decoupled by a 100 nF capacitor.

The power supply is best built into a case together with the digitester so that you have an independent, self-contained test instrument for digital circuits.

If you want to use the digitester with CMOS circuits, it will be necessary to adapt the (TTL) outputs to the CMOS logic under test. This is relatively simple and is described in some detail in the article 'mating logic families' elsewhere in this issue. ⋈