BY HOWARD JOHNSON, PhD

Terminator

My friend Lloyd builds timing analyzers for high-energy physics experiments. In these experiments, an array comprising hundreds of detectors senses the times of arrival for the spray of particles emanating from a cascading sequence of atomic interactions.

Each detector connects through a length-matched coaxial cable to Lloyd's analyzer. The analyzer records the times-of-arrival data and triangulates the location of each atomic event. When calibrated, the accuracy of the system is truly awe-inspiring.

The detectors are mounted in a high-radiation zone 3 ft from the analyzer. At that distance, the RG-58A/U 50Ω coaxial cable may slightly degrade the 400-psec rise time of the detector outputs. However, that situation does not matter as long as the cable affects each detector the same way and as long as the step response of the cable itself adds no significant jitter. (It doesn't.)

The reflections that may occur between the detector outputs and the analyzer inputs *do* matter. If any late reflections occur, the reflected signals may perturb the rising edges from subsequent events, shifting their apparent times of arrival. You cannot postprocess out of the system the jitter that this mechanism induces.

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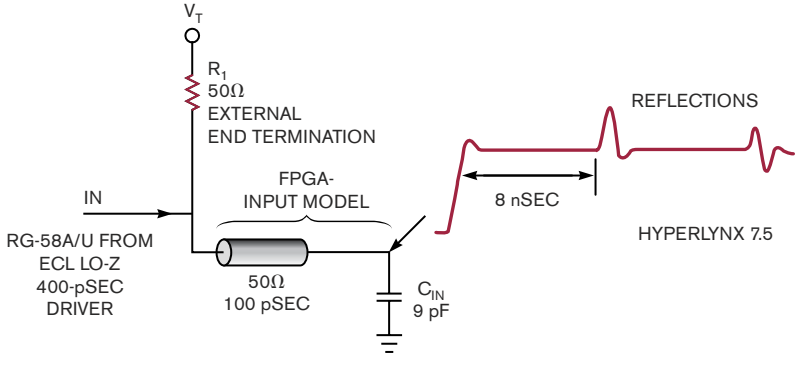

Figure 1 The FPGA-input capacitance creates massive reflections.

If you can limit the magnitude of the reflections to, say, X% of the signal swing, then the worst-case time-domain jitter that those errant reflected blips induce will amount to only X% of the signal rise time.

At this point, you are probably thinking about termination at both ends. That scenario is an excellent way to mitigate reflection. However, just for fun, imagine that a government contractor built the detectors and that they provide low-impedance ECL outputs. You cannot change them. Consequently, the analyzer must provide near-perfect end terminations.

Next, stipulate that, for cost reasons, you must use an off-the-shelf FPGA to receive the detected signals. The FPGA incorporates switchable internal resistors, but they are insufficiently accurate for this application. Your contract mandates external terminating resistors, 50Ω±1%, for each signal.

Unfortunately, even with a perfect external termination, the 9-pF capacitance of the FPGA input creates massive reflections (**Figure 1**). The reflections return every 8 nsec, commensurate with the round-trip delay of the coaxial cables. The person who wrote the system specification failed to consider that fact.

In any system in which the time constant, $\frac{1}{2}Z_0C_{IN}$, approaches the rise time of your source, you can expect these types of big reflections.

Given these specifications, can Lloyd's system possibly work? Stay tuned for my next column, when we will work on the answer together. EDN

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