Single-Supply IF-Strip Digitizes QAM Signals

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Quadrature amplitude modulation (QAM) and quadrature phase-shift keying (QPSK) systems abound. In quadrature schemes, two independent signals ("in-phase" and "quadrature") are transmitted via a single carrier, making use of the orthogonality of signal components at 90°. Cellular standards, such as the international GSM standard, the US IS54, IS95, and IS136 standards, and the Japanese PHS, all require I/Q demodulation in some form. Other applications for QAM or QPSK include CATV set-top-box converters and hybrid fiber/coax video transmission.

Two common demodulation schemes for QAM and QPSK IF signals are quadrature (I/Q) demodulation and direct digitizing. In quadrature demodulation, a pair of mixers driven in quadrature demodulate the IF into its baseband I and Q components; they are then digitized by a pair of A/D converters. In direct digitizing, a single A/D converter samples the IF, eliminating a down-conversion; the digitized IF is then demodulated digitally.

Direct digitizing can be implemented with a handful of passive elements and four low-cost ICs: the AD607* IF Subsystem [see the sidebar for details], developed for cellular radio applications, the AD876* 10-bit, 20-MSPS A/D converter, and two AD8011* op amps. The system (Figure 1) provides a 45-dB spurious-free dynamic range (SFDR) over a 4-to-6-MHz bandwidth for such applications as CATV and hybrid fiber/coax; it can demodulate 64 [8×8] QAM and 256 [16×16] QAM with a low bit error rate (BER).

The signal chain: The key components of the integrated solution are the AD607 IF Subsystem, and the AD876 A/D converter, plus an active filter tailored for the application.

A typical input to the IF strip is from a surface-acoustic-wave (SAW) filter that establishes the system bandwidth and filters out adjacent channels. The AD607's first stage down-converts the input from a 45-MHz first IF to a 5-MHz second IF, using a 40-MHz local oscillator (LO). The spectrum at the output of the AD607's mixer (MXOP) contains the desired demodulated IF frequency ($f_{in} - f_c$), and an image frequency ($f_{in} + f_c$). The mixer's output is passively low-pass filtered by a three-pole, 7-MHz, Chebyshev filter,† comprising a two-pole LC stage that feeds the AD607's amplifier strip, plus a single-pole RC stage at the IFOP output.

Because of the high gain and bandwidth of the AD607's IF amplifiers, some filtering is necessary to limit noise and prevent aliasing in the AD876. The last stage of the Chebyshev, the simple RC section, limits the noise bandwidth of the IF strip to about 10 MHz. A 3rd-order Butterworth high-pass filter [U3 and U4] further reduces low-frequency noise. U3's 14-dB ac gain amplifies the ±100-mV (–10 dBm) IFOP signal from the AD607 so that peak signals span the AD876's full input range.

The input to the AD876 is ac-coupled; this level-shifts the signal to the A/D's nominal input range and avoids concerns about headroom at the output of the AD8011 with a single supply. The AD876's reference voltages, generated by a simple resistance network, set the boundaries of its input range. R1 and R2, in conjunction with the 250-Ω resistance ladder inside the AD876, provide 3.5 & 2.5-V reference voltages at REFTF and REFBF.

The 40-MHz local oscillator frequency is halved to provide a 20-MSPS sample clock for the AD876. Oversampling the analog input simplifies filtering of the output by the digital processor.

Distortion Analysis: Figure 2 shows measured output spectra at the extremities of an assumed input range of –35 dBm to –55 dBm. To predict the level of intermodulation distortion (IMD), the system is analyzed for both the minimum and maximum expected signal levels. To simplify the analysis, the effects of a low-noise amplifier (LNA) are not included. However, many systems would include an LNA at the front end to increase the signal-to-noise ratio.

The IMD for the AD607 is predictable and increases as signal levels increase. The third-order intercept specification of the AD607 indicates that performance will remain acceptably linear over the above input signal range. The amplitudes of the third-order products are generally the most important; they lie close to the input signal frequencies and are not removed by filtering. The calculated third-order intermodulation products should remain at least 45 dB below the fundamental for signals up to –27.5 dBm. Because the spurious-free dynamic range from the AD8011s and the AD876 is typically greater than 60 dB, they do not contribute substantially to the overall noise and distortion.

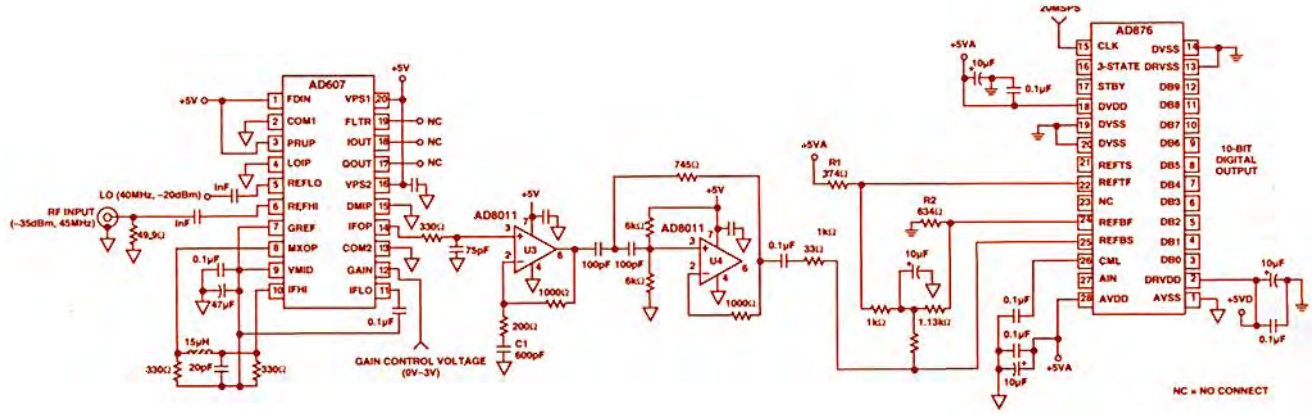


Figure 1. Schematic of direct IF-to-digital converter.

*Use the reply card for technical data. **Circle 2** for AD607 (prices begin at $5.95 in 1000s), **Circle 1** for AD8011 and AD876.

† The phase distortion introduced by the Chebyshev filter may be a problem in systems without some form of equalization.

The table summarizes the individual gains and cumulative levels at each stage for the max and min signal levels. It can be used for analyzing the effects of gain distribution on IMD and noise.

	Signal	Mixer	Mixer gain	Low-pass	IF amps	Low-pass	High-pass
Stage gain (dB)	Max	−6	7.9	−3	26.1	0	14
	Min	−6	13	−3	41	0	14
Cumulative gain (dB)	Max	−6	1.9	−1.1	25	25	39
	Min	−6	7	4	45	45	59
Level (dBm)	−35	−41	−33.1	−36.1	−10	−10	4
	−55	−61	−48	−51	−10	−10	4

Measurement of Performance: Communication systems use specialized tests, such as bit error rate (BER) and spectral analysis (FFT) to provide a figure of merit for receiver distortion performance. Figure 2 shows the 8-k FFT of the AD876 output resulting from a two-tone input at 45.02441 and 45.39056 MHz (IF outputs at 5.02441 and 5.39056 MHz) for the minimum and maximum signal levels. Shown are the (numbered, aliased) harmonics of the 5.39056-MHz signal, plus other related spurs. The SFDR for the entire system can be seen. All spurious tones are at least 47 dB below the fundamentals. The dominant spurious components are the 3rd and 5th order IMD products.

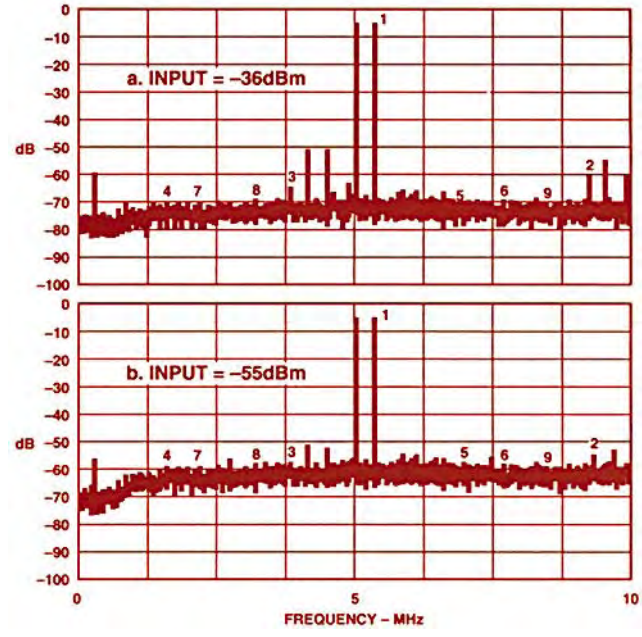
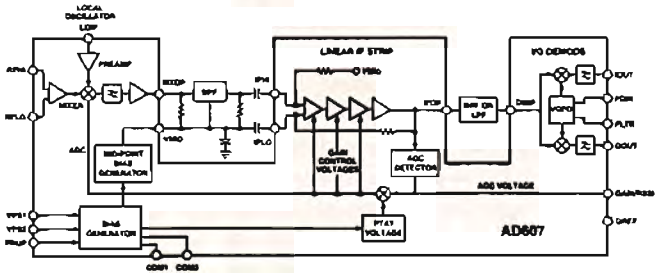


Figure 2. Two-tone FFTs of IF strip.

AD607 ARCHITECTURE

The AD607 comprises a mixer with a LO preamp, a linear IF strip with voltage-controlled gain, dual (I & Q) demodulators, each followed by a 2-pole, 3-MHz low-pass filter, and a phase-locked voltage-controlled quadrature oscillator to provide the in-phase and quadrature clocks, as well as an on-board peak detector and AGC loop with a received-signal strength (RSSI). The IF strip's output is available for insertion of a low-pass or bandpass filter for noise reduction and/or an A/D for direct digitizing, as in Figure 1.



The signal path begins with the mixer. Although most IFs are in the 45 to 300-MHz range, it can accept inputs as high as 500 MHz. Its input-referred 1-dB compression point is −15 dBm (or ±54 mV, regardless of input termination) and its input third-order intercept point (IIP3) is −8 dBm. Both are measured with a 50-Ω source and 50-Ω input termination.

The mixer provides a high-impedance current output to drive a parallel-terminated filter; this avoids a 6-dB (voltage-mode) series termination loss. The conversion gain is specified for operation into an IF band-pass filter (BPF) load of 165 Ω, i.e., a 330-Ω filter doubly shunt-terminated and assuming a local oscillator drive at LOIP of at least −16 dBm (±50 mV, regardless of input termination). The IF signal voltage at pin MXOP can swing 2 V p-p when using a 3-V supply; the high headroom minimizes the likelihood of significant intermodulation from adjacent-channel and other strong interfering signals at the mixer output.

Both the mixer's conversion gain and the IF amplifier gain (dB) are proportionally controlled by the voltage, V_G, at pin GAIN/RSSI. The gain of all sections is maximum when V_G is zero, and decreases, reaching a minimum at [V_P – 0.8 V], where V_P is the supply voltage; for example, V_G = 2.2 V for V_P = 3 V. Gain-control scaling is proportional to a reference voltage applied to GREF; when GREF is at the mid-point of the supply (VMID), the scale is nominally 20 mV/dB, or 50 dB/V.

Pin GAIN/RSSI, as an output, provides an RSSI voltage derived from the IF peak detector's output voltage; as in input, it accepts an external gain control voltage. In either case, the gain-control voltage to the IF amplifier cells is multiplied by a voltage proportional to absolute temperature (PTAT) so that the overall gain scale-factor is insensitive to temperature.

Low-impedance IF output, IFOP, may be loaded by resistances as low as 500 Ω to VMID. This output can either be digitized by an external A/D converter, as in Figure 1, or routed to the on-chip demodulator (DMIP) via a low-pass or bandpass filter to attenuate wideband noise generated in the high-gain IF amplifiers. For example, a single-pole low-pass filter at the IF reduces the signal level by 3 dB, but it improves the S/N ratio by reducing the wideband noise presented to the demodulator. Each demodulator comprises a full-wave synchronous detector and a two-pole low-pass filter, producing single-sided outputs at IOUT and QOUT.

The I and Q demodulators are driven by quadrature signals provided by an on-chip phase-locked loop (PLL)with its reference (at pin FDIN) at the IF.

The PLL's variable-frequency quadrature oscillator (VFQO) ensures excellent phase accuracy, as well as low EMI and power consumption. The PLL uses a sequential-phase detector (SPD), implemented in low-power current-mode logic, and a charge pump, which can source or sink 40 µA. The VFQO control path is filtered using an external CR network connected to FLTR. The circuit is designed to hold the frequency-control voltage on this pin for rapid reacquisition after power-down.