FPGA-DSP Board for Narrowband SDR

Part 2: transmission and RF front end

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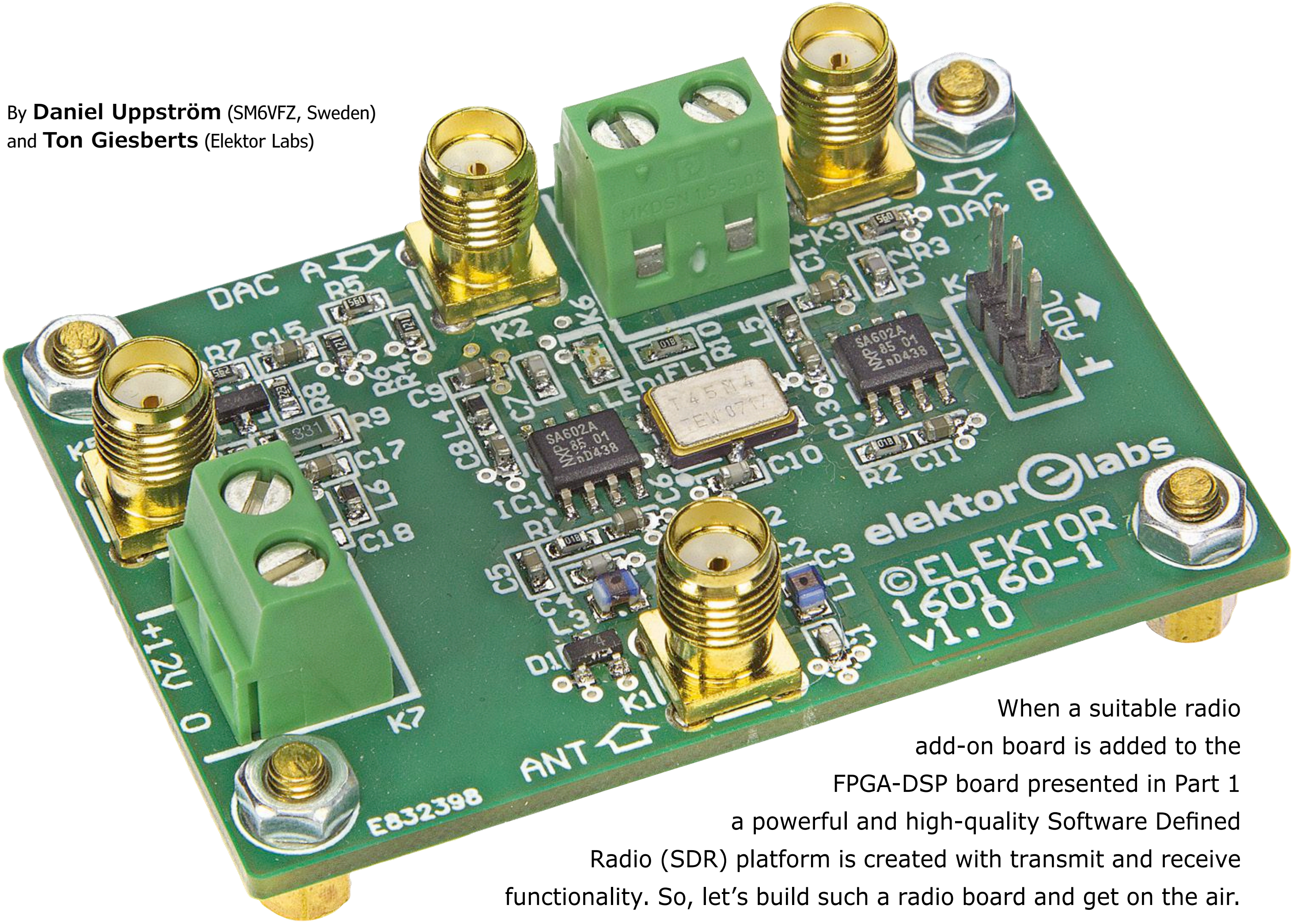


When a suitable radio add-on board is added to the FPGA-DSP board presented in Part 1 a powerful and high-quality Software Defined Radio (SDR) platform is created with transmit and receive functionality. So, let's build such a radio board and get on the air.

Features

- FPGA + DSP + Audio CODEC
- Narrowband software defined radio (SDR) platform
- FPGA board can be used for radio operation at virtually any frequency between zero and many GHz
- Uses superheterodyne principle
- Low second IF >0 Hz
- RX (receive) and TX (transmit)
- Weaver SSB modulator/demodulator

However, before we dive into the part where we solder tiny capacitors, resistors, crystal filters and the like on a printed circuit board especially developed for this occasion, we will finish our description of the FPGA-DSP board initiated in part 1 [2]. Indeed, the reception and decoding of radio signals was treated in quite some detail, but not much was said on using the system in transmit mode. Therefore, in order to provide you with as much background information as possible about this exciting part, let's have a look at "doing TX" with the FPGA-DSP board. You may want to get out **Part 1** first to refresh your memory and also to have all the illustrations handy.

Digital signal processing — transmission

When the push-to-talk (PTT) signal on header K7 is pulled logic Low (see Part 1, Figure 2), the FPGA goes into transmit mode. A CW carrier can then be generated with the DDS block in the FPGA, through the DAC, by pulling the KEY signal Low.

In addition, the Weaver blocks are implemented in such a way that they can be used “backwards” to form an SSB modulator. When USB or LSB is selected and PTT pulled Low, the audio at the microphone input is sampled, compressed and low-pass filtered, and then fed to the modulator. This works very well, but needs external filtering due to the difficulty of up-sampling from the low KSPS rates in the audio and modulator to the high 120 MSPS rate used by the DAC.

The two spectrum plots in **Figure 1** show transmitter signals generated in the 14 MHz (20-m) amateur radio band. The graph on the left is a CW signal generated directly by the DDS. The discrete noise components, spurious responses or “spurs”, around the carrier are around −70 dBc (i.e. they have an amplitude of −70 dB relative to the carrier) and originate from clock signals inside the FPGA. This signal may be amplified to, say, 5 to 10 watts and transmitted while keeping interference risks low.

The spectrum on the right of Figure 1 shows the output from the Weaver SSB modulator when fed with an audio signal. Here the internal clock signal residues are much stronger, and strong alias products due to the modulation are visible too. With these unwanted signal components now as strong as −30 dBc, one should not simply amplify and transmit; filtering is required.

Apart from the spurious/alias products from the modulator there are also other limitations to be aware of. These stem mainly from the fact that the non-modulated signals generated by the FPGA through the DAC are not as clean as one would want ideally. This has two reasons mainly:

1. The clock for the DAC, generated at 240 MHz and then divided by two, is created by the internal PLL circuitry of the FPGA. This master PLL clock signal is not ideal with respect to phase noise, i.e. its output has a certain amount of jitter and is not a perfect square wave with an exactly determined frequency and phase.
2. There will also be discrete spurious frequency components in the output. These have different origins, like unwanted coupling between different clocks, or quantization effects in the DDS blocks and lookup tables due to word-size limitations in calculation steps, memory and DAC resolution. Some of these parasite signals are visible in the unmodulated spectrum in Figure 1 (left graph).

All these effects combined limit the maximum output power that is possible in transmit mode if one wants to respect radio regulations and avoid creating interference for other users and radio services. They could also have an influence on the receiver and potentially limit the selectivity and dynamic range. There are, however, ways to solve this problem,and they will be discussed further on.

A simple radio board

We now present a simple radio board for shortwave (SW) reception (i.e. downwards of 30 MHz). It is constructed according to the block diagram shown in **Figure 2**.

The antenna signal is low-pass filtered and amplified. By mixing it with a local oscillator (LO) signal from DAC A, the frequency of interest is converted to 45 MHz before it is passed through a crystal fil-

PROJECT INFORMATION

FPGA | DSP | SDR | Radio | Transmitter | Receiver | Amateur Radio

entry level
intermediate level
→ expert level

2 hours approximately

SMD Soldering Tools

£45 / €50 / $55 approx.

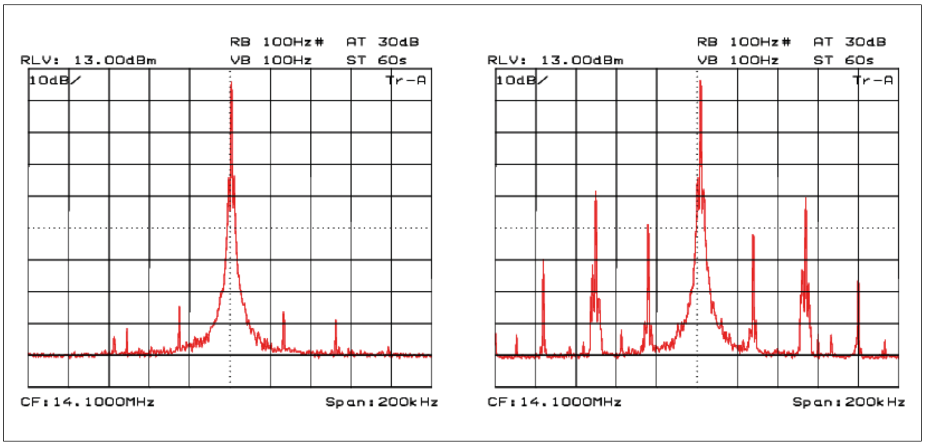


Figure 1. Two spectra of a CW signal produced by the FPGA-DSP board in transmit mode. Left: without modulation; right: with modulation. The center frequency is 14.1 MHz, the span is 200 kHz, the vertical axis is 10 dB/div.

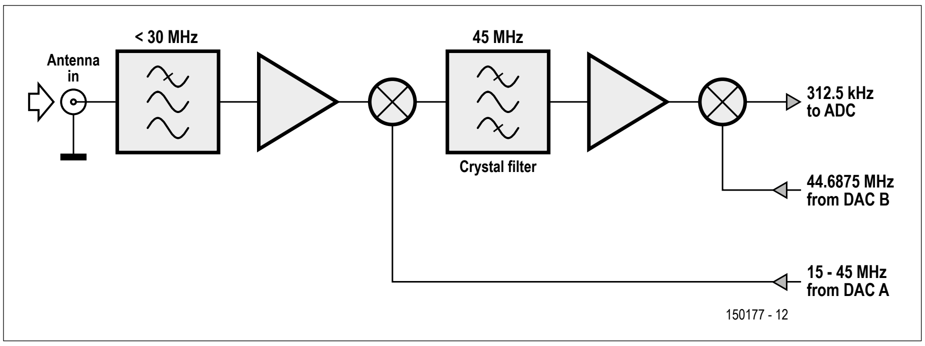


Figure 2. Block diagram of a radio add-on board.

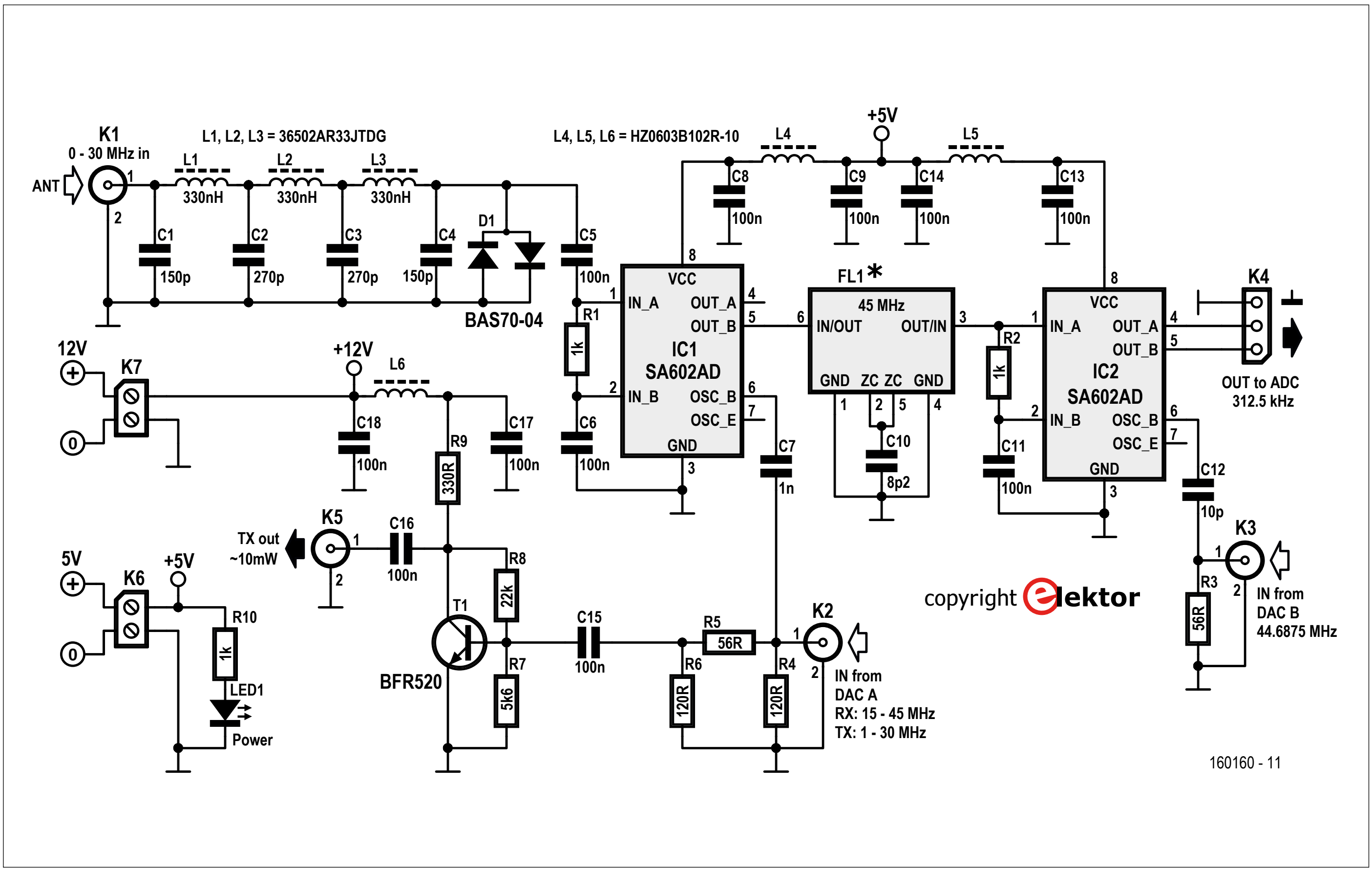


Figure 3. The circuit for a radio board suitable for receiving and transmitting at frequencies up to 30 MHz.

ter. This intermediate frequency (IF) signal is amplified before entering a second mixer where it is converted down to a second IF signal centered at 312.5 kHz (see Part 1) with the help of a second LO signal provided by DAC B. The second IF signal is digitized by the ADC and fed into the FPGA where it is processed and ultimately demodulated to audio.

Such a radio board, together with the FPGA DSP board, works very well for the reception of signals from virtually zero up to around 30 MHz. When connected to a large antenna that picks up both weak and strong signals the receiver does not easily saturate and will not produce distorted audio. It can therefore be used for serious work and reception of sporadic and weak signals.

The schematic of the radio board is shown in **Figure 3**.

The antenna is connected at K1 where it enters a low-pass filter intended to remove FM broadcast signals and other potential VHF/UHF interferers. The anti-parallel diode pair D1 limits very strong signals passing through the filter while it also provides a DC return path for static charge that otherwise can build up in a long and isolated antenna wire. A good old SA602 (IC1), amplifies the signal and mixes it with the one coming from DAC A (connected to K2). Crystal filter FL1 provides sharp filtering at the first intermediate frequency. FL1 with its center frequency at 45 MHz is a bit of a difficult part to obtain. Ideally it should have a bandwidth of 15 kHz, but 30 kHz may work too; 7.5 kHz, on the other hand, is too narrow for good quality AM. The impedances of the SA602 and the filter match fairly well so no additional matching components (which would be needed otherwise) are used. A second SA602 (IC2) mixes the output of FL1 with the signal produced by DAC B to create the second IF as a differential signal, available at K4, to be fed to the ADC of the FPGA board.

Transmission

For the licensed radio amateur it is easy to add a few components to this simple radio board to allow the system to be used as a transmitter. In transmit mode, DAC channel A will then generate a CW carrier directly in the 0-30 MHz range which is amplified by T1 to 10 mW or so. It is then only a matter of amplifying this signal to a few watts using an external power amplifier (PA), connect it to a tuned antenna and communicate with other stations at thousands of miles away across the nation or globe.

The maximum power possible (for CW mode/carrier) is debatable, but the author would not recommend more than 5 to 10 watts on shortwave, based on the remarks above about the spectrum purity. Such a power level is obviously less than the “standardized” 100 W available from commercially built shortwave transceivers but it still enables communication around the globe when the conditions are favorable, and intercontinental daily operation in the 40 m (7 MHz) amateur band for instance.

Less noise, more transmit power, VHF and up

The radio board presented here is good for reception and CW low power transmission, and should be a good and simple starting point overall. However for serious amateur radio where the goal is to build a high-performance transceiver (i.e. a combined receiver and transmit-

COMPONENT LIST

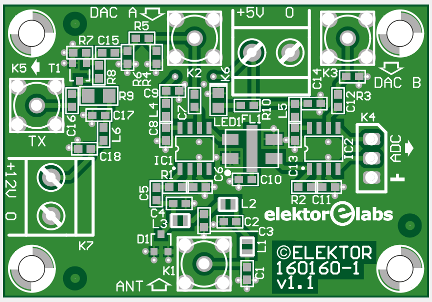
Resistors
Default: 1%, 100mW, 0603
R1,R2,R10 = 1kΩ
R3,R5 = 56Ω
R4,R6 = 120Ω
R7 = 5.6kΩ
R8 = 22kΩ
R9 = 330Ω, 1%, 250mW, 1206

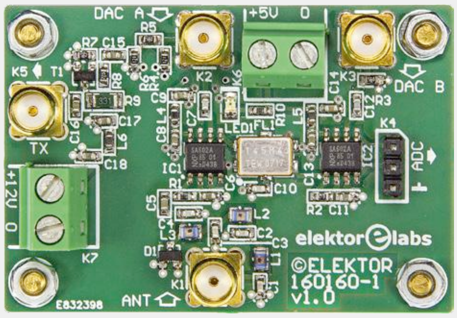
Capacitors
Default: 0603
C1,C4 = 150pF
C2,C3 = 270pF
C5,C6,C8,C9,C11,C13-C18 = 100nF
C7 = 1nF
C10 = 8.2pF, ±0.25pF
C12 = 10pF

Inductors
L1,L2,L3 = 330nH, 5%, 310mA, f_{res} 60 MHz (36502AR33JTDG, TE Connectivity)
L4,L5,L6 = 1000Ω @ 100MHz, 200mA (HZ0603B102R-10, Laird Technologies)

Semiconductors
D1 = BAS70-04
LED1 = green, 0805
T1 = BFR520
IC1,IC2 = SA602AD, SO-8

Miscellaneous
K1,K2,K3,K5 = SMA connector, straight jack, 50Ω
K4 = 3-pin pinheader, 0.1” pitch, vertical
K6,K7 = 2-way PCB screw terminal block, 0.2” pitch
FL1 = 45MHz crystal filter, 1kΩ, BW=15kHz (see text), e.g. Golledge crystal filter GSF-75 45R15B1 45.0MHz
PCB # 160160-1





ter) comparable to or better than what is commercially available, with a clean transmit spectrum to enable SSB transmission also, a more advanced radio topology has to be chosen.
Adding a filter bank to filter out anything outside the band one is tuned to is tempting and would help to get rid of some spurious signals (“spurs”) and harmonics, but the phase noise and jitter around the carrier cannot easily be filtered out and thus set a limit for this seemingly easy approach. It is also unlikely that filtering the modulator alias products will help much if the filter is not particularly sharp (which is impractical since it would need to be tuned to the exact frequency of operation).
Instead, the more practical way to do things is to generate the TX carrier at the crystal filter frequency (45 MHz), filter out all alias components and spurs, and mix it down to the channel frequency (within 0-30 MHz) with the help of a

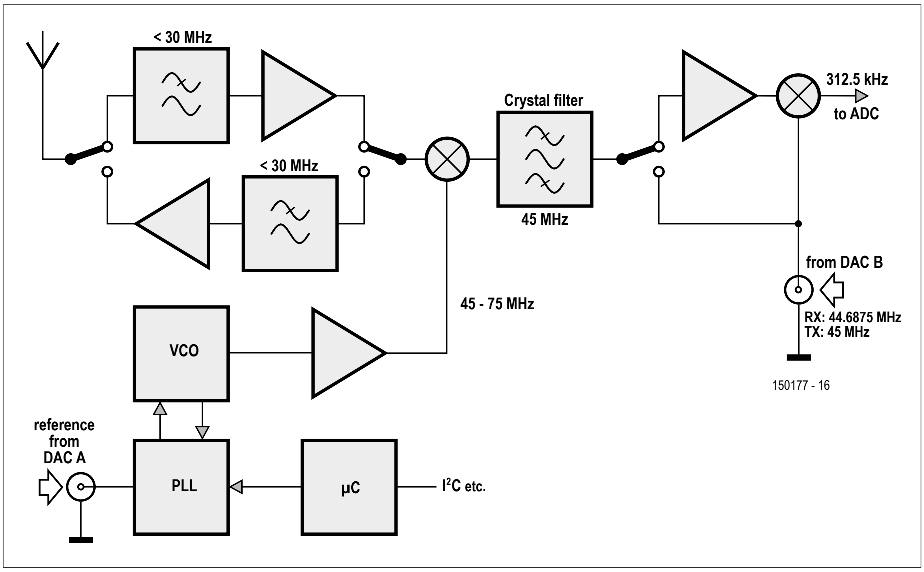


Figure 4. Block diagram for a transceiver suitable for SSB voice transmission.

local oscillator (LO) tuning in the range 45-75 MHz. This LO can be generated from a voltage controlled oscillator (VCO) that is phase-locked to a reference signal coming from one of the DAC channels. This approach fully enables SSB voice transmission. A transceiver block diagram is shown in **Figure 4**.

For higher frequencies, like the 144 MHz amateur band, a similar topology could be used but it is then a better choice to have the first IF at 21.4 MHz, where sharper crystal filters are available, and have the VCO at around 165 MHz.
In the 2 m (144 MHz) band there are sometimes many strong signals from local amateurs and out-of-band transmitters which also place higher requirements on the blocks in the receiver chain. The use of a good mixer and a sharp crystal filter is necessary. It is also very important to transmit clean signals. The higher gain of antennas and more of line-of-sight propagation at VHF than at shortwave can create huge signal levels at fellow radio amateurs in the vicinity. It is not a rare situation to listen to weak signals at −140 dBm while simultaneously having a local transmission at −30 dBm just tens of kHz away. Meaning we want a (blocking) dynamic range in excess of 100 dB, with signals 10,000,000,000 times stronger than the noise floor without raising the latter at adjacent frequencies!

Join us

In this article we did not present any detailed design of a radio board for full performance. Experiments with such boards are ongoing [4] and a complete 2-meter radio has been built by the author. Depending on the interest and feedback received we may proceed to publish more details in the future. To build a transceiver is a big project and radio amateurs and experimenters are encouraged to join in with their designs and suggestions!

Coming next…

In a future installment a control board will be presented to take care of the user interface and the digital communication with the FPGA, which is the remaining piece for a complete bench-top radio.

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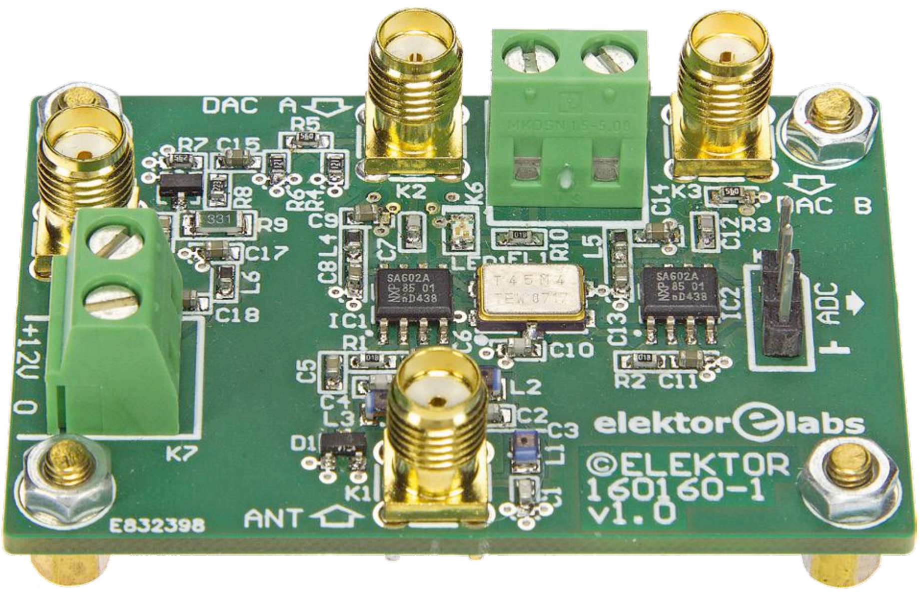

Web Links

[1] www.elektormagazine.com/160160

[2] www.elektormagazine.com/150177

[3] www.elektormagazine.com/labs/fpga-dsp-radio-for-narrow-band-communications-150177-i

[4] Author's blog: sm6vfz.wordpress.com