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AFAL-TR-76-28

FET POWER AMPLIFIER

Texas Instruments Incorporated

April 1976

TECHNICAL REPORT AFAL-TR-76-28

Final Technical Report for Period 1 March 1975 - 30 November 1975

AIR FORCE AVIONICS LABORATORY

AIR FORCE WRIGHT AERONAUTICAL LABORATORIES

AIR FORCE SYSTEMS COMMAND

WRIGHT-PATTERSON AIR FORCE BASE, OHIO

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This final report was submitted by Texas Instruments Inc., Dallas, Texas 75222, under contract F33615-75-C-1123, job order number 69CK0135, with the Air Force Avionics Laboratory, Wright-Patterson AFB, Ohio 45433. Chern I. Huang, AFAL/DHM-1, is the project engineer for the project.

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This program had as its objective the development of an X-band GaAs FET power amplifier. Advances were made in materials, device, and microwave circuit technology during the course of the amplifier development.

Devices with 2400 μm gate width from nine device runs (seven different epitaxial slices) produced 1 W or more at 9 GHz with 4 dB gain and power-added efficiencies of 20 to 30%. Two device chips were connected in parallel to give a total gate width of 4800 μm. In this case, an output power of 2.5 W was

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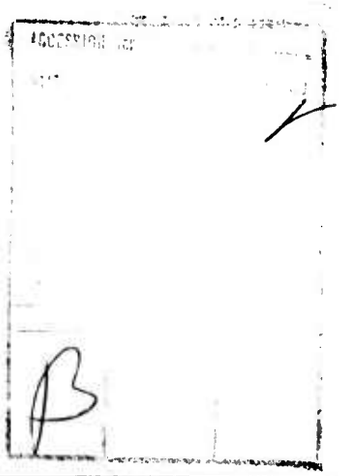
achieved at 8 GHz with 4.0 dB gain and 25% power-added efficiency.

An output power (cw) of 360 mW was achieved with a gain of 20.5 dB at 9.3 GHz for a three-stage FET amplifier. The 3 dB bandwidth was 1.0 GHz (8.9 to 9.9 GHz). This performance exceeded the contract goals. A microstrip hybrid FET (three-stage)/IMPATT amplifier was fabricated that had an output power of 1.2 W with 26 dB gain at 9.5 GHz with a 700 MHz 3 dB bandwidth. This amplifier also met the performance goals. Two three-stage FET amplifiers and two FET/IMPATT hybrid amplifiers were delivered to AFAL.



FOREWORD

This project was initiated by the Air Force Avionics Laboratory and was under the direction of Dr. Chern Huang (AFAL/DHM). This report is a summary of the entire research program conducted from 1 March 1975 to 30 November 1975.

The work described herein was carried out at the Central Research Laboratories of Texas Instruments Incorporated, 13500 North Central Expressway, Dallas, Texas 75222. The program was initially directed by Dr. D. N. McQuiddy and was completed under the direction of Dr. W. R. Wisseman. Other principal contributors were Dr. R. L. Adams, Dr. H. M. Macksey, Dr. V. Sokolov, and Dr. H. Q. Tserng.

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SECTION I

INTRODUCTION AND SUMMARY

This is the final report for a nine-month program carried out under Contract No. F33615-75-C-1123, for the development of an FET power amplifier. The amplifier is designed to operate at 9.5 GHz with a 600 MHz 3 dB bandwidth and 20 dB gain and to deliver 300 mW cw output power. The FET amplifier is to be used with an IMPATT single-stage amplifier to give an output power of 1.2 W with 26 dB gain over the same frequency band.

Although the end goal of this program was the development of multistage amplifiers that meet the specifications given above, a major device development effort was also required, since suitable devices for the amplifier were not available at the outset of the program.

The program was divided into three phases: (1) GaAs epitaxial growth and transistor process optimization, (2) large signal transistor circuit development, and (3) multistage amplifier design. Significant progress was made on all three phases of the program; however, throughout most of the program the major effort was devoted to Phase I. FET microwave performance was well below that required to meet the amplifier specifications until the last one and a half to two months of the program. At that point, the device mounting scheme was changed, and a significant improvement in microwave performance was achieved. With devices mounted in the new configuration, the microwave performance improved to the extent that it became relatively straightforward to design and build amplifiers that met the program goals.

Some of the major accomplishments that were made in this program include:

(1) Establishment of the materials growth and device fabrication capabilities required for the development of high power GaAs FETs.

(2) Development of a device mounting scheme that can be reproducibly achieved with high bonding yield and that gives state-of-the-art microwave performance.

(3) Achievement of high power performance at X-band with devices from many different epitaxial slices. At the completion of the program, nine slices had yielded devices that delivered 1 watt or more at 9 GHz with 4 dB gain.

(4) Attainment of the highest FET output power presently reported at X-band: 2.5 watts at 8 GHz with 4 dB gain and 25% power-added efficiency (4800 μm gate width).

(5) Development of a three-stage FET amplifier that exceeded the performance specifications. The amplifier delivers 360 mW of cw output power at 9.3 GHz. The gain is 20 ± 0.5 dB over the 9.1 to 9.8 frequency band, and the 3 dB bandwidth is 1.0 GHz.

(6) Development of a hybrid FET (three-stage)/IMPATT amplifier that meets the performance specifications. The amplifier delivers 1.2 W with 26 dB gain at 9.5 GHz with a 3 dB bandwidth of 9.1 to 9.8 GHz.

The remainder of this report is organized as follows. Device design is covered in Section II. Section III reports the details of the work on material growth and characterization. Device fabrication is discussed in Section IV. Section V describes device evaluation and includes a summary of the most significant microwave performance results. The microstrip amplifier development is covered in Section VI, and performance results are given in this section for the amplifiers that were delivered at the completion of the program. Finally, conclusions and recommendations are given in Section VII.

SECTION II

DEVICE DESIGN CONSIDERATIONS

In this section the basic physics of GaAs FET operation is described, and a discussion of the factors influencing the choice of the various device parameters is given. The values chosen for the present power FET design are enumerated.

A. Basic Structure, Device Physics, and Equivalent Circuit

To understand the operation of the GaAs FET, refer to the simplified sketch of the basic device structure shown in Figure 1. An n-type layer of uniform shallow donor doping N_d and thickness a is grown epitaxially on an insulating substrate. Ohmic "source" and "drain" contacts of width Z are placed as shown. Between them is a Schottky barrier "gate" of length ℓ. In normal operation the source is grounded and a positive voltage + V_{ds} is applied to the drain, causing current I_{ds} to flow from drain to source under the gate. The n-type GaAs under the gate is depleted of carriers in the Schottky barrier space-charge region, with a negative gate voltage V_g increasing the depletion depth. Thus, changes in gate voltage modulate the drain current I_{ds}. If V_g is large enough, the depletion region of the gate reaches the insulating substrate, and conduction is entirely "pinched off" ($|V_g| \equiv V_p$).

As V_{ds} increases with $V_g = 0$, I_{ds} increases linearly at first, and then saturates at a current I_{dss} beginning at a threshold voltage V_T. This saturation is caused by the forward drain bias effectively reverse-biasing the gate and pinching off the conducting channel. Also contributing to current saturation is the fact that at higher drain voltages the electrons are excited into the low mobility (100) conduction band minima, causing their velocity to saturate. The saturation current decreases as V_g is made more negative. In actual operation, the dc values of V_{ds} and V_g are fixed such that the device is biased into saturation, an rf signal is applied between the gate and source, and the amplified signal is available across the drain and source.

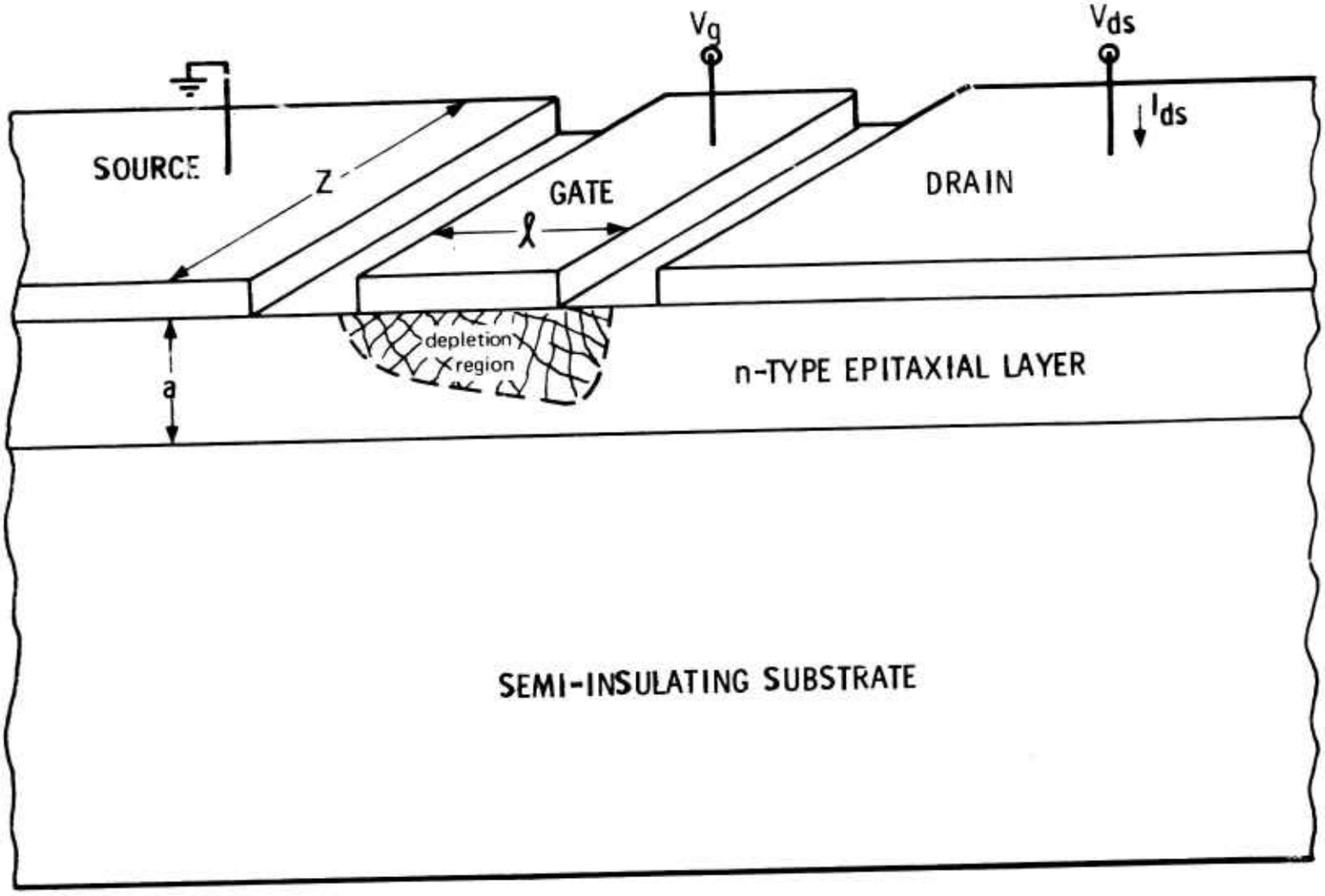


Figure 1 Simplified Sketch of the Basic GaAs FET Device Structure

One of the reasons the FET is superior to bipolar devices at high frequencies is that it is a majority carrier device. The response time is not limited by the charge storage capacitance of p-n junctions or long minority carrier diffusion times. The essential limitation is the charging of the Schottky barrier (fast compared to p-n junctions) and the electron transit time from source to drain. The transit time is very short, since the carriers are drifting rather than diffusing. Even relatively modest dimensions such as a 2 μm gate length and 6 μm source-drain spacing give a maximum frequency of oscillation of approximately 30 GHz. A 1/2 μm gate length device would have a maximum frequency of oscillation approaching 100 GHz. The major source of noise in a bipolar transistor is shot noise in the collector-base junction. This, of course, is not present with the FET, and very low noise operation is possible.

An equivalent circuit is often derived for active semiconductor devices to aid in impedance matching, analysis of microwave results, etc. The physical origin of the equivalent circuit elements for the GaAs FET is shown in Figure 2(a). The circuit itself is shown in Figure 2(b). In this figure R_g is the (parasitic) resistance of the gate metal; R_s is the (parasitic) source-gate (including contact) resistance; R_d is the (parasitic) drain-gate (including contact) resistance; V_a is the applied voltage and g_m is the device transconductance; C_{gs} is the gate-to-source capacitance (capacitance of gate depletion region); R_i is the resistance in series with the gate capacitance; C_{gd} is the drain-to-gate feedback capacitance; R is the reciprocal of the drain-to-source conductance; and C_{ds} is the drain-to-source capacitance. Because of the very low feedback capacitance C_{gd} and the high channel resistance R, the simple equivalent circuit shown in Figure 2(c) can be used for design calculations.

B. Device Parameter Selection

In GaAs power FET design, there are several constraints on the selection of device parameters, and trade-offs must be made between these constraints in

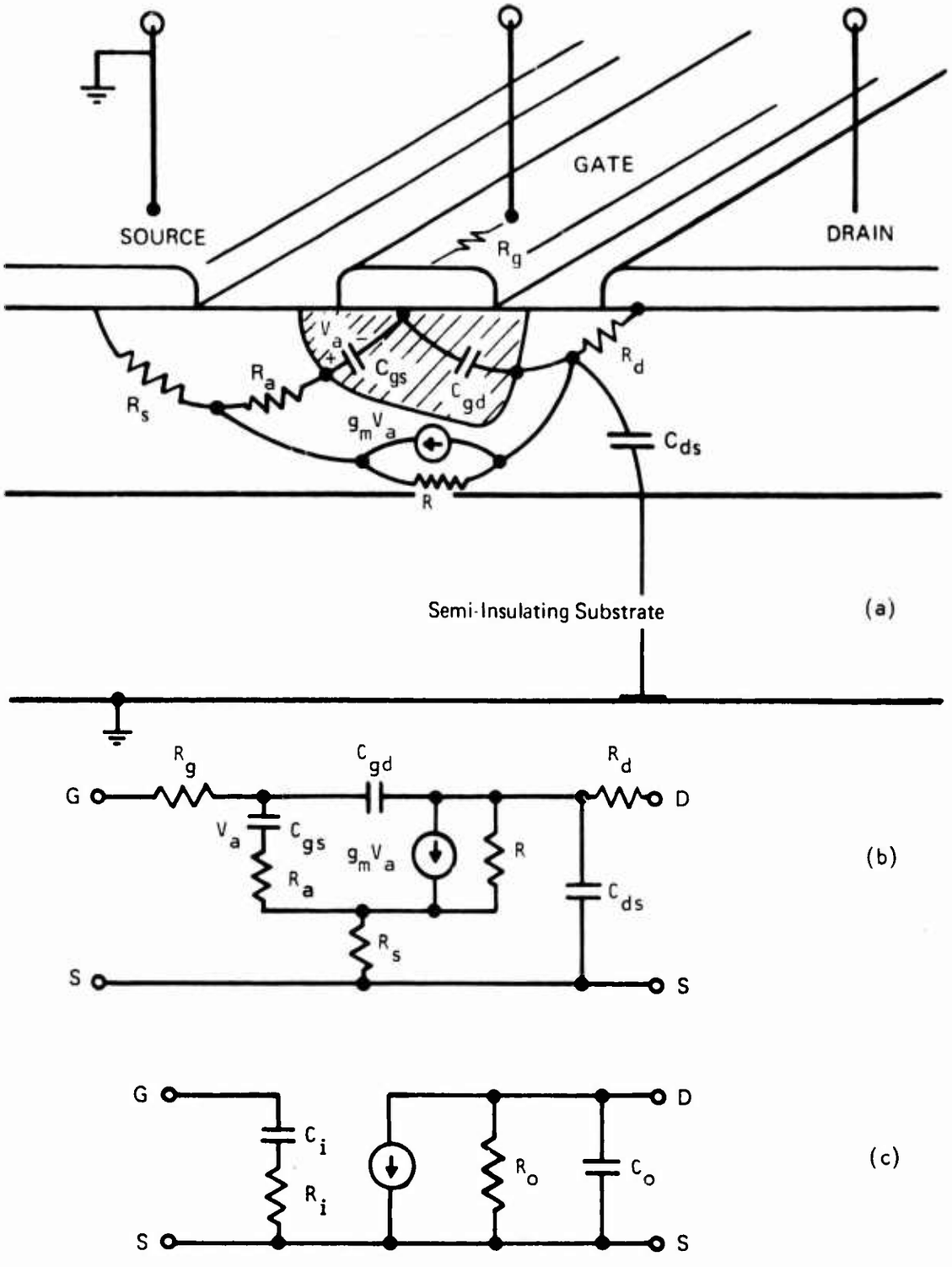


Figure 2 FET Lumped Microwave Equivalent Circuit. (a) Physical origin of circuit elements, (b) equivalent circuit, (c) simplified equivalent circuit.

arriving at an optimum device structure. The transconductance and maximum frequency of oscillation (f_{max}) increase with increasing carrier concentration, but the breakdown voltage and epitaxial thickness for a given pinch-off voltage decrease. Current-carrying capacity increases with epitaxial thickness, but consequent increasing pinch-off voltage results in higher operating voltages with resultant increased intervalley scattering noise.[1] In addition, the higher voltage may approach the breakdown voltage of the material. The net result of these considerations is that for high power X-band GaAs FETs, a donor concentration $N_d \sim 1 \times 10^{17}$ cm^{-3} and epitaxial thickness a ~ 0.3 μm ($V_p \sim 5V$) are employed.

Decreasing the gate length increases f_{max} and results in devices with higher gain and lower noise figure at a given frequency. In addition, the gate capacitance is decreased, making the input impedance easier to match. Shorter gate length devices are difficult to fabricate using conventional photolithography, however. A gate length of 2 μm has been chosen because it provides devices having useful gain at X-band without excessive photolithographic alignment problems.

Increasing the total gate width increases the device power-handling capability, but the increased gate-source capacitance and reduced real impedance [R_a of Figure 2(b)] make the input impedance more difficult to match. In addition, there is a reduced device yield with large gate widths due to gate breakage and shorting. The individual gate stripes must be short enough so that the attenuation and phase shift of a signal moving along the stripe (acting as an RC transmission line) is not significant. A longer gate stripe will require a thicker metallization for its resistance to remain unchanged. For X-band power amplification a total device gate width of 2400 μm has been chosen. An N_d and a above this gives a device current of several hundred milliamps under typical bias conditions, which corresponds to 2 to 5 W dc power dissipation at drain voltages low enough to prevent avalanche breakdown (V_{ds} = 5 to 10 V). This gives approximately 1 W rf output power if the drain efficiency is a

reasonable 20 to 40%. With a 2 μm gate length the real part of the input impedance is around 1 Ω, which can be matched with microstrip circuits. The gate fingers are 150 μm each, so a total of 16 are needed. These are contained in four independent cells, so if one is broken or shorted it is still possible to fabricate an 1800 μm gate width device from the three good cells.

The chip size must be small enough so that it is not a significant fraction of a wavelength at the operating frequency from one end to the other in order to prevent interference effects. A reasonable size is less than $\lambda/8 \cong 0.05$ inch at X-band (in GaAs). The device thickness must be small to facilitate heat transfer to the mounting block, but not so small that the chips break easily and are difficult to handle. Also, when the slice becomes too thin, the gate and drain bonding pad capacitances to the ground plane become excessive. The chip size used is 0.020 inch × 0.040 inch; the large dimension is close to the minimum possible with 0.003 inch wide source pads, since nine pads are needed to accommodate the 16 gate fingers. The device thickness chosen is approximately 0.004 inch.

The gate bonding pad capacitance to ground should be small relative to the gate capacitance; this requirement is usually satisfied by making the pad as small as possible, consistent with ease in bonding, and placing it on insulating material. Both gate and drain bonding pads are approximately 0.005 inch x 0.005 inch.

Finally, it is desirable to minimize the source-gate and gate-drain spacings and contact resistances, since these result in parasitic resistances in series with the active region that reduce gain and increase the noise figure. A source-drain separation of 6 μm was chosen, since it is the smallest compatible with ease in aligning the 2 μm gate.

SECTION III

MATERIALS GROWTH AND CHARACTERIZATION

Throughout the program, epitaxial GaAs structures have been supplied for FET device fabrication. Due to previous experience at Texas Instruments in the areas of Gunn, IMPATT, varactor, and multiplier diodes, the development of the FET materials growth technology has proceeded very rapidly. Work has been directed toward the growth of single-layer FET structures as well as multilayered structures where the buffer layer is introduced to remove the active layer from intimate contact with the substrate. As with most microwave devices, material is needed that has high mobility and a low degree of compensation. The remaining parts of this section describe the approaches used to obtain the desired structures.

A. Substrate Characterization

1. Specifications

Compared to other microwave devices, the FET structure is unique in that the epitaxial layer is grown on a high-resistivity substrate and the entire active layer may be only a few thousand angstroms thick. Therefore, the role of the substrate is a critical consideration in any successful device program. Throughout the program, the specifications to the substrate vendors have been as follows:

(1) Resistivity $> 10^7$ ohm-cm (chromium or chromium/oxygen doping)

(2) Etch pit density $< 10^4/cm^2$

(3) Minimum area > 1 $in.^2$/wafer

(4) Cut and polished on one side to 15 ± 1 mil.

2. Evaluation

When the wafers are received, a series of tests and inspections is carried out on random wafers from each crystal. The first inspection is merely

an optical examination of the polished surface to determine if any foreign matter or scratches are present that will degrade the quality. If no visible faults are observed, the wafers are placed in a sulfuric acid, hydrogen peroxide, water (8:1:1) mixture and etched for ten minutes. The wafers are again examined optically to determine the presence of any crystal degradation revealed by the 8:1:1 etch. If the results reveal no problem, the wafer is subjected to a third evaluation.

The purpose of the third test is to determine if there is any high temperature surface conversion on the wafer that will give rise to a thin (2000 to 4000 Å) conducting channel at the epitaxial layer/substrate interface. Obviously, this conversion would have a very negative effect on device performance. For this experiment the sample is heated in a hydrogen ambient at 800°C for two hours. After cool-down and removal of the wafer, a thin film of aluminum is evaporated on the surface and a pattern of annular rings is defined on the surface by standard photolithographic techniques. The resistance between rings is then measured to ensure that the original value, $> 10^7$ ohm-cm, is preserved.

This series of tests is applied to two or three wafers from each crystal, depending on ingot dimensions. If any test results prove negative, all the wafers from that crystal are rejected.

Wafers are selected at random from various crystals for confirmation of resistivity and etch pit density (epd). The resistivity is measured as described above, but without the heat treatment, and the epd is verified by using a molten KOH etch for 15 minutes. Once wafers of acceptable quality have been identified, epitaxial growth is the next step.

B. Epitaxial Growth

1. Growth Process

Epitaxial GaAs layers can be grown by either vapor phase or liquid phase techniques. For growth of FET structures, the vapor phase system is preferred because (1) high quality surfaces are routinely obtained; (2) the doping level can be adjusted by merely altering the gas phase dopant concentration, as opposed to saturation of a new melt; and (3) the process is capable of multislice deposition.

Of the possible vapor phase systems, the arsenic trichloride ($AsCl_3/Ga/H_2$) approach has emerged as the most successful for growth of microwave material. Epitaxial growth systems using $AsCl_3$ have been in use at Texas Instruments since 1964.

A schematic drawing of an $AsCl_3$ deposition system is shown in Figure 3. During the actual growth operation, palladium-diffused hydrogen is passed through an $AsCl_3$ saturator, and the resulting saturated gas stream enters the main reactor tube. Upon entering the hot zone upstream from the source, the $AsCl_3$ is reduced by hydrogen to form arsenic and hydrogen chloride. This mixture then passes over a boat filled with gallium, where the arsenic tends to dissolve until the source is saturated. When the gallium source becomes saturated, a crust of GaAs forms on the surface, and the necessary conditions for growth are established. With this saturated gallium, the following steady state reaction occurs at the source:

$$4\ HCl(g) + 4\ GaAs(s) \rightarrow 4\ GaCl(g) + 2\ H_2(g) + As_4(g). \qquad (1)$$

This mixture of gallium monochloride, hydrogen, and arsenic then passes into the deposition region, which is held at a lower temperature (750°C). There the thermodynamic equilibria are such that the reverse of the source reaction occurs, and

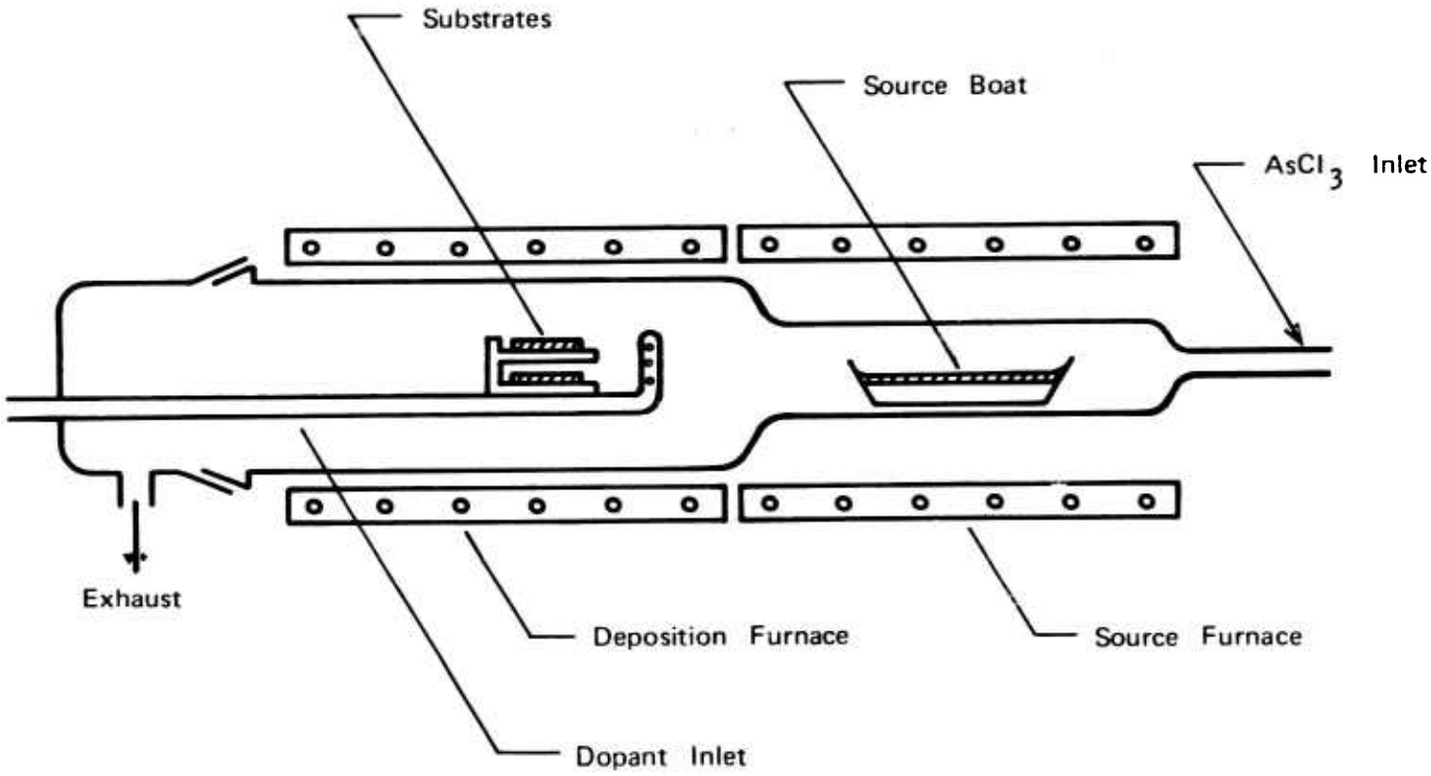


Figure 3 Schematic of Epitaxial Reactor

GaAs is epitaxially formed on the substrate. Figure 4 illustrates the epitaxial deposition system used for this program. Once the substrates are loaded into the reactor, this system functions in an automatic mode until growth is complete and the furnaces are returned to room temperature. The system can be used to grow sequential layers required in the multilayered structures.

2. Growth Procedure

The growth techniques used for FET structure are modifications of normal procedures used for growth of n-type layers on n^+ substrates. The alterations were necessary to grow very thin layers (2500 to 4000 Å) with high doping levels, approximately 1×10^{17} cm^{-3}, on semi-insulating substrates. The standard growth run begins with an *in situ* vapor etch followed by epitaxial growth. Some samples are grown with no vapor etch, thus minimizing the time necessary to establish steady state growth conditions. This procedure places stringent demands on wafer preparation prior to insertion of the wafer into the reactor. Samples of acceptable surface quality were grown by this procedure, optimized, and submitted for device processing. A second scheme that was tried is one in which the wafer is placed in a special seed holder so that the wafer is exposed to only a nongrowth atmosphere of hydrogen during the heating cycle and the establishment of steady state conditions. The wafer is positioned in the etching atmosphere only after steady state conditions are established. Following the etch portion of the run, the wafer is withdrawn into the hydrogen filled chamber until steady state growth conditions are established. Then it is removed from the hydrogen ambient and placed in the growth environment. This procedure was tried, again, in an effort to minimize epitaxial film growth in non-steady state conditions.

In addition to the above variations in growth procedures, a series of experiments to determine the optimum flow rate was made. Flows from 60 cc/minute to 200 cc/minute were used, and the resulting surface quality was evaluated. As

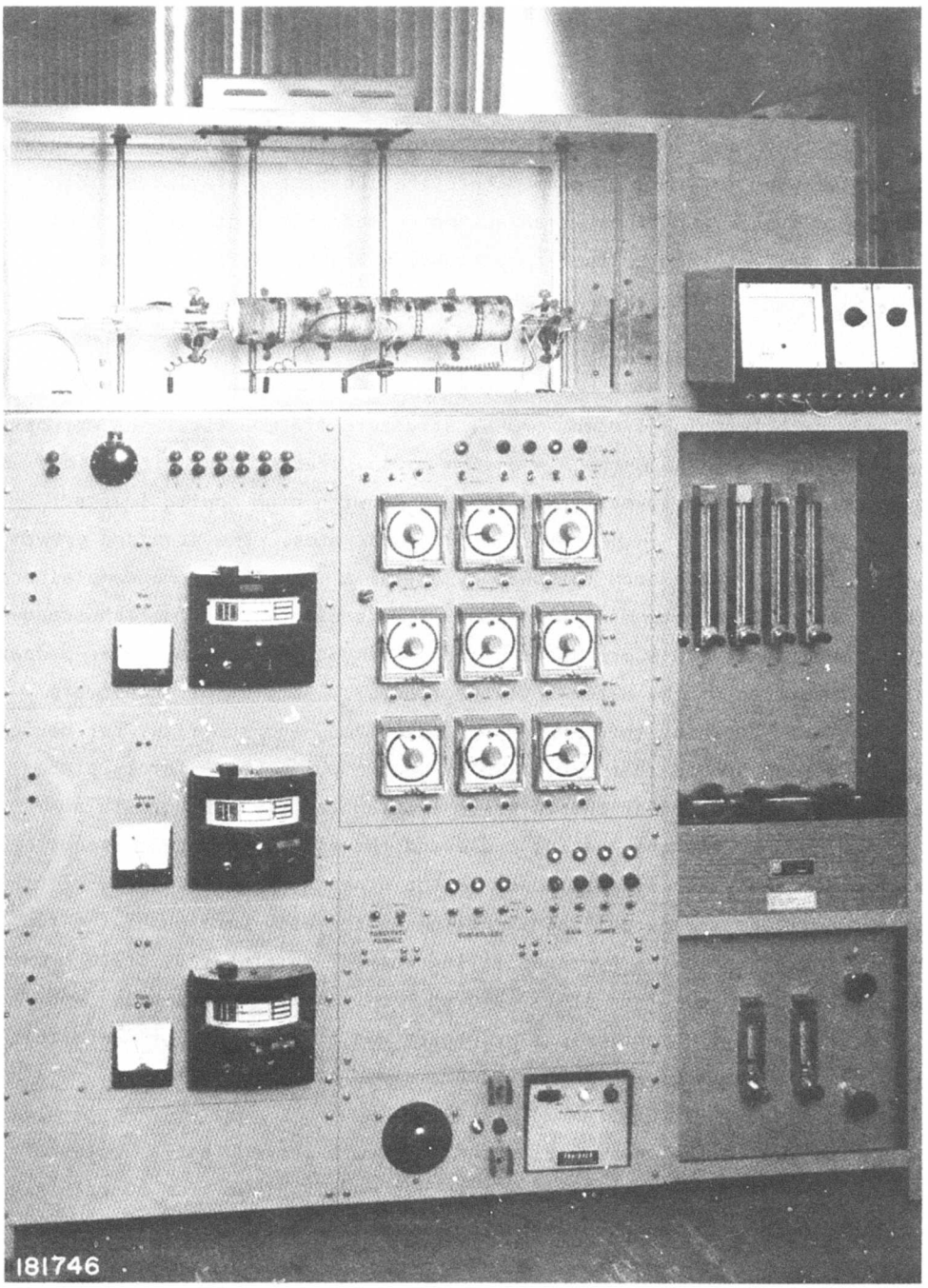


Figure 4 Automatic GaAs Epitaxial Reactor

the flows are increased from 60 cc/minute, the surface quality is observed to improve up to a flow rate of approximately 75 cc/minute. Beyond this point, degradation in surface quality is observed, with a flow rate of 120 cc/minute being the worst case. After passing through this minimum, the surface quality again improves, with flows of approximately 175 to 200 cc/minute giving surfaces superior to any other flow rate. This high rate is also optimum in the growth of the chromium-doped buffer layers to be discussed later in this section.

The influence of deposition temperature has also been investigated. Temperatures from 780°C to 740°C have been used for layer deposition. Within this range the surface quality as well as device performance show no correlation with deposition temperature.

3. Structures Grown

During the course of the program, the above discussed techniques were applied in the growth of four epitaxial structures: n-type layers on high resistivity, chromium-doped substrates; n-type layers on undoped buffer layers on chromium-doped substrates; n-type layers on chromium-doped buffer layers on chromium-doped substrates; and n-type layers on chromium-doped buffer layers on n-type substrates. The growth of single layers on high resistivity substrates was used extensively in the early portion of the program, both with and without vapor etching. In addition, layers were grown using the modified holder allowing for the hydrogen ambient during the establishment of steady state conditions. These single-layered structures were evaluated through device performance and found to demonstrate high power operation, > 1 W at 9 GHz with 4 dB gain.

Samples have also been grown using buffer layers, both undoped and chromium-doped. The role of the buffer layer is to enhance surface quality by

physically isolating the active n-type layer from the substrate, since the crystalline quality of the substrate is inferior to that of the epitaxial layer. The undoped buffer layers are grown from 1 to 5 μm thick with carrier concentrations corresponding to the background level of the reactor, 5 to 11 x $10^{14}/cm^3$. Sequential growth is achieved using the automatic system described previously. Following epitaxial optimization, devices fabricated from the wafers have been found to have high power performance, i.e., > 1 W at 9 GHz with 4 dB gain.

Samples grown with the chromium-doped buffer layers have not been as successful as the previously discussed material. The initial work with chromium-doped buffer layers was with the n^+/high resistivity buffer/high resistivity substrate structure. Chromium was introduced in the form of chromium oxychloride (chromyl chloride), CrO_2Cl_2, by the following high temperature reaction with hydrogen:

$$3\ CrO_2Cl_2 + 3\ H_2 \rightarrow CrO_3 \cdot Cr_2O_3 + 6\ HCl. \qquad (2)$$

The CrO_3 is further reduced by hydrogen,

$$CrO_3 + 3\ H_2 \rightarrow Cr + 3\ H_2O, \qquad (3)$$

and forms the chromium used as the acceptor necessary to produce semi-insulating material. Double epitaxial layers have been grown that have reverse breakdown values greater than 500 V for the buffer layer, indicative of high resistivity, and a top active layer with the desired carrier concentration, $N_d \sim 1 \times 10^{17}\ cm^{-3}$. A cleaved cross section of such a structure is shown in Figure 5. The role of the buffer layer is clearly demonstrated in this figure. As can be seen, a large nonuniformity existed in the substrate after vapor etching, but the imperfection is missing at the n-type/buffer layer interface, enhancing surface regularity.

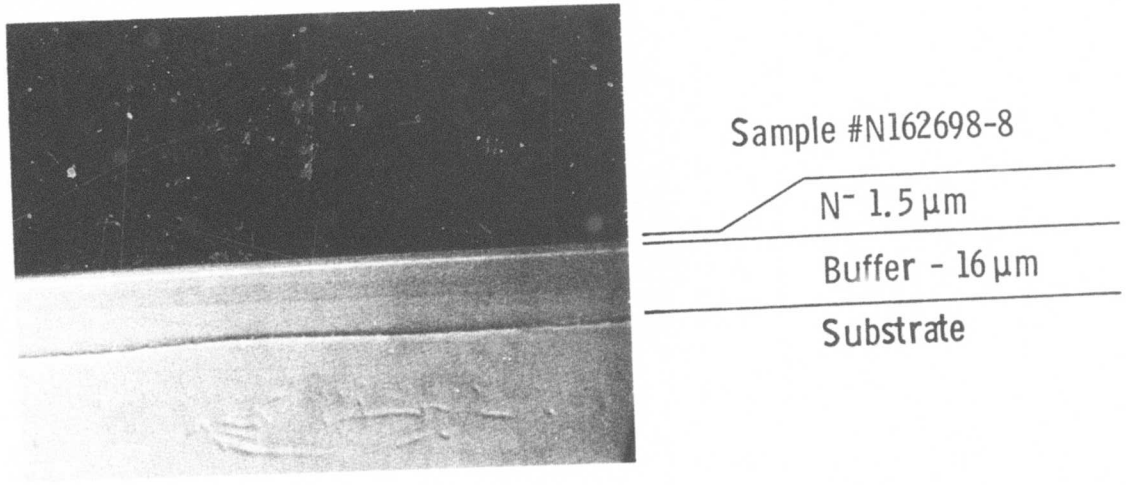


Figure 5 Cleaved and Etched Cross Section of FET Slice with Semi-Insulating Layer

Devices fabricated from these wafers have not demonstrated the same high level of performance as earlier structures. Possible reasons for the inferior performance are discussed in a subsequent portion of this section.

The final structure grown for use with the plated-through ground device scheme was the most difficult of the four. It consists of an n^+ layer and a high resistivity layer grown sequentially on an n^+ substrate. The insulating buffer layer is required in this case to isolate the source and drain. This situation was complicated by the fact that the substrate out-diffuses an n-type dopant, Te, that must be compensated by the Cr in different concentrations as the run progresses. By the end of the run, the concentration of n-type dopant is greatly reduced because the epitaxially grown layers have covered most of the n-type substrate. Following growth of the thick buffer layer (20 μm) the top n^+ layer is sequentially grown with a carrier concentration of approximately 1×10^{17} cm^{-3}. Of the many attempts to grow this structure, very few met all the desired parameters. Most samples were rejected because the resistivity in the buffer layer was too low or the quality of the surface was poor.

4. Characterization

Following growth of the various structures, the wafers are characterized in terms of thickness and carrier concentration. The thickness is measured optically on a cleaved and etched cross section of each wafer using conventional microscopy. The carrier concentration is measured by two techniques. One is the point contact method,[2] which is a quick and nondestructive evaluation technique that gives a close approximation of carrier concentration and a qualitative estimate of thickness for the very thin layers. As a verification for these values, random samples have been chosen on which aluminum is evaporated and the concentration determined by conventional C-V procedures. The agreement in the two methods is close in most cases.

5. Optimization

Following growth and characterization, samples are optimized if they are within specifications. The optimization technique consists of etching with a kinetically limited etch,[3] followed by anodic oxidation.[4] In all cases, samples are grown thicker than required for device work and then thinned. This post-growth thinning ensures that the Schottky barrier is fabricated not on the surface formed during growth termination, but rather under steady-state conditions. Since growth termination is not instantaneous, the final portion of the epitaxial layer would have a composition of other than steady state proportions. Optimization consists of thinning the layer with the kinetically limited etch until the point contact indicates the thickness is approaching optimum values for the carrier concentration of that wafer. The sample is then anodically oxidized until the final thickness is achieved. This self-limiting technique, through current limitation, results in a large-area wafer that has an optimum carrier concentration-thickness combination for device processing. Anodic oxidation can also be used to determine thickness uniformity of a sample by observing the color of the as-grown oxide and the number of oxidation steps necessary for optimization.

6. Discussion

A number of wafers have been grown from which transistors have been fabricated that have shown performances in excess of 1 W at 9 GHz with 4 dB gain. These wafers have been conventional single n^+ layers on high resistivity substrates or n^+ layers on undoped buffer layers on high resistivity substrates. Samples with chromium-doped buffer layers on n-type or high resistivity substrates produced less desirable results. It is believed that these latter two structures do not have the carrier concentration uniformities of the first two. This belief is based on the observation of the color scheme produced with the anodic oxidation procedure. On the successful structures, the anodically grown oxide follows a

definite orderly clearing pattern with optimization, while the oxide pattern on the samples with chromium-doped layers is very nonuniform in color across a wafer. For successful doping with $CrO_2C/2$, a great deal more effort must be spent in enhancing the uniformity of both carrier concentration and surface smoothness.

SECTION IV

DEVICE FABRICATION

The GaAs FET device design and fabrication processes continued to evolve throughout the course of the contract. The three planar device structures that were studied and the differences between them are briefly described. A non-planar structure is also discussed. A number of experimental studies were conducted to improve the device processing; these studies and their results are described. Finally, the current GaAs power FET fabrication process is examined.

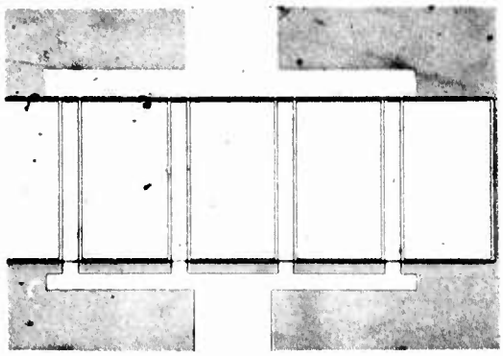
A. Review of Structures Investigated

The three planar device structures and the plated-through ground structure are described. In all cases gate lengths are nominally 2 μm; $N_d \sim 1 \times 10^{17}/cm^3$, and $V_p \sim 5$ V.

1. Planar Device Structures

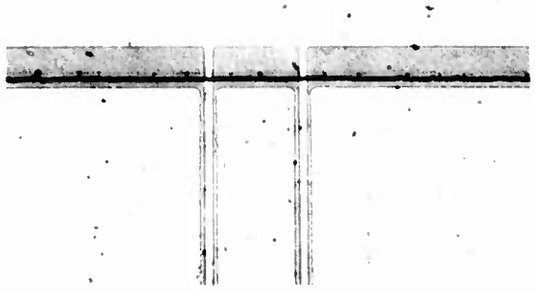
Photographs of the first structure studied are shown in Figure 6. The total gate width is 2000 μm in eight gate fingers (250 μm each), all of which are connected to a single gate bonding pad. Source pads are 0.005 inch wide. Half the devices on the slice have four gate fingers (1000 μm total gate width). Output powers were only 100 to 150 mW with 4 dB gain at 8 GHz from the 1000 μm gate width devices. Poorer output powers were obtained from the 2000 μm devices. This poor performance is partially the result of the high parasitic resistances present with the AgInGe ohmic contacts and nonrecessed gates then in use (see Section IV.B for a discussion of parasitic resistances).

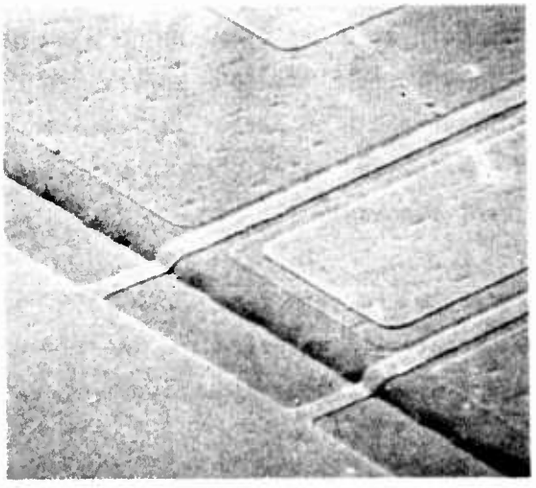
In an attempt to improve these results, the structure shown in Figure 7 was developed. There are 1200 μm and 2400 μm gate width devices on the slice. The masks were fabricated by electron beam definition, so a significant fraction of the slice is taken up by alignment marks. Individual gate stripes were



A) LOW MAGNIFICATION

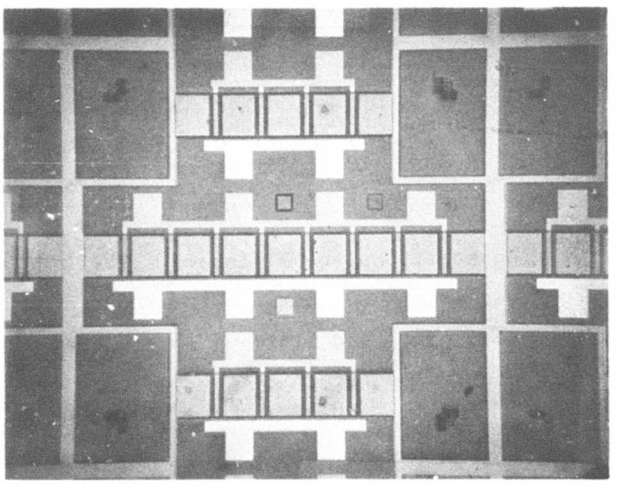
B) HIGHER MAGNIFICATION



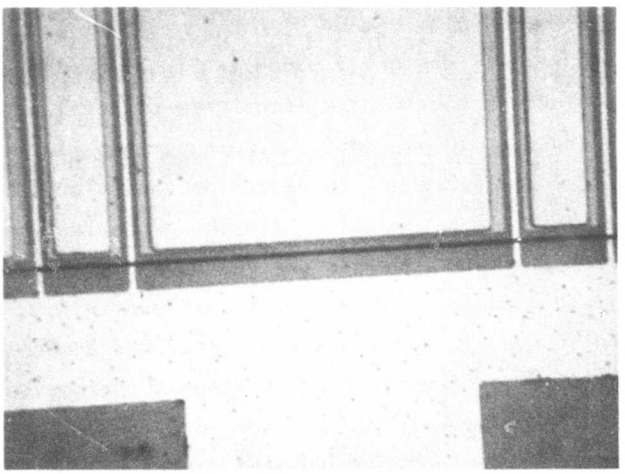


C) SEM PHOTOGRAPH

Figure 6 Photographs of 2000 μm Gate Width GaAs FET



(a) LOW MAGNIFICATION



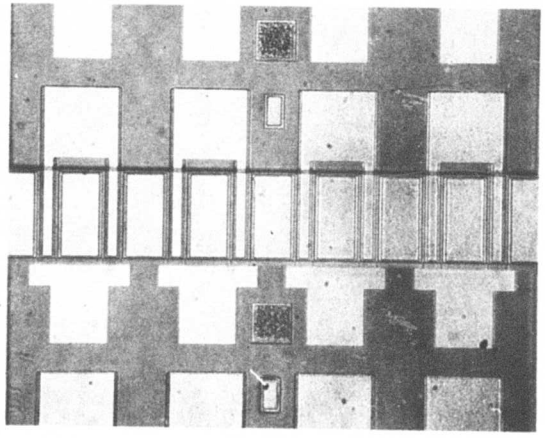
(b) ACTIVE AREA DETAIL

Figure 7 Photographs of 1200 μm and 2400 μm Gate Width GaAs FETs Fabricated from E-Beam Delineated Photomasks

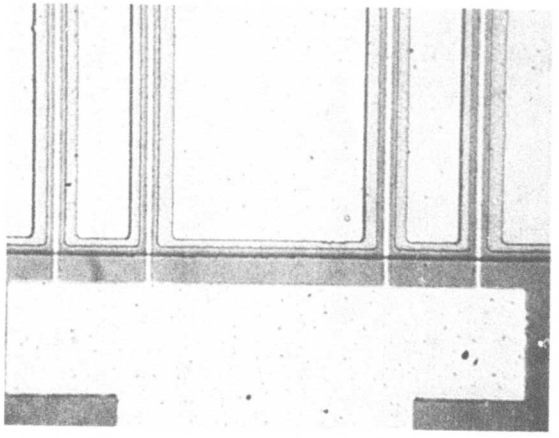
shortened to 150 μm, necessitating additional gate fingers. The 0.005 inch source pad width makes a large chip length (0.060 inch for 2400 μm gate width) necessary. The capability to recess gates and plate-up source pads is included, but all gate fingers are interconnected on the chip, giving a low yield of good devices.

1200 μm gate width devices of this design have reached a maximum of 300 mW output power at 9 GHz with 4 dB gain. Devices that have 2400 μm gate widths are no better, however. Most of the improvement over the previous design is probably due to reduction in parasitic resistance through use of recessed gates and AuGe/Ni ohmic contacts.

The current GaAs power FET design is shown in Figure 8. Total gate width is still 2400 μm contained in four 600 μm (four gate stripes) cells, but source pad width has been reduced to 0.003 inch, allowing a chip width reduction to 0.040 inch. The individual cells are not connected on the slice (connections are made with bond wires), which, in conjunction with the higher device packing density, provides a much higher yield of usable devices having at least 1200 μm gate width. This higher yield, coupled with the fact that one in four chips is made up of test patterns (discussed in Section V.A.1), provides a much greater capability for studying the effects of various processing, mounting, bonding, etc., changes. When mounted on ceramic substrates (as were the two previous device types), 1200 μm gate width devices from several slices have had output powers of 300 to 400 mW at 9 GHz with 4 dB gain. Devices with 1800 μm and 2400 μm gate widths are slightly better. These improvements over the previous design are partly due to deeper gate recession and smaller chip size (a smaller fraction of a wavelength from one end to the other). As discussed in Section V.B.2, the mounting of these latest GaAs FETs directly to Cu blocks instead of alumina substrates has resulted in a further multiplication of the output power by a factor of 2 to 3.



Overview



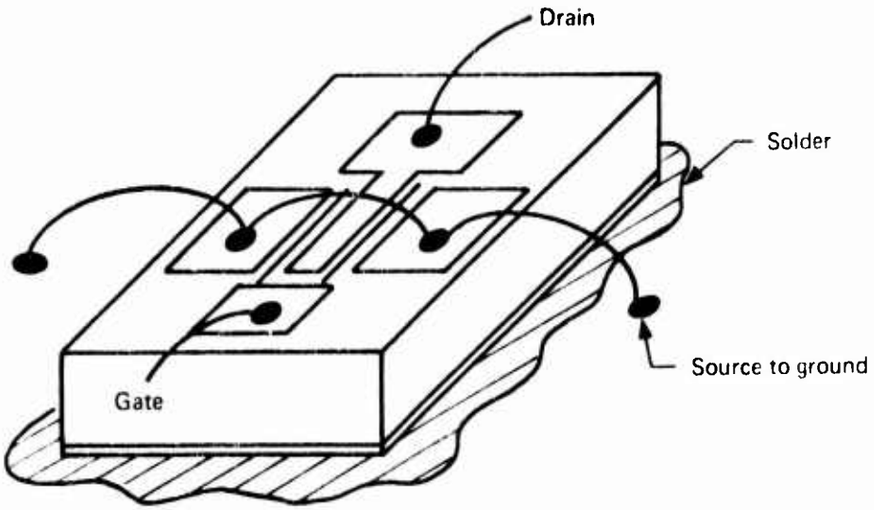
Gate Region

Figure 8 Four-Cell GaAs Power FET

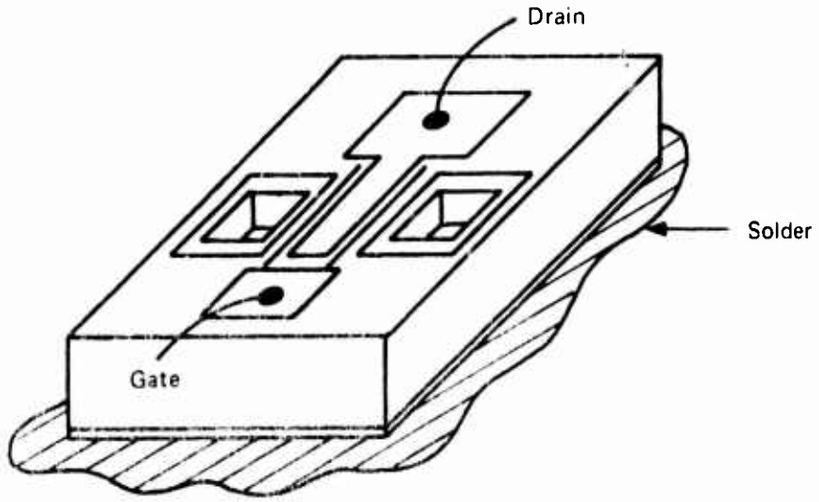
2. Nonplanar Device Structure

It was originally thought that a major limitation on GaAs power FET performance would be the inductance of the bond leads interconnecting the multiple source pads. For this reason the design of Figure 9 was devised. In this design the source pads are interconnected through an n^+ substrate. A schematic cross section of the slice is shown in Figure 10. A high resistivity buffer layer and an n-type active layer are grown on an n^+ substrate, as described in Section III.B.3. Holes are etched through the buffer layer to the substrate, and electrical connections are made by metallization in the holes plated through ground. No source leads are necessary, and very low inductance contacts are possible. The high resistivity buffer layer should be at least 20 μm thick to prevent excessive gate and drain bonding pad capacitance.

Figure 11 is a photograph of such a structure with a 20 μm Cr-doped buffer layer. The problem encountered is that as the holes are etched, they become wider at the top, and for a 20 μm depth they approach the edges of a 0.005 inch wide source pad. If the high resistivity layer is made thinner, the gate and drain pad capacitances become excessively large; and if the source pads are made wider to permit deeper holes, the chip size becomes too large for a gate width of more than about 1200 μm (eight gate stripes). The device of Figure 11 is a compromise with the holes etched as deeply as possible (about 20 μm). The source pads are interconnected, but since the hole depth is about the same as the buffer layer thickness, the resistance of the connection is excessive. This causes the current to saturate at ~ 3.5 V instead of the 2 to 2.5 V typical of planar devices and results in 1 to 2 dB lower microwave gain than with a comparable planar device under the same conditions. Because of the difficulty in making a low resistance interconnection and the additional difficulty of growing a high quality high resistance buffer layer, this idea has been abondoned in favor of the planar approach. As discussed in Section V.B.2, source lead inductance is not now thought to be a significant problem with GaAs power FETs.



A) conventional bonding



b) Plated through ground sources

Figure 9 Double-Source FET with Conventional Bond Wires to Ground Compared with Plated-Through Interconnected Source Grounding

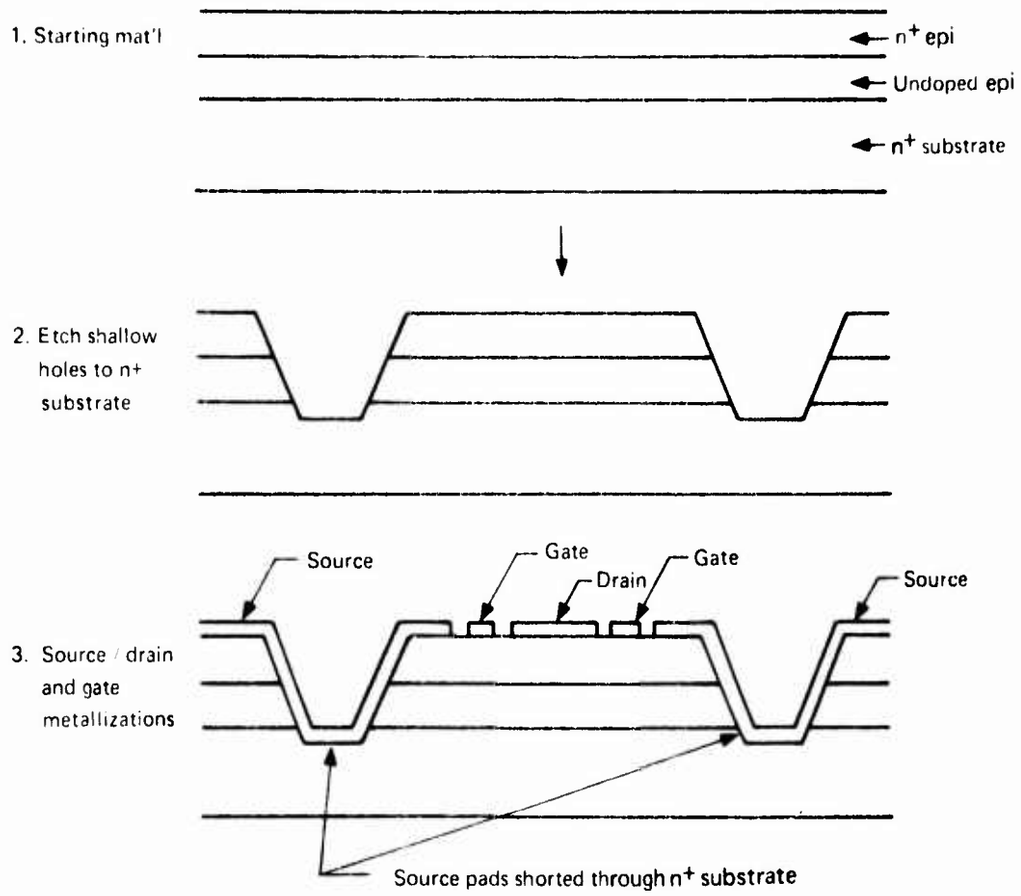


Figure 10 Schematic Cross Section of Structure for Plated-Through Ground Source Interconnection

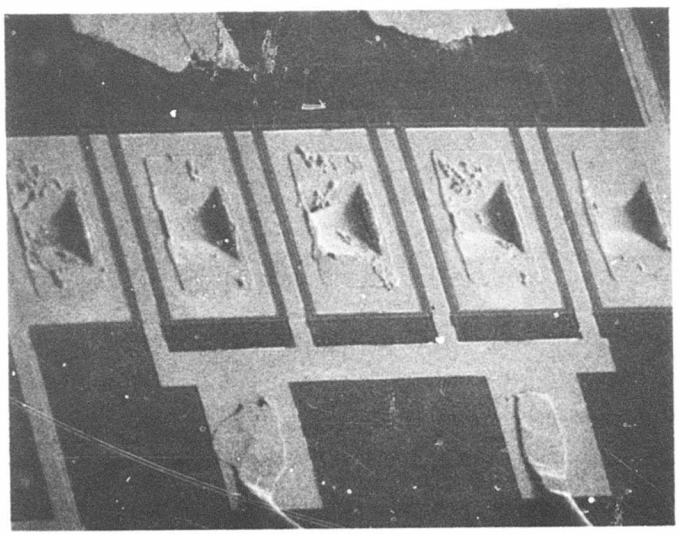


Figure 11 Plated-Through Ground Source Pad Interconnection

B. Process Studies

It is extremely important that all parasitic resistances be reduced to the lowest possible values. It is also important that the gate metallization be reliable (Schottky barrier properties do not change with time) and of sufficient thickness to prevent excessive attenuation of the input rf signal. The experiments leading to the improvement of these parameters are described in this subsection.

1. Ohmic Contacts

Operation of GaAs FETs at high power levels requires very low resistance ohmic contacts. Excessive contact resistance seriously degrades the device transconductance and thus the rf gain. Because the ohmic contacts are fabricated in an n-type layer on a semi-insulating substrate, the conventional contact resistance measurement technique[5] is not applicable, and a different scheme must be employed. Three contacts with separations ℓ and 2ℓ (where $\ell \simeq 3\ \mu m$) are fabricated as shown in Figure 12. They are placed on a mesa of width Z (or are cleaved to that width) so that all the electric field lines will be straight lines perpendicular to the contact edges. The resistance of the n-type layer between contacts 1 and 2 is then found by simply treating it as a resistor of resistivity, ρ, length, ℓ, and area, Za. The contacts are fabricated exactly as with the actual devices and are overcoated with Au to spread the current evenly across the contact width.

When the resistance between two contacts is measured, it is made up of three components: the resistance of each contact, R_c; the resistance of each probe, R_p; and the resistance of the n-type layer, R (length ℓ) or $R' = 2R$ (length 2ℓ). Define R_{ab} as the measured resistance between contacts a and b. Then

$$R_{12} = 2\,R_c + 2\,R_p + R \tag{4}$$

$$R_{23} = 2\,R_c + 2\,R_p + 2\,R. \tag{5}$$

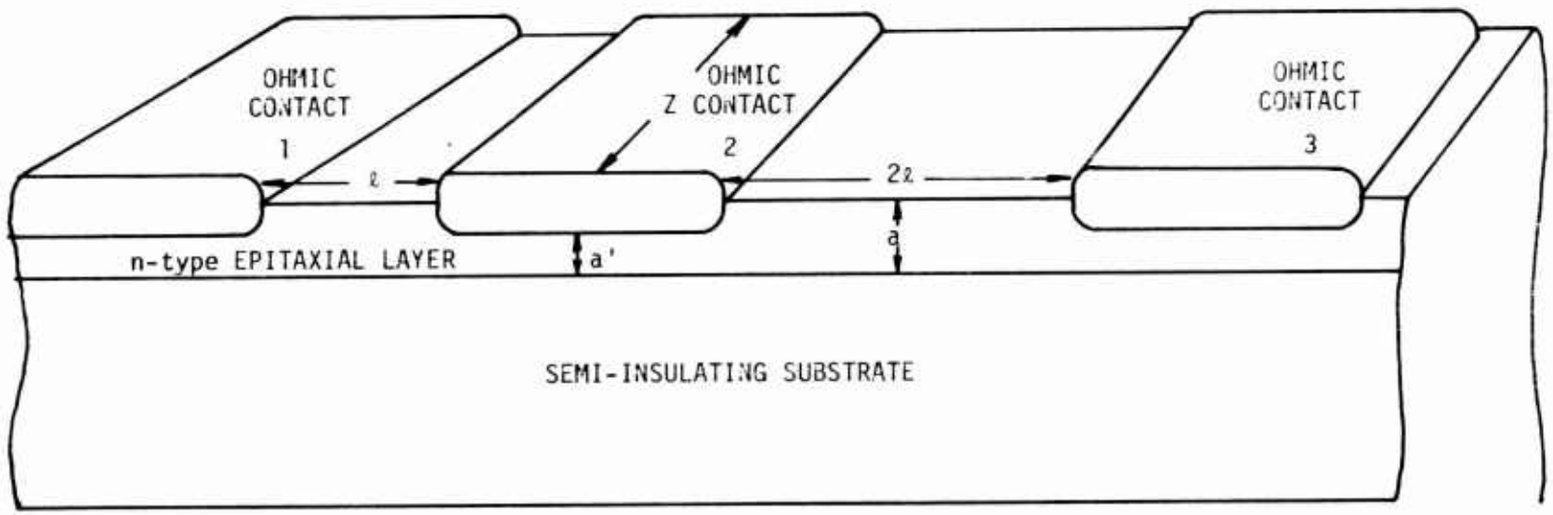


Figure 12 Contact Resistance Measurement Geometry

By subtracting R_{23} from 2 R_{12}, the resistance of the n-type layer is eliminated (assuming ρ and a are uniform), and one has

$$R_c \left(\frac{\Omega}{\text{mm gate width}}\right) = \left[\frac{2R_{12} - R_{23}}{2} - R_p\right]\left[\frac{Z(\text{mm})}{1\ \text{mm}}\right] \quad . \tag{6}$$

Rather than use probes for which R_p can depend on probe pressure, wires are bonded to each contact and R_p can be measured by bonding two wires to the same contact.

During the contact alloying process, the alloy depth is not known (a' in Figure 12 is unknown) so the specific contact resistance, r_c (in Ω-cm^2), in general cannot be calculated exactly. The resistance in Ω/mm gate width is therefore used to compare different samples. It can be shown that the contact resistance is given by

$$R_c = \frac{1}{Z}\sqrt{\frac{r_c \rho}{a'}} \quad , \tag{7}$$

where ρ = GaAs resistivity, and in two cases (where a' is known) r_c can be determined from the measured values of R_c. The two cases are a' = a (no alloy penetration into the GaAs) and penetration to the substrate. In these cases one has

$$r_c = \frac{R_c^2 Z^2 a}{\rho} \qquad a' = a \tag{8}$$

$$r_c = R_c Z a \qquad a' = 0. \tag{9}$$

Calculation of r_c in these limits allows some comparison with the results of others. When R_c becomes very small, the calculated values of r_c for these two cases are not drastically different in the range of Z, a, and ρ employed for GaAs FETs.

The contact resistance has been measured for AgInGe, AuGe, and AuGe/Ni alloyed contacts on several different slices. The AgInGe contact[5] (90 weight % Ag, 5% In, 5% Ge) was initially used because of its very sharp edge definition compared to AuGe, which balls up significantly when alloyed. The AgInGe contact is alloyed for five seconds at 600°C in flowing Ar. More recently, eutectic composition AuGe with a 200 to 400 Å Ni overcoat[6] has become the standard GaAs FET ohmic contact in this laboratory. These contacts have an edge definition as sharp as that of AgInGe contacts, and significantly lower resistance. Robinson has shown[7] that when the AuGe/Ni is heated, the Ni diffuses through the AuGe to the AuGe-GaAs interface, increasing the wetability and giving a much more uniform alloy. The contact resistance results are shown in Table 1. The improvement is clearly apparent: the contact resistance using AgInGe is around 2 to 3 Ω/mm gate width, while with the AuGe/Ni it is in the 0.3 Ω/mm gate width range. The values of R_c may be uncertain by a factor of two due to variations in epitaxial thickness, probe resistance, measurement of contact separations, etc. As will be shown shortly, changing from 2 to 3 Ω to 0.3 Ω is a reduction from the same order as the channel resistance to a small fraction of that resistance. Although the specific contact resistance is not precisely known, since a' (Figure 12) is not known, it is approximately 1×10^{-6} for the AuGe/Ni contacts.

When a slice is cleaved into two portions and the devices on one piece are fabricated with AuGe/Ni contacts with the others having AgInGe, the superiority of the AuGe/Ni is clear. As shown in Figure 13, the saturation voltage is 2.5 V for devices with AuGe/Ni contacts as opposed to 3.0 V for identical devices with the AgInGe. The rf performance is similarly improved; devices with the AuGe/Ni have about 1 dB more gain at a given input power level and bias condition than identical devices with AgInGe contacts.

Table 1

MEASURED CONTACT RESISTANCE FOR DIFFERENT OHMIC CONTACT ALLOYS

Slice No.	Run No.	Ohmic Contact Alloy	Contact Resistance R_c (Ω/mm gate width)	a (μm)	SPECIFIC CONTACT RESISTANCE r_c (Ω-cm^2) a′ = a (Very thin alloyed region)	a′ = 0 (Alloyed down to substrate)
1	A	AuGe/Ni	0.32	0.3	2.1×10^{-6}	0.96×10^{-6}
2	A	AgInGe	2.9	0.3	1.4×10^{-3}	8.7×10^{-6}
3	A	AuGe/Ni	0.62	0.25	3.8×10^{-6}	1.5×10^{-6}
4	A	AuGe/Ni	0.21	0.35	6.2×10^{-7}	7.4×10^{-7}
	B	AuGe/Ni	0.16	0.35	3.6×10^{-7}	5.6×10^{-7}
	C	AgInGe	2.8	0.35	1.10×10^{-4}	1.0×10^{-5}
	D	AgInGe	3.0	0.35	1.26×10^{-4}	1.05×10^{-5}
	E	AgInGe	1.5	0.35	3.1×10^{-5}	5.3×10^{-6}
5	A	AuGe	6.1	0.25	1.0×10^{-3}	1.8×10^{-5}

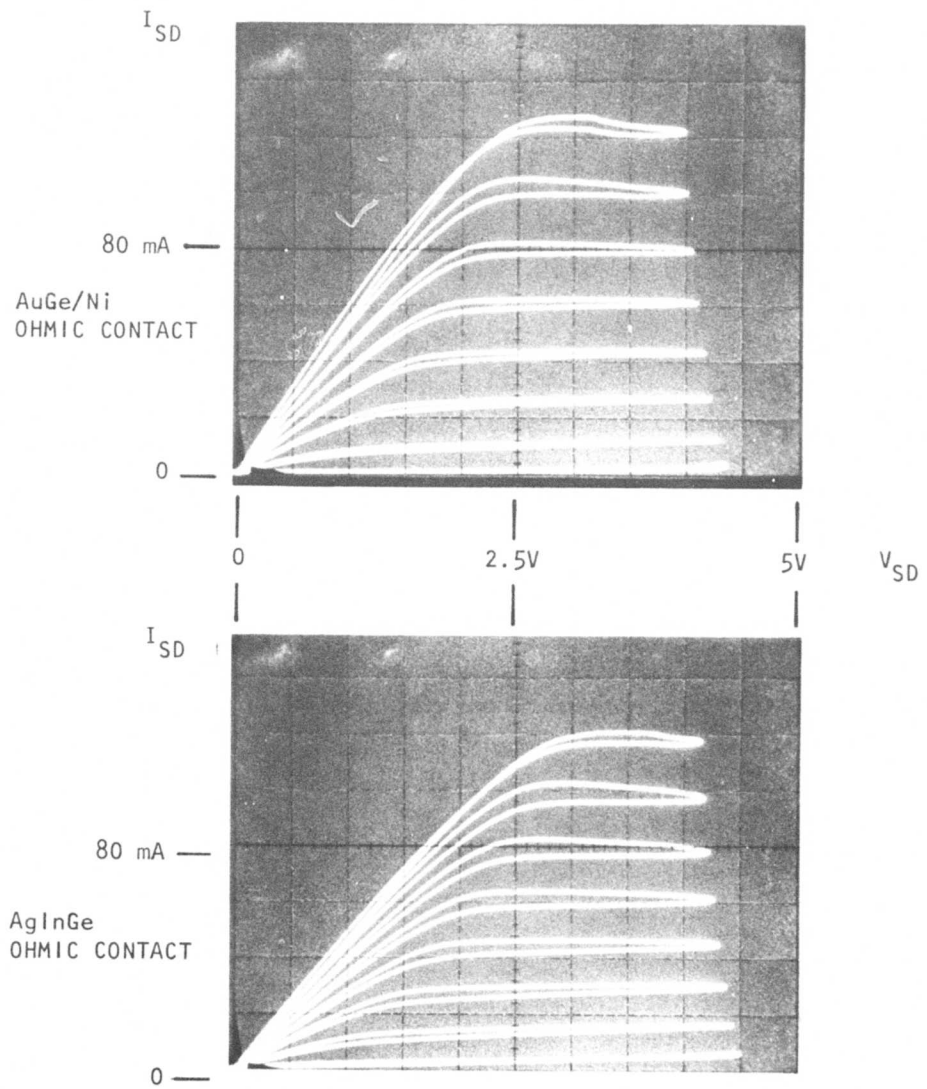


Figure 13 Comparison of Current-Voltage Characteristics of Devices Having AuGe/Ni Ohmic Contacts and AgInGe Ohmic Contacts. 20 mA/vertical division, 0.5 V/horizontal division, 1 V/step, 300 μm gate width.

2. Recessed Gate

The ohmic contact is not the only source of parasitic resistance; the regions between the source and gate, R_{sg}, and drain and gate, R_{dg} also act as parasitic resistances and, being of the same dimensions as the active area under the gate, make a significant contribution to the total resistance. When the contact resistance is very low, as with AuGe/Ni, the contribution from these regions may be as much as 2/3 of the total parasitic resistance. One way to significantly reduce the contribution of these parasitic regions is to recess the gate below the epitaxial surface as shown in Figure 14, thus permitting a thicker epitaxial layer for the same pinch-off voltage. Since the resistance of the (source-gate) parasitic region is now $R_{sg}' = \rho \ell_{sg}/Za'$ instead of $R_{sg} = \rho \ell_{sg}/Za$, it is decreased since $a' = a +$ recess depth. The recess depths achieved have been in the range from 500 to 2500 Å, which can lead to as much as 50% reduction in the parasitic resistance. The improvement is not only in the parasitic GaAs resistance; an increase in the epitaxial layer thickness also reduces the contact resistance since it changes from

$$R_c = \frac{1}{Z}\sqrt{\frac{r_c \rho}{b}}$$

to

$$R_c' = \frac{1}{Z}\sqrt{\frac{r_c \rho}{b'}},$$

where $b' = b +$ recess depth, and $r_c =$ specific contact resistance in $\Omega - cm^2$.

Devices fabricated on two halves of the same slice with AuGe/Ni ohmic contacts have shown no difference between them except that one has a slightly thicker epitaxial layer. The gate has been recessed about 0.07 μm on the slice with the thicker epitaxial layer, which gives devices on both slices the same

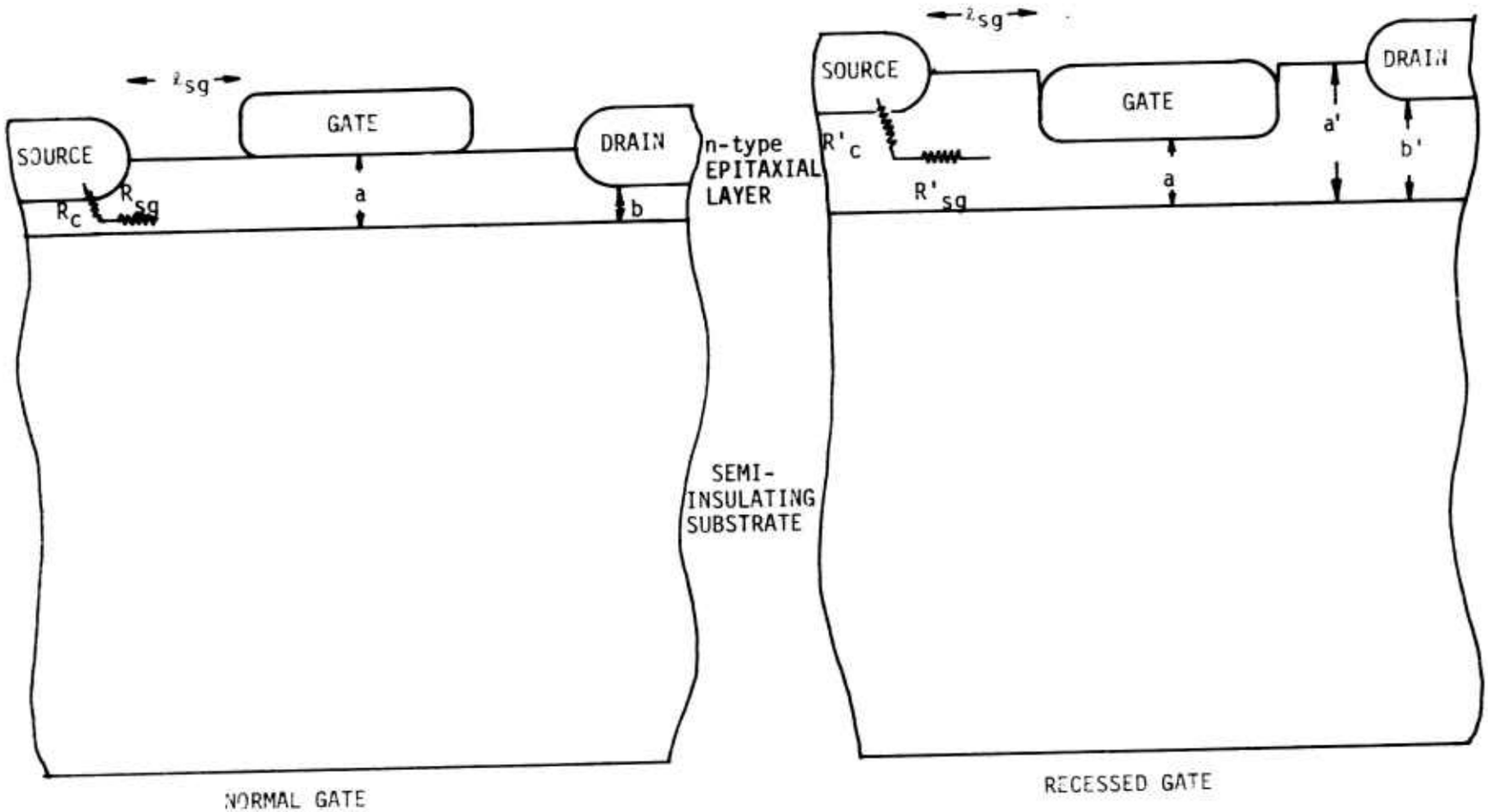


Figure 14 Effect of Recessing the Gate on Parasitic Resistance

pinch-off voltage. Figure 15 compares the I-V characteristics of devices from the two slices. The saturation voltage of the devices with the recessed gate is only 2.3 V, while for the others it is 2.6 V. There is a similar improvement in the relative microwave performance of the devices; devices with recessed gates have approximately 1 dB higher gain than those without under the same operating conditions.

3. Channel Conductance

One of the better devices studied is analyzed in detail to show the numerical contributions of the various parasitic resistances. The I-V characteristic is shown in Figure 16. The source and drain ohmic contacts are AuGe/Ni, and the gate is recessed 1500 Å.

One way to determine the parasitic resistance has been described by Hower and Bechtel[8] and makes use of the fact that when the drain current is zero, the small signal source-drain resistance is given by

$$R_{ds} = R_{parasitic} + \frac{1}{G_o(1 - \sqrt{\eta})} , \qquad (10)$$

where G_o is the open channel conductance and $\eta \equiv (-V_{gs} + V_B)/(V_p + V_B)$. V_B is the Schottky barrier height at zero bias (approximately 0.7 V for Aℓ), and V_p is the pinch-off voltage (approximately 5.5 V for this device). The donor concentration, N_d, is measured to be 1×10^{17} cm^{-3} from the Schottky barrier capacitance at zero bias. When R_{ds} measured near zero drain bias is plotted as a function of $1/(1 - \sqrt{\eta})$ as in Figure 17, the extension to $1/(1 - \sqrt{\eta}) = 0$ gives the parasitic resistance, which is shown here to be 2.4 Ω. If the epitaxial layer had a uniform carrier concentration and mobility, the graph would be a straight line; since its slope increases with gate bias, V_{gs}, the $N_d \mu$ product for this slice decreases as the substrate is approached. The point labeled

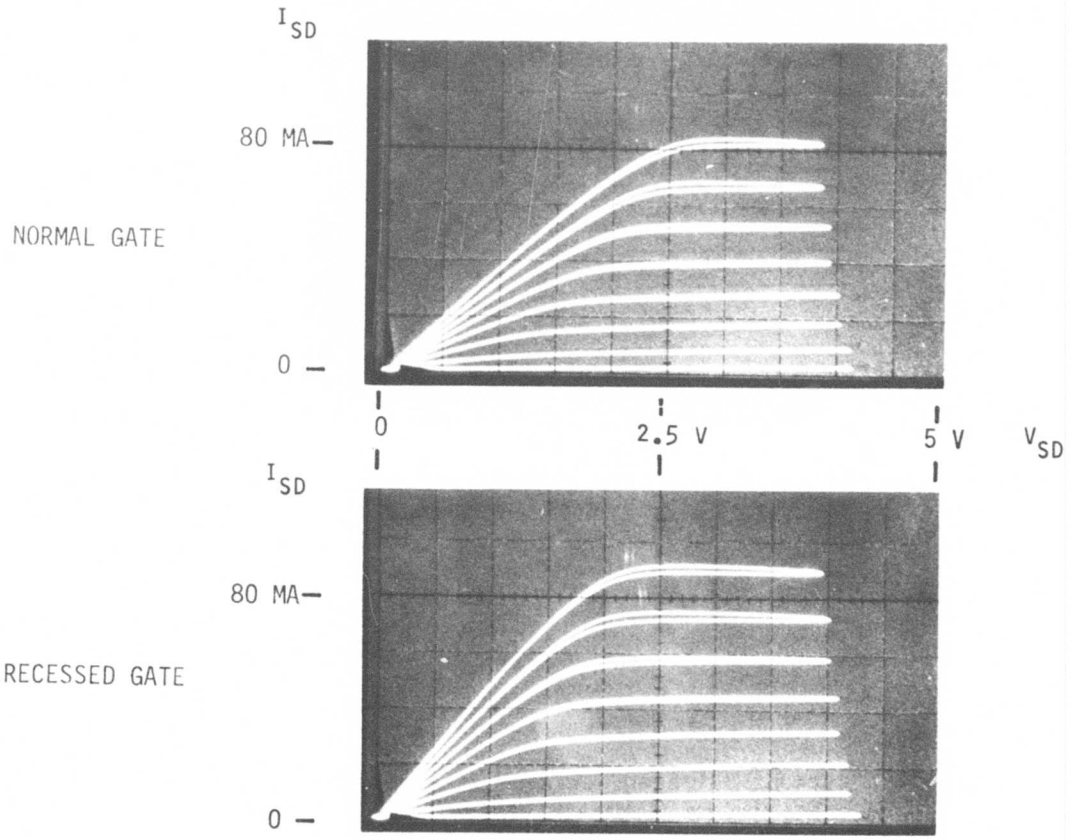


Figure 15 Effect of Recessing the Gate on I-V Characteristic; 20 mA/Vertical Division, 0.5 V/Horizontal Division, 1 V/Step, 300 μm Gate Width.

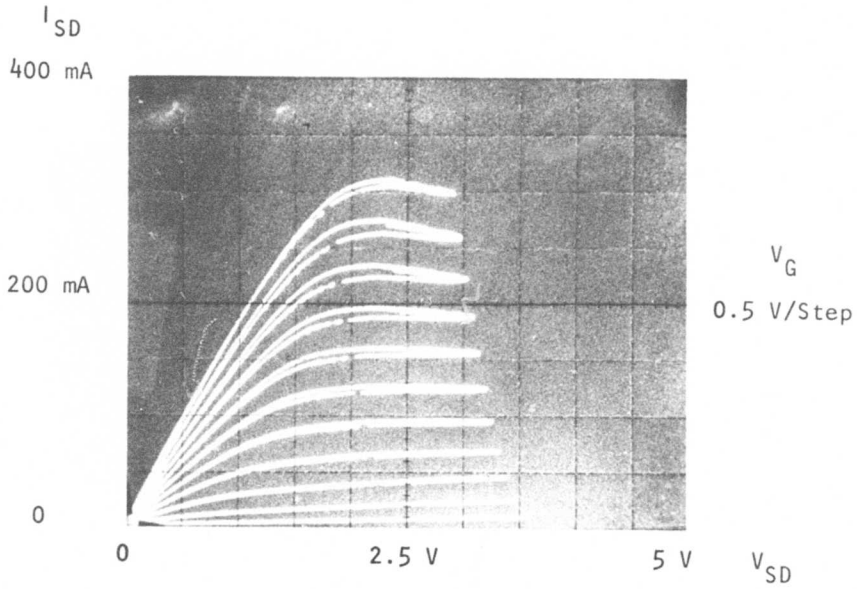


Figure 16 Current-Voltage Characteristic of GaAs FET Having a Total Gate Width of 1200 μm. Gate length is ℓ = 2.4 μm and source-drain spacing is ℓ_{sd} = 5.9 μm.

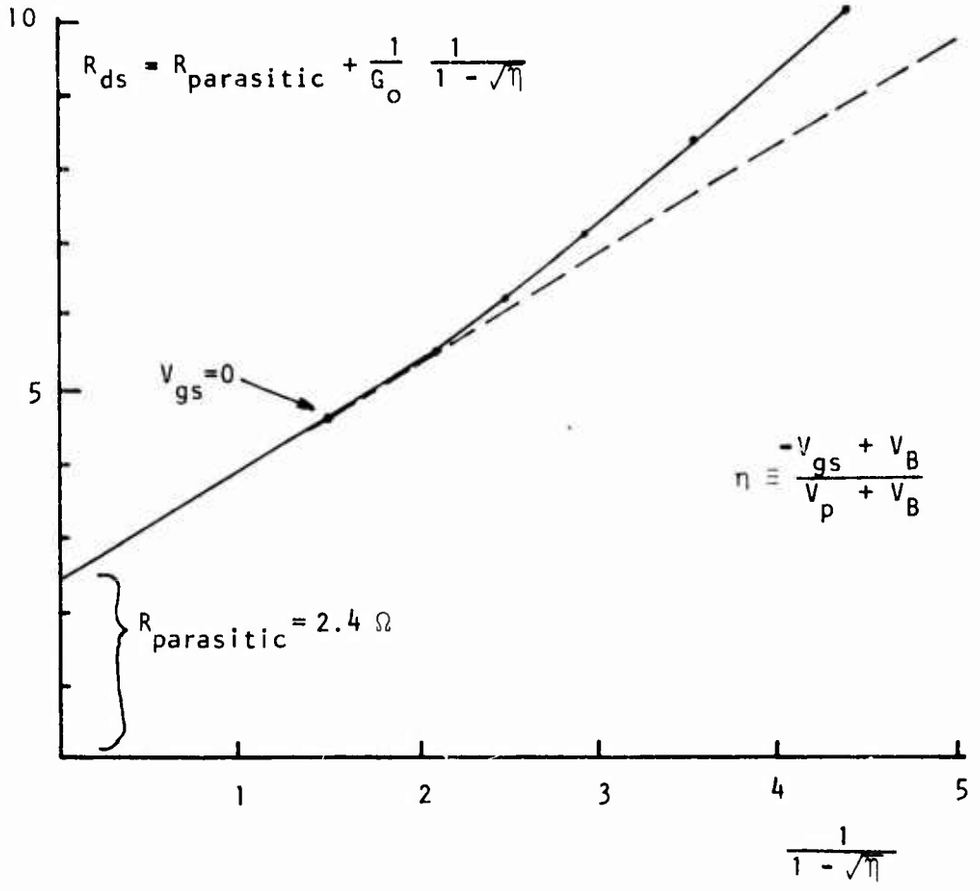


Figure 17 Analysis of Elements Contributing to Source-Drain Resistance of GaAs FET of Figure 16

$V_{gs} = 0$ shows that with zero gate bias the resistance between source and drain near zero drain current is 4.6 Ω, giving a channel resistance of 4.6 Ω - 2.4 Ω = 2.2 Ω.

The epitaxial thickness under the gate is

$$a = \sqrt{\frac{2\epsilon\ (V_p + V_B)}{qN_d}} = 0.29\ \mu m. \tag{11}$$

The epitaxial thickness in the parasitic regions is a' = a + recessed depth = 0.44 μm. The resistivity may be obtained from

$$\rho = \frac{E_{crit}\ Z(a - 0.1\ \mu m)}{I} = 0.0188\ \Omega\text{-cm}\ , \tag{12}$$

where I is the saturated current with the gate unbiased and $E_{crit} = 3.3 \times 10^3$ V/cm. In (12), a - 0.1 μm = 0.19 μm is used because current does not flow through the 0.1 μm Schottky barrier depletion region. The resistance of the channel can be calculated from ρ and a above and ℓ in Figure 16:

$$R_{channel} = \frac{\rho\ell}{Z(a - 0.1\ \mu m)} = 2.0\ \Omega, \tag{13}$$

which is similar to the 2.2 Ω found with Figure 17. The source-gate and drain-gate resistances can also be calculated using ρ and a' above and ℓ_{sd} from Figure 16:

$$R_{sg} + R_{dg} = \frac{\rho(\ell_{sd} - \ell)}{Z\ (a' - 0.1\ \mu m)} = 1.6\ \Omega. \tag{14}$$

For this device, the contact resistance was measured to be $R_c = 0.3\ \Omega$, and the resistance of bond wires, TC bonds, striplines, etc., contributed

another 0.3 Ω (measured with two wires bonded to the same pad). The total of these parasitic resistances $R_{sg} + R_{dg} + 2R_c + 0.3\ \Omega = 1.6\ \Omega + 0.6\ \Omega + 0.3\ \Omega = 2.5\ \Omega$ is close to the 2.4 Ω of Figure 17. One can see that the actual active channel resistance is less than half of the total measured source-drain resistance, and the majority of the parasitic resistance comes from the source-gate and drain-gate regions.

4. Schottky Gate Metallization

Both Aℓ and Cr/Au Schottky barriers have been employed as GaAs FET gate metallizations in this laboratory. Aluminum is used exclusively at present because CrAu has been found to react with the GaAs when heated to 300 to 350°C. After heating to this temperature for 20 minutes, there is an obvious change in the appearance of the Cr/Au, with the surface growing more bumpy. As shown in Figure 18, the reverse saturation current of the Schottky barrier also increases drastically while that of the aluminum barriers increases relatively little, remaining less than 1 μA (for an 8 mil dot) after a two-hour 450°C anneal. These results are similar to those reported by Kim, et al.[9]

5. Gate Finger Width

To determine the thickness of gate metallization that is necessary to prevent attenuation of the input signal as it travels from the gate pad down the gate stripe (which acts as an RC transmission line), this thickness has been varied across a slice by slowly moving a shield out of the way during the metal evaporation. The devices are thus identical except for the gate metal thickness, and the relative microwave performance can be measured as a function of gate thickness. The gain as a function of gate metallization thickness is plotted in Figure 19 for constant input power level and bias. Thicknesses of 1500 to 2000 Å for individual finger widths of 150 μm and 2.5 μm gate lengths are sufficient to maximize gain. The resistance of an individual gate stripe from one end to the other has been measured to be approximately what one would calculate from the observed dimensions and the bulk resistivity of Aℓ.

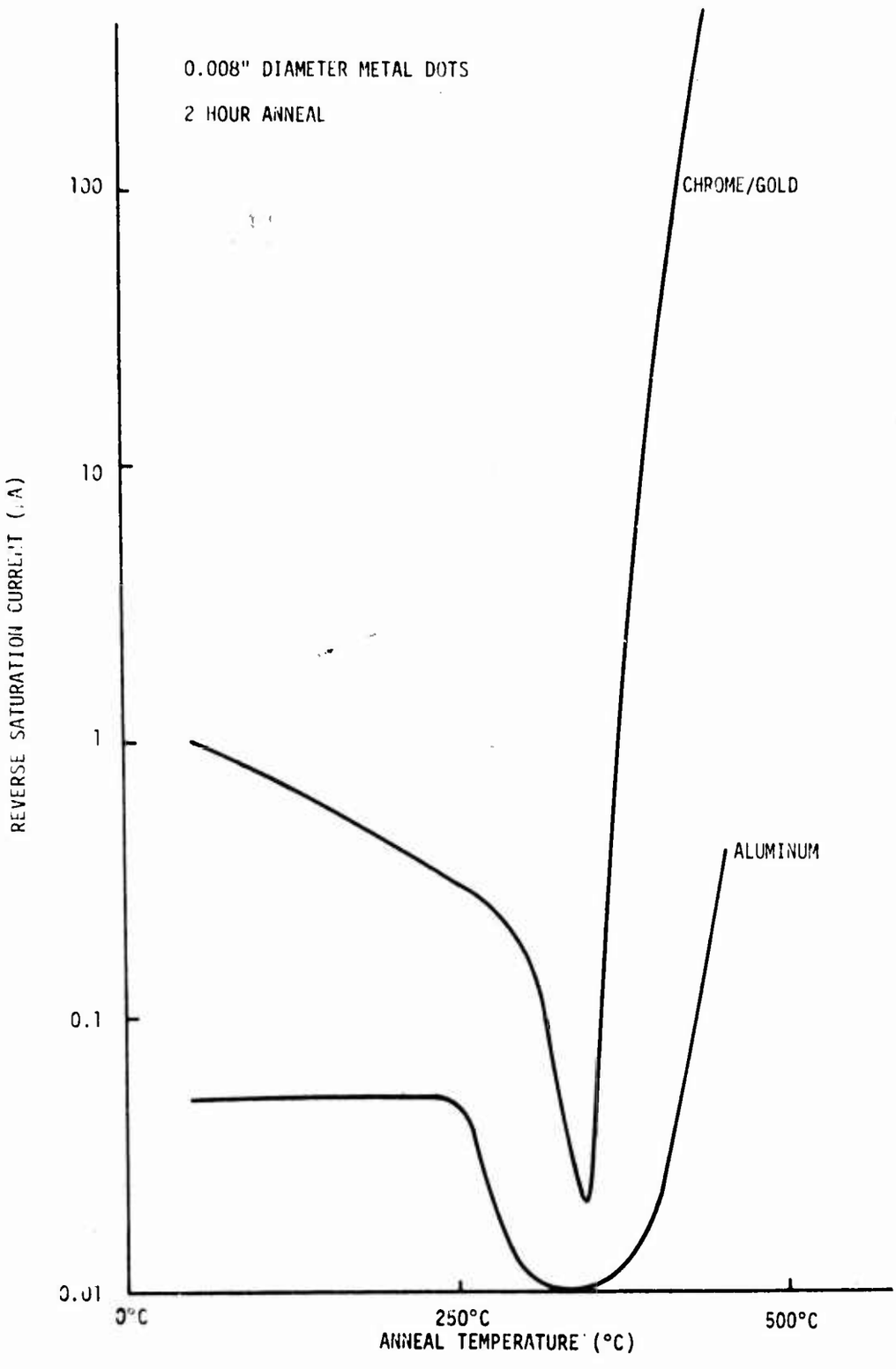


Figure 18 Reverse Saturation Current as a Function of Anneal Temperature of Aℓ and Cr/Au Schottky Barriers

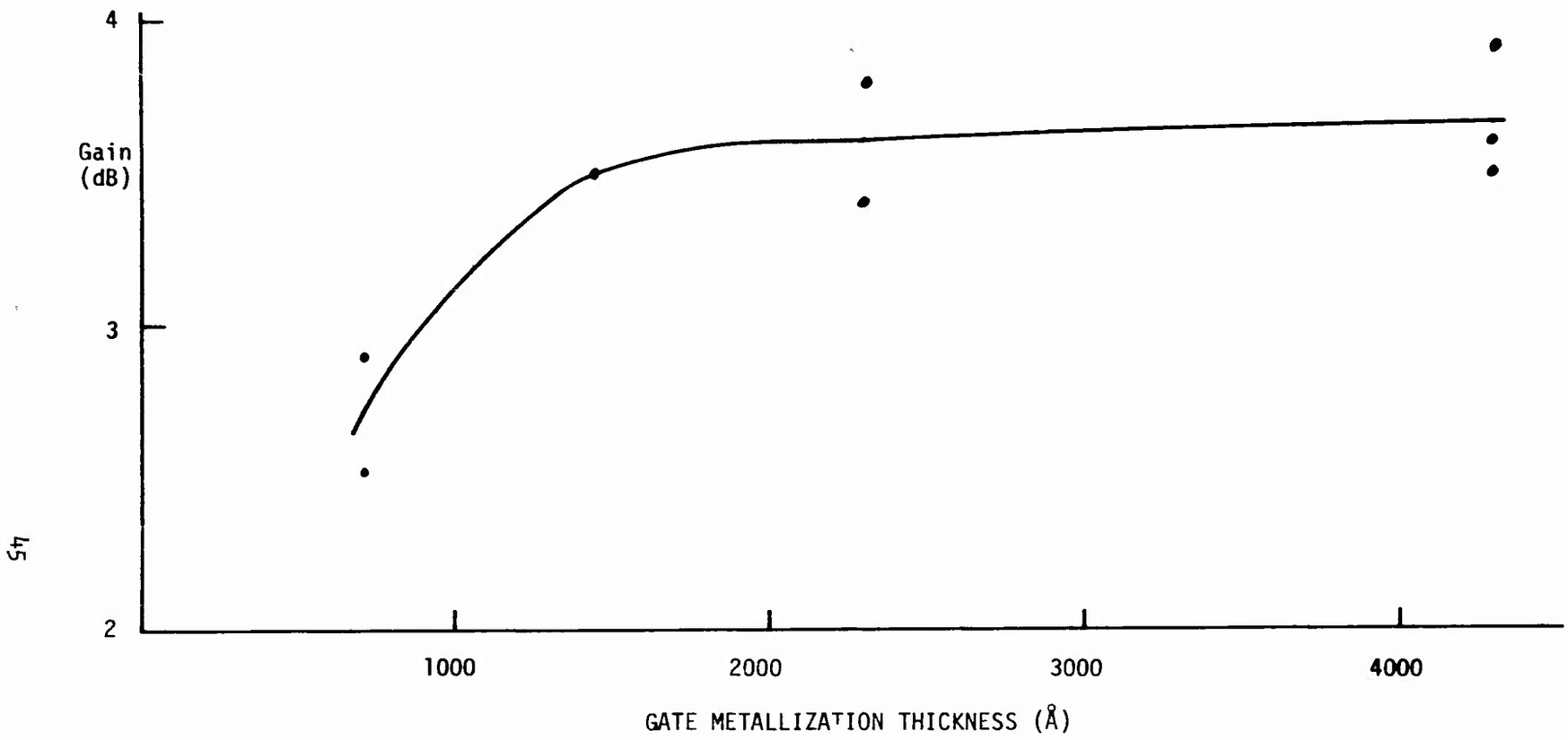


Figure 19 Device Gain at 9 GHz as Function of Aluminum Gate Metallization Thickness. (Input power is 15 dBm, V_{ds} = 5 V, V_{gs} = -1 V, total gate width is 1200 µm, individual gate stripe width is 150 µm, device mounted upright on ceramic.)

C. Fabrication Process

The fabrication process now being used for GaAs power FETs at Texas Instruments is described below; the process is relatively simple, with only four major steps.[10] The first three steps for a two gate stripe device are shown in Figure 20.

- Mesa Etch

Following epitaxial thinning, the first major processing step is to etch mesas through the thin n-layer to the semi-insulating substrate with room temperature 8 $H_2SO_4/H_2O_2/H_2O$. This isolates the source and drain terminals except for the channel under the gate and provides an insulated surface for the gate bonding pad. A mesa height of 0.5 to 1.0 μm is adequate to isolate adjacent mesas (resistances of 1 to 10 M Ω).

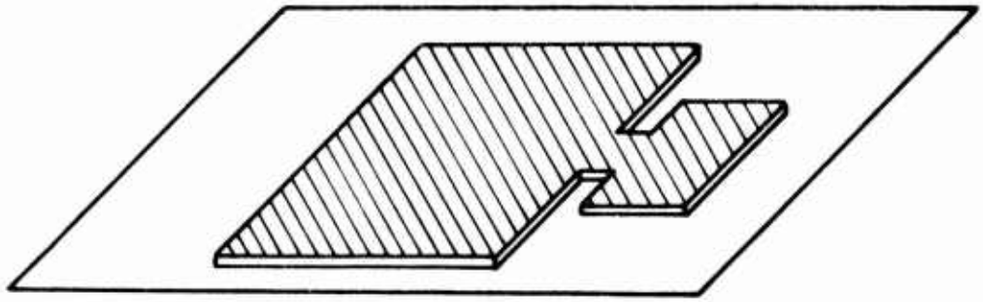
- Source/Drain Ohmic Contacts

The second step is the source/drain metallization. A lift-off pattern is defined in AZ-1350 photoresist, and the source/drain metal is evaporated over the slice. The unwanted metal is lifted off by dissolving the photoresist in acetone. This method of metal definition is very simple, gives sharp edge definition, and is capable of extremely fine geometries. The metal remaining on the source and drain is then alloyed into the GaAs, forming an ohmic contact.

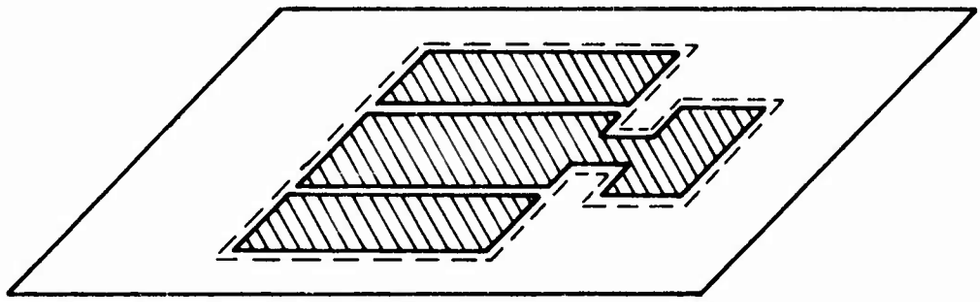
The ohmic contacts are formed by evaporating approximately 2000 Å of eutectic composition AuGe followed by a 200 to 400 Å Ni overcoat. Alloying is accomplished by raising the slice to 450°C for several seconds in flowing argon.

- Gate Metallization

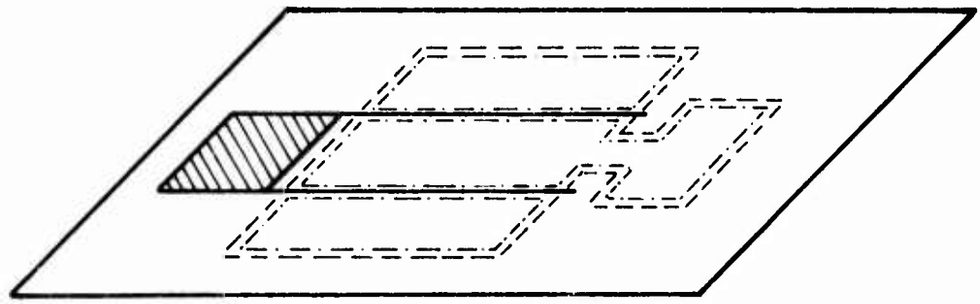
The third major processing step is the gate metallization. The gate pattern is defined in photoresist, a groove is etched in the GaAs surface for



MESA ETCH



SOURCE AND DRAIN METALLIZATION



GATE METALLIZATION

Figure 20 Planar Device Fabrication Process

two seconds with 10 $H_2SO_4/H_2O_2/H_2O$ at 5 to 25°C, and the metal is evaporated and lifted off as with the source and drain. The alignment of the gate in the source-to-drain gap is the most critical step. A 2 μm gate length and a 6 μm source-drain gap are entirely adequate for X-band operation. Gate stripe widths of 150 μm are found to be more than sufficient to eliminate attenuation effects with the gate metallization thicknesses employed (~ 4000 Å). The gate recess depths are in the range of 500 to 2500 Å, which can lead to as much as 50% reduction in the parasitic resistance.

Aluminum is used as the gate metal because of its reliability (see Section IV.B.4). Evaporation is carried out at about 50°C with a glow-discharge prior to deposition to ensure good adhesion. The slice is then annealed at 275°C for 15 minutes to minimize the gate leakage current.[11]

- Bonding Pad Metallization

Following the gate metallization, a layer of Cr/Au is evaporated on the source and drain to improve current spreading and bondability. A nitride layer is then deposited in the active region, and a thick (10 to 15 μm) Au layer is plated to the source pads to simplify bonding. Both the nitride and plated-up source pads protect the active regions from scratches. The slice is then lapped to 0.003 inch to 0.004 inch, metallized on the back, and scribed into individual devices.

SECTION V

EVALUATION

In this section the GaAs power FETs fabricated as described in the previous section are evaluated. Low frequency studies and X-band performance are discussed.

A. Low Frequency Evaluation

Several useful measurements can be performed on the GaAs FETs before actual microwave testing. A test pattern, which is placed periodically across the slice, permits study of the properties of the epitaxial material, ohmic contacts, and Schottky barrier right at the device. In this section the evaluation features on the test bar are described first, followed by a description of the results obtained by using the test bar as well as by measurements on the device structures.

1. Photomask Evaluation Features (Test Bar)

Photographs of the test bar which replaces one device in four are shown in Figure 21. The right-hand photograph is an overview, and details are shown in the left-hand photograph. The contact resistance and epitaxial sheet resistance are measured on the variably spaced ohmic contacts as described in Section IV.B.1, with typical results shown in Table I. The narrow Aℓ stripe can be used to measure the resistance of the gate stripe, which is found to be approximately what one would calculate from the bulk resistivity and known dimensions. Also, the square Schottky barriers can be used to determine the donor concentration as a function of depth from the C-V characteristics.

2. Visual Screen and Reliability

A close visual examination of the GaAs FET chips is an important step. Most four-cell devices (80 to 90%) which appear to have no shorted or broken

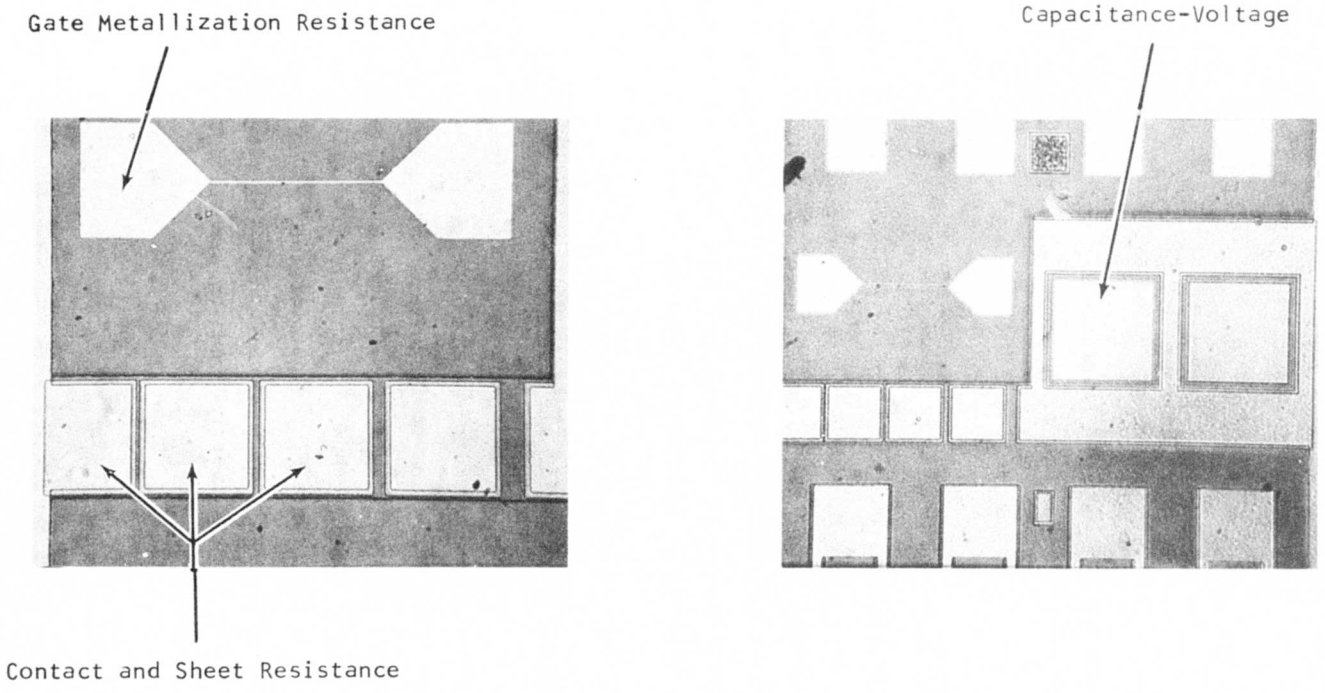


Figure 21 GaAs FET Test Bar

gates do not short out when voltage is applied. The number of good four-cell devices on a slice is usually in the range from 5 to 25%. The remainder of the devices are not useless, however, as they may be used for lower power (fewer cells) amplifier stages. Virtually all the devices that do fail when voltage is applied (for no readily apparent reason) do so within the first few minutes (most within a few seconds), and those that last beyond this time appear to be reliable when operated at a drain voltage of 8 V.

3. Capacitance-Voltage (C-V) Measurement

An automatic profiler is used to determine the carrier concentration as a function of depth into the epitaxial layer from the C-V characteristic of the square Schottky barrier on the test bar (see Figure 21). Because of the semi-insulating substrate, both probes are to the upper surface. The increasing series resistance as pinch-off is approached causes the plots to be somewhat distorted in that region. Several such plots are shown in Figure 22; all the curves are from slices that yielded 2400 μm gate width devices capable of at least 1 W output power at 9 GHz with 4 dB gain. The dashed curves are from slices near the high and low carrier concentration limits for 1 W output power. Clearly, there is a large range of carrier concentration profiles that will produce good devices. It is apparently very important whether or not the profile is flat or the carrier concentration increases somewhat as the substrate is approached. When the concentration is less than about 5×10^{16} or above about 1.5×10^{17} cm^{-3}, device performance drops; 8 to 10×10^{16} cm^{-3} appears to be about optimum.

4. Current-Voltage (I-V) Measurement

Further information is gained from the device I-V characteristic. Figure 16 showed typical characteristics for a 1200 μm gate width device. A

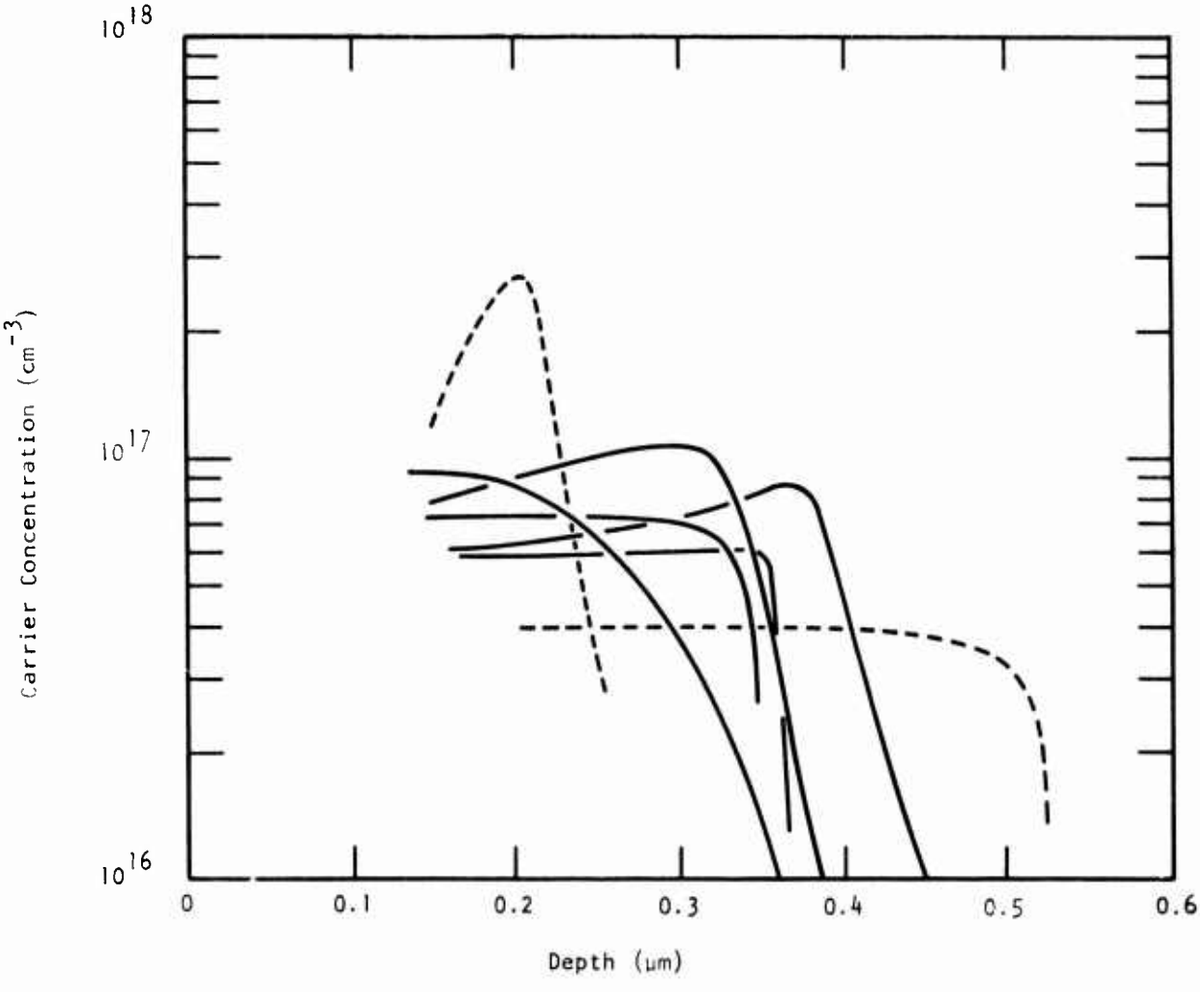


Figure 22 Carrier Concentration vs Depth for a Number of GaAs FET Slices

low value of the saturation voltage indicates a low resistance ohmic contact and adequate gate recess. For the devices studied here, a saturation voltage of 2.2 V or less is considered good. The values of saturation current and pinch-off voltage indicate the epitaxial layer thickness if the carrier concentration determined from the C-V data is taken into account. It has been found that the pinch-off voltage should be at least 3 V. The conductivity of the epitaxial layer is indicated by the transconductance. A high transconductance for a device made from a slice known to have only moderate donor doping implies a high mobility. A good transconductance for $n \cong 1 \times 10^{17}/cm^3$ is g_m = 65 to 85 mmho/mm gate width.

B. Microwave Evaluation

The microwave performance at X-band of the GaAs power FETs fabricated as described earlier are summarized in this subsection. The circuit in which the tests are made and the various device mounting configurations are described. The device performance as an amplifier is discussed, along with the factors influencing performance such as gate length, gate width, frequency, epitaxial thickness, etc. Finally, some noise figure measurements are described.

1. Test Circuit Description

All the rf gain and output power measurements are made in the waveguide test set-up with the schematic shown in Figure 23. The gain is determined by first calibrating the set-up after replacing the FET with a length of coaxial line; the gain at that input power level is then found from the increased output power with the FET in place. The FET is mounted to a small Cu block as described in the next subsection. Short lengths of microstrip butting up to the device and to which the gate and drain are bonded allow partial matching of the device impedance to 50 Ω by chip tuning. The slide screw tuners permit slightly better matching of the impedance (gain improvement of around 1 dB) and are used to match all changes in device impedance caused by changes in bias voltages and input power level.

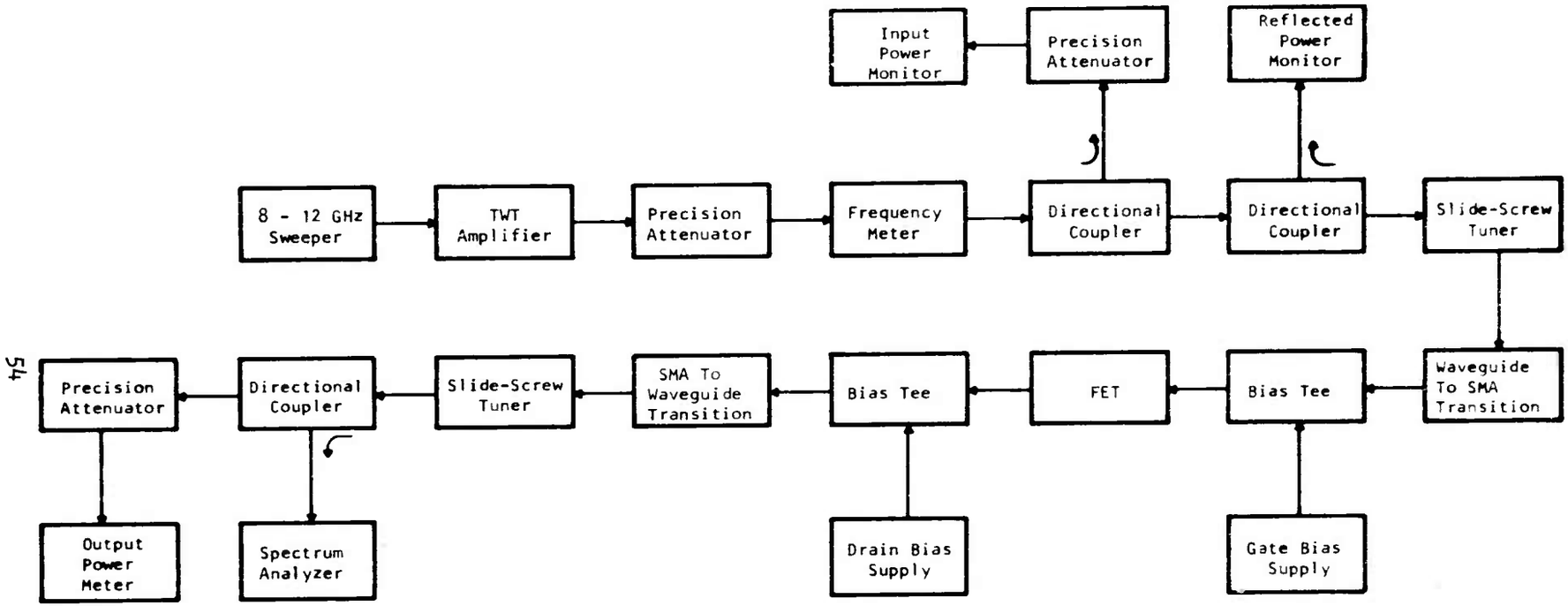


Figure 23 Block Diagram of Gain and Output Power Measurement Equipment

2. Device Mounting Configuration

As mentioned in Section IV.A.1, the improvement responsible for the largest increase in GaAs FET output power is mounting directly on a Cu block instead of an alumina carrier. Output powers for two-cell (1200 μm gate width) devices from the same processing run are shown in Table 2. The devices mounted on Cu blocks are clearly superior to the one on alumina; the superiority is even greater when one considers that three- and four-cell devices are little better than two-cell devices when mounted on alumina carriers, but give up to 1 W when mounted on Cu blocks. The devices flipped and pressed into In-coated Cu blocks (shown in Figure 24) and the upright mounted devices soldered to Au-plated Cu blocks (shown in Figure 25) have similar microwave performance. Devices are now routinely mounted upright, since that configuration is much easier to accomplish. Devices are soldered to small Au-plated Cu blocks with AuSn preforms, and these small blocks are tightly screwed to larger Cu blocks containing short microstrip lines leading to the gate and drain bonding pads to which 0.001 inch Au wires are bonded. A photograph of a GaAs FET soldered to a small block and screwed to a larger block is shown in Figure 26.

These larger blocks are screwed to a water-cooled heat sink during device testing. As mentioned earlier, the device impedance is partially tuned with metal-coated ceramic chips on these microstrip lines.

It was originally thought that flip-chip mounting on a Cu block would improve GaAs FET performance primarily by reducing source lead inductance. The equally good performance of the upright stitch-bonded configuration indicates that this may not be the case, since the upright device probably has greater source impedance than the flipped device. It is now thought that the improvement is primarily thermal. It is possible that the improved electrical ground contact causes the increase in output power, but the fact that the relative

Table 2

DEPENDENCE OF OUTPUT POWER ON FREQUENCY AND NUMBER OF CELLS CONNECTED FOR A GaAs POWER FET (GATE LENGTH - 1.8 μm)

Frequency (GHz)	Number of Cells	P_{out} (mW) with 4 dB Gain	P_{out} (mW) with 6 dB Gain
8	1	340	315
	2	710	600
	3	1100	890
	4	1380	955
9	1	340	280
	2	660	500
	3	850	615
	4	1150	790
10	1	315	250
	2	560	440
	3	725	525
	4	980	660
11	1	250	190
	2	410	310
	3	560	415
	4	775	540
12	1	225	160
	2	330	260
	3	415	350
	4	575	400

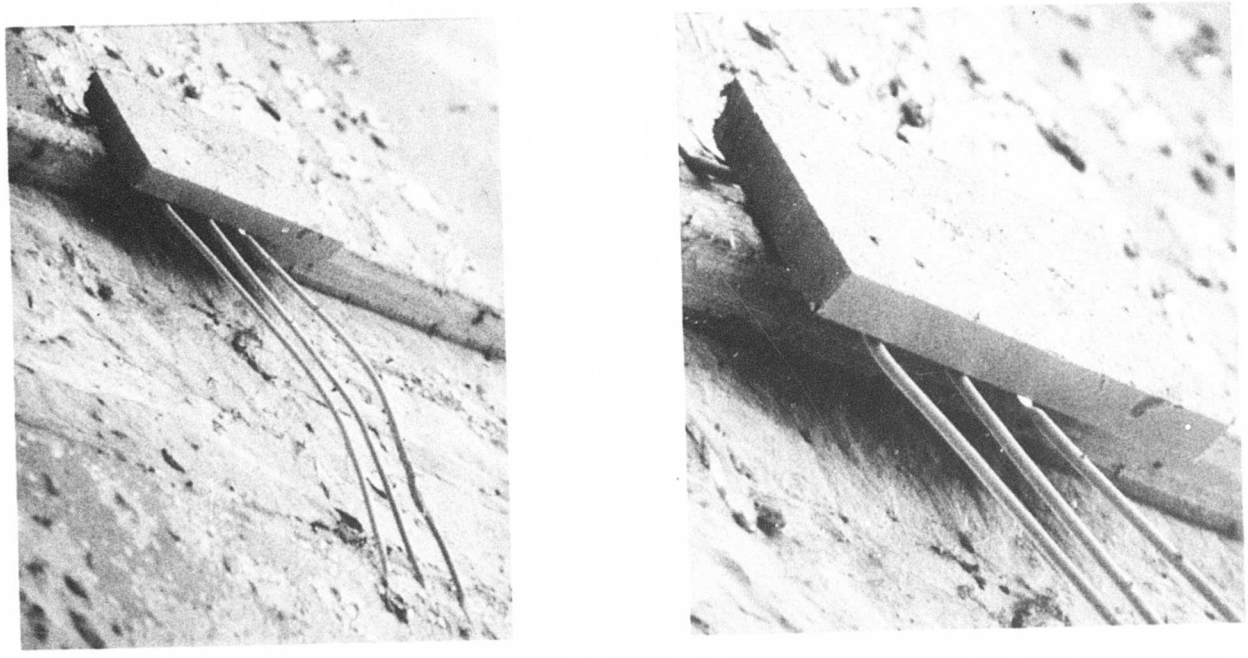


Figure 24 SEM of Four-Cell GaAs FET Mounted in the Flipped Configuration on a Cu Block. Three cells are bonded.

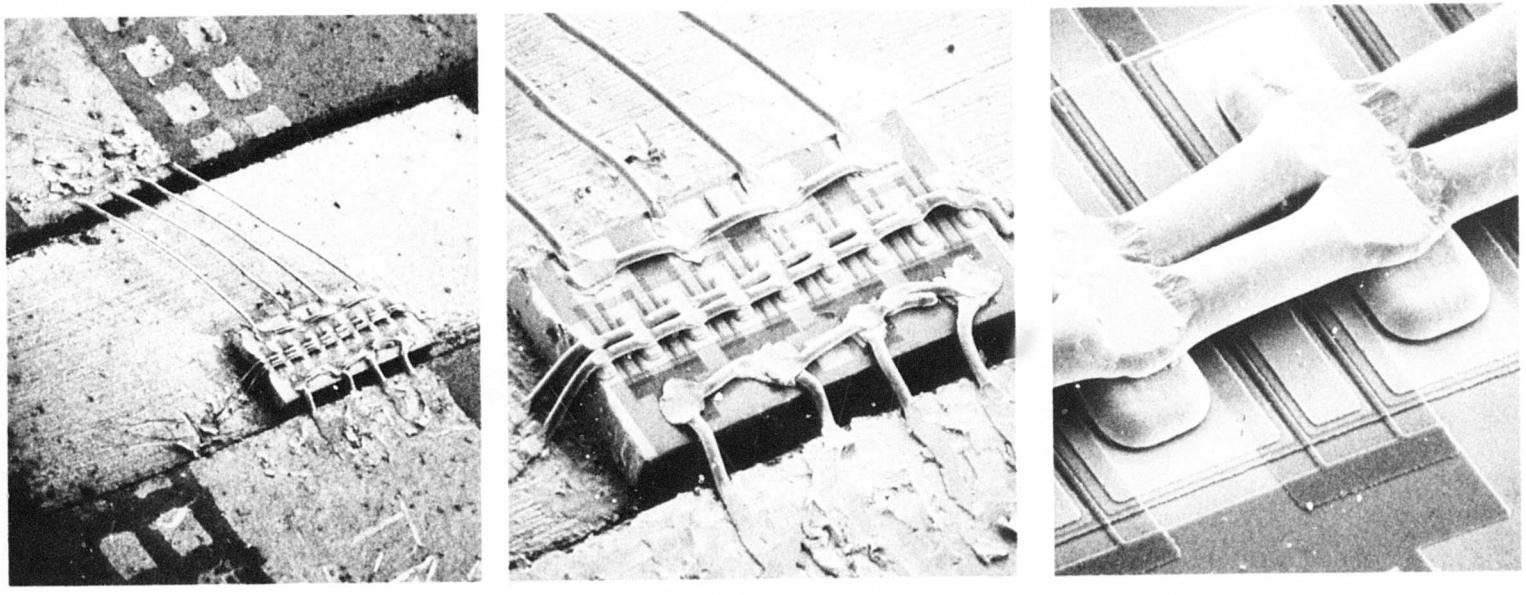


Figure 25 SEM of Four-Cell GaAs FET Mounted in the Upright Configuration on a Cu Block

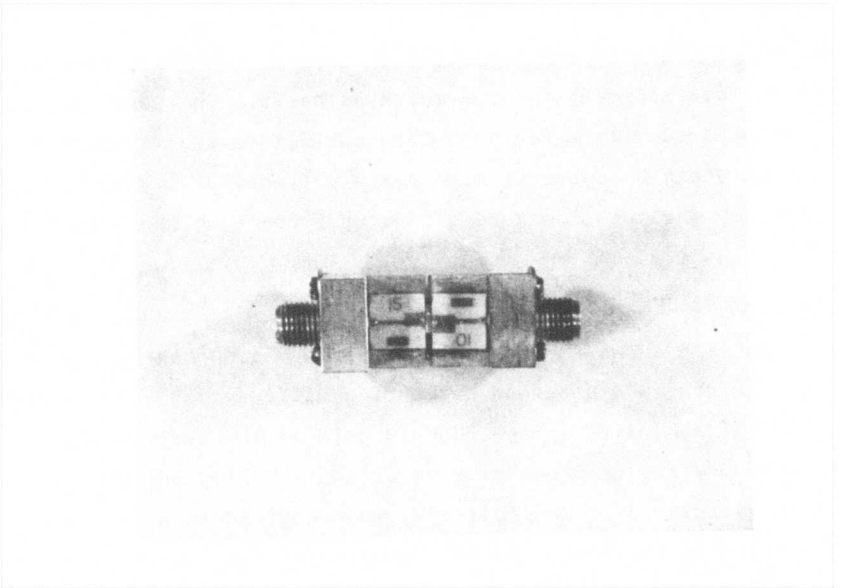


Figure 26 Photograph of GaAs FET Mounted to Cu Block for Microwave Testing

improvement with three- and four-cell devices is much more than with one- and two-cell devices supports the thermal hypothesis. The GaAs FETs mounted to Cu blocks are also much more reliable than earlier devices mounted to alumina carriers (they can be operated with drain voltages of 8 V or more), probably as a result of the much lower temperatures present in the active region.

3. Microwave Performance

Table 3 shows the best device performance observed to date. Different gate widths are obtained by bonding different numbers of cells (bonding two devices side-by-side in the 4800 μm gate width case), while the different gate lengths are due to processing variations. Different pinch-off voltages are due to variations in the epitaxial layer thickness and gate recess depth from one slice to the next. As the results for the device giving the two sets of data at 9 GHz show, the linear gain at low input power levels may be increased at the expense of reduced maximum output power. The difference between the two cases is just the impedance matching, since the device impedance changes with input drive level. This is further illustrated in Figure 27 where the output power of a four-cell GaAs FET at 9 GHz is plotted as a function of input power for three different tuning conditions. The bias conditions remain unchanged, and the device is tuned for maximum output power with 15 dBm, 20 dBm, and 26 dBm input power by changing the input and output circuit impedances. The circuit impedance is not changed when moving along any one of the curves.

Devices with 2400 μm gate widths from nine device runs (seven different slices) have produced 1 W or more at 9 GHz with 4 dB gain, and it appears that devices from most slices having the correct epitaxial carrier concentration and thickness (see Figure 22 for an estimate of the range of acceptable values) are capable of this performance.

Table 3

GaAs POWER FET PERFORMANCE

Frequency (GHz)	Linear Gain (dB)	Output Power (mW)	Gain at P_{out} (dB)	Power-added Efficiency at P_{out} (%)	Total Gate Width (μm)	Gate Length (μm)	Operating Conditions		
							Class	Drain Voltage (V)	Pinch-off Voltage (V)
8	6.7	910	5.6	20	1200	1.5	A	8	15
8	5.4	710	4.5	46	1800	2.0	B	8	3.5
8	4.9	1620	4.1	32	2400	2.4	AB	9	8
8	4.8	2500	4.0	25	4800	2.4	AB	9	8
9*	5.2	1000	4.0	30	1800	2.4	AB	8	8
9**	6.5	630	5.0	22	1800	2.4	AB	8	8
10	5.7	780	4.0	16	1200	1.5	A	8	15
10	5.5	500	4.0	34	1800	2.0	B	8	3.5
12	5.0	510	4.1	11	1200	1.5	A	8	15

* Tuned for maximum P_{out} at 4 dB gain

** Same device as * but tuned for high linear gain

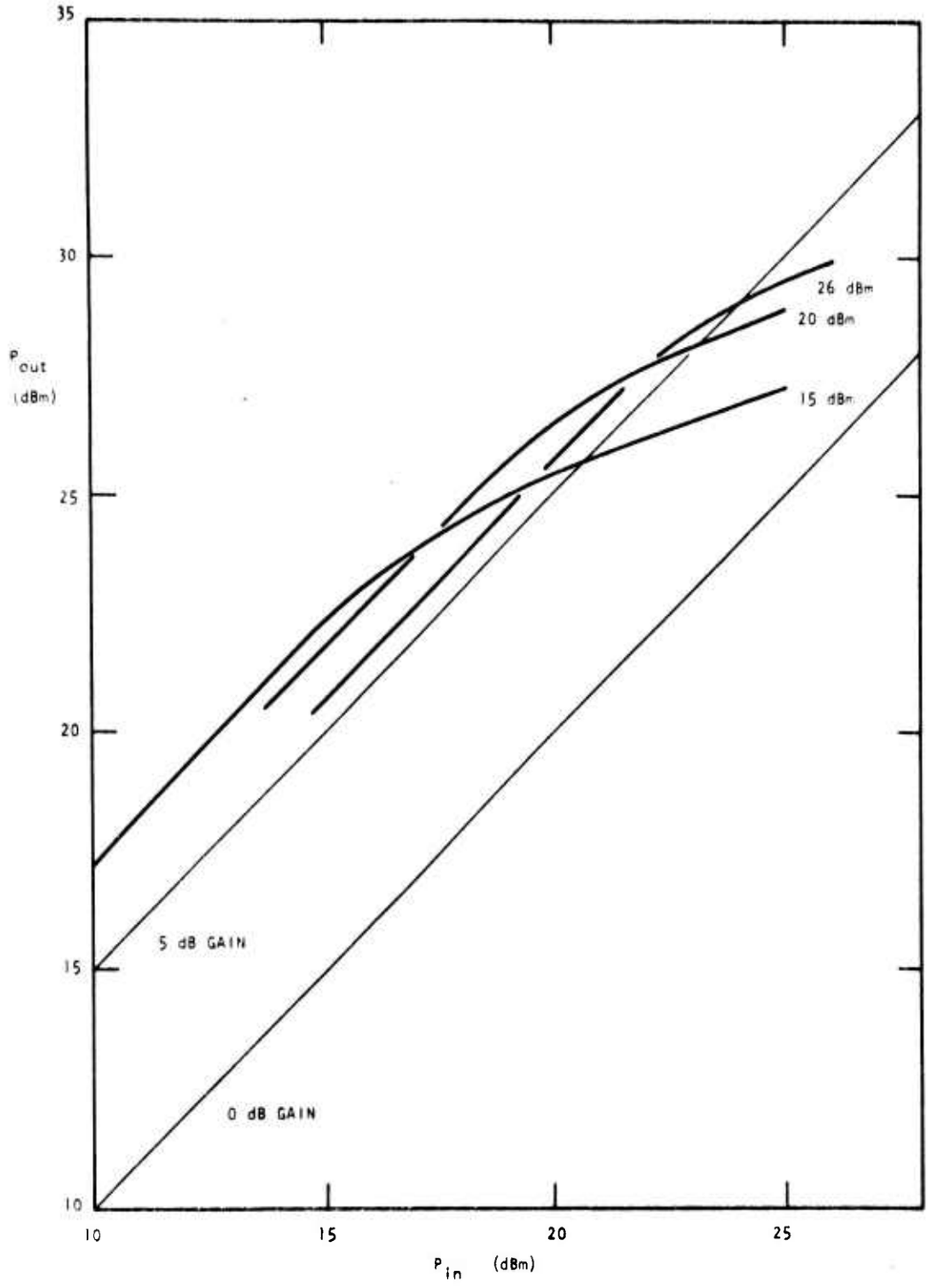


Figure 27 Dependence of 9 GHz Performance On Tuning for 2400 μm Gate Width GaAs FET V_{ds} = 8 V, V_g = -3 V. Tuned for maximum P_{out} at the input powers shown.

High power operation requires that if the number of cells in the GaAs FET increases, the output power increases, preferably by the same fraction. Figure 28 shows the output power at 9 GHz as a function of input power for one 2 μm gate length device with from one to four cells bonded and constant bias conditions. The output power for a specific gain is approximately doubled with two cells over that for one cell, and three and four cells increase the output power by almost a proportionate amount.

At higher frequencies the addition of extra cells is not as effective. Table 4 gives the output power at 4 dB gain and 6 dB gain as a function of frequency for different numbers of cells connected on a typical device having a 2.4 μm gate length. For this device the addition of extra cells (up to four) causes a significant increase in output power at 8 GHz with the fractional improvement decreasing at higher frequencies. Four cells have three and a half times the output power of one cell at 8 GHz, but only two times as much at 12 GHz.

There is also a difference in microwave performance with gate length. Shorter gate length devices have approximately the same maximum output power as relatively longer ones at 8 GHz, but the decrease with frequency is much less severe (e.g., the two-cell, 1.5 μm gate length device of Table 3 has higher output power at 12 GHz than the four-cell, 2.4 μm device of Table 4). The shorter gate length devices have a higher linear gain at all frequencies, and it is possible to use more cells with shorter gate lengths.

Another device variable is epitaxial layer thickness (pinch-off voltage). Table 5 compares two devices from the same processing run that have different pinch-off voltages (due to epitaxial layer thickness variations and/or different gate recess depths). The device with the larger pinch-off voltage is capable of somewhat higher output power, but its maximum power-added efficiency is less. Devices with low pinch-off voltages can be run at or close to class B, whereas those with large pinch-off voltages must be run at or near class A.

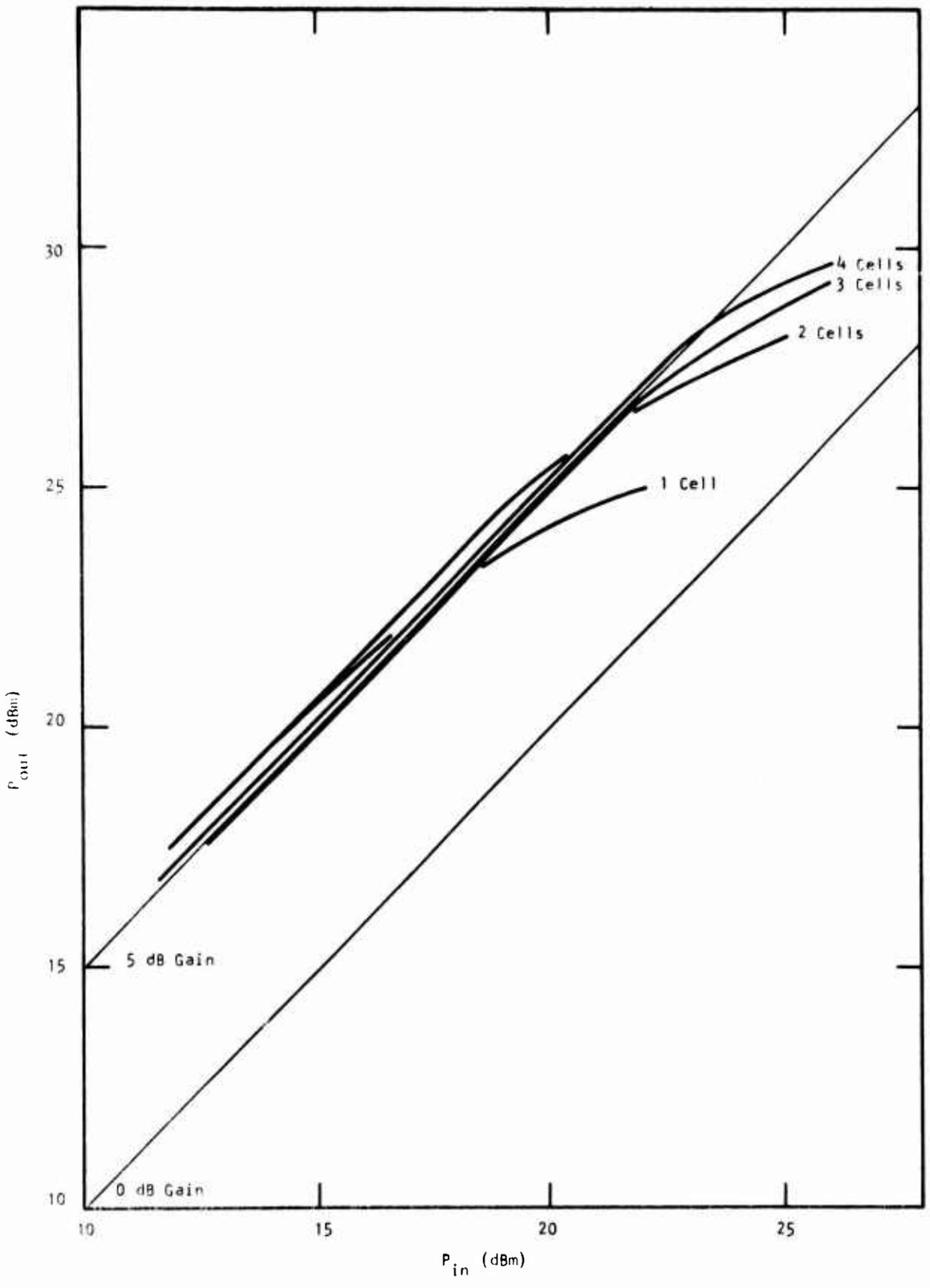


Figure 28 9 GHz Performance of One to Four Cells of the Same GaAs FET Tuned for Maximum Output Power at 4 dB Gain. V_{ds} = 8 V, V_g = -2.5 V

Table 4

DEPENDENCE OF OUTPUT POWER ON FREQUENCY AND NUMBER OF CELLS CONNECTED FOR A 2.4 μm GATE LENGTH GaAs FET

Frequency (GHz)	Number of Cells	P_{out} (mW) at 4 dB Gain	P_{out} (mW) at 6 dB Gain
8	1	420	360
	2	810	500
	3	1150	600
	4	1450	630
9	1	360	210
	2	660	345
	3	870	480
	4	1070	500
10	1	315	135
	2	480	220
	3	645	325
	4	775	390
11	1	260	125
	2	330	175
	3	490	260
	4	615	355
12	1	200	100
	2	260	150
	3	330	200
	4	380	210

Table 5

EFFECT OF GaAs POWER FET MOUNTING SCHEMES ON 9 GHz PERFORMANCE. V_{ds} = 8 V, GATE LENGTH = 2.0 μm.

Device	Maximum P_{out} at 4 dB Gain (mW)	Maximum P_{out} at 6 dB Gain (mW)	Maximum Power-Added Efficiency at 4 dB Gain (%)
Two-cell Upright on Alumina Carrier	390	--	27
Two-cell Flipped on In-Coated Cu Block	590	465	38
Two-cell Upright on Au-plated Cu Block	615	470	35

4. Noise Measurement

Noise figures have been measured on GaAs FETs from several device runs in the set-up schematized in Figure 29. The impedances are matched with metallized alumina chips to give a minimum noise figure. The results of measurements on several devices, shown in Table 6, indicate that the noise figure is not significantly affected by the number of cells or the bonding scheme (flipped or upright on Cu blocks). The best data are plotted in Figure 30, which includes theoretical data for 1 μm and 2 μm gate length devices and a curve averaging the experimental data on 1 μm devices from a number of laboratories.[12] Apparently, the theory predicts lower noise figures with 1 μm devices than are observed in other laboratories; yet the 2 μm results at Texas Instruments are lower than the theory predicts. This may be due to the superior ohmic contact and mounting schemes developed for high power operation.

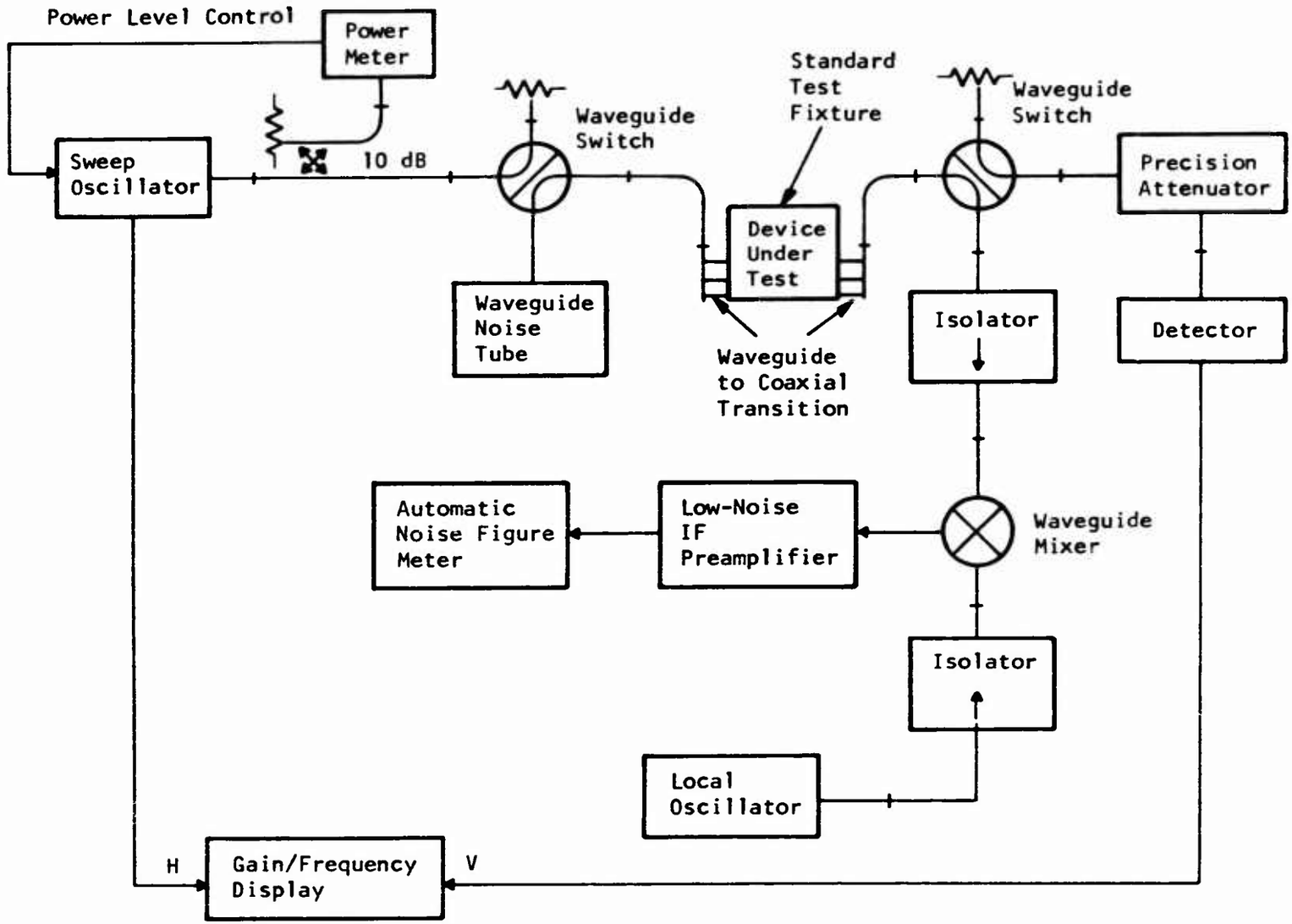


Figure 29 A Schematic Block Diagram of Noise Figure Measurement Equipment

Table 6

MINIMUM NOISE FIGURES OF GaAs POWER FETs MOUNTED ON Cu BLOCKS

Slice Number	Run Number	Device Number	Number of Cells	f (GHz)	NF_{min} (dB)	G_{av} (dB)
16711-84A	2	13	1 Upright	8.5	4.8	7.0
16711-84A	2	8	1 Upright	8.0	3.7	6.5
				8.5	4.1	6.5
				9.5	4.6	5.5
				10.0	5.4	5.0
16711-84A	2	9	1 Flipped	8.5	4.8	6.0
				10.0	5.2	5.0
16711-84A	2	11	3 Upright	8.5	4.2	4.0
16711-84A	2	12	2 Upright	8.5	4.1	5.0
16711-84A	3	4	1 Upright	8.5	5.0	5.0
16582-66	2	2	1 Flipped	8.5	4.0	5.5
				10.0	5.0	5.0

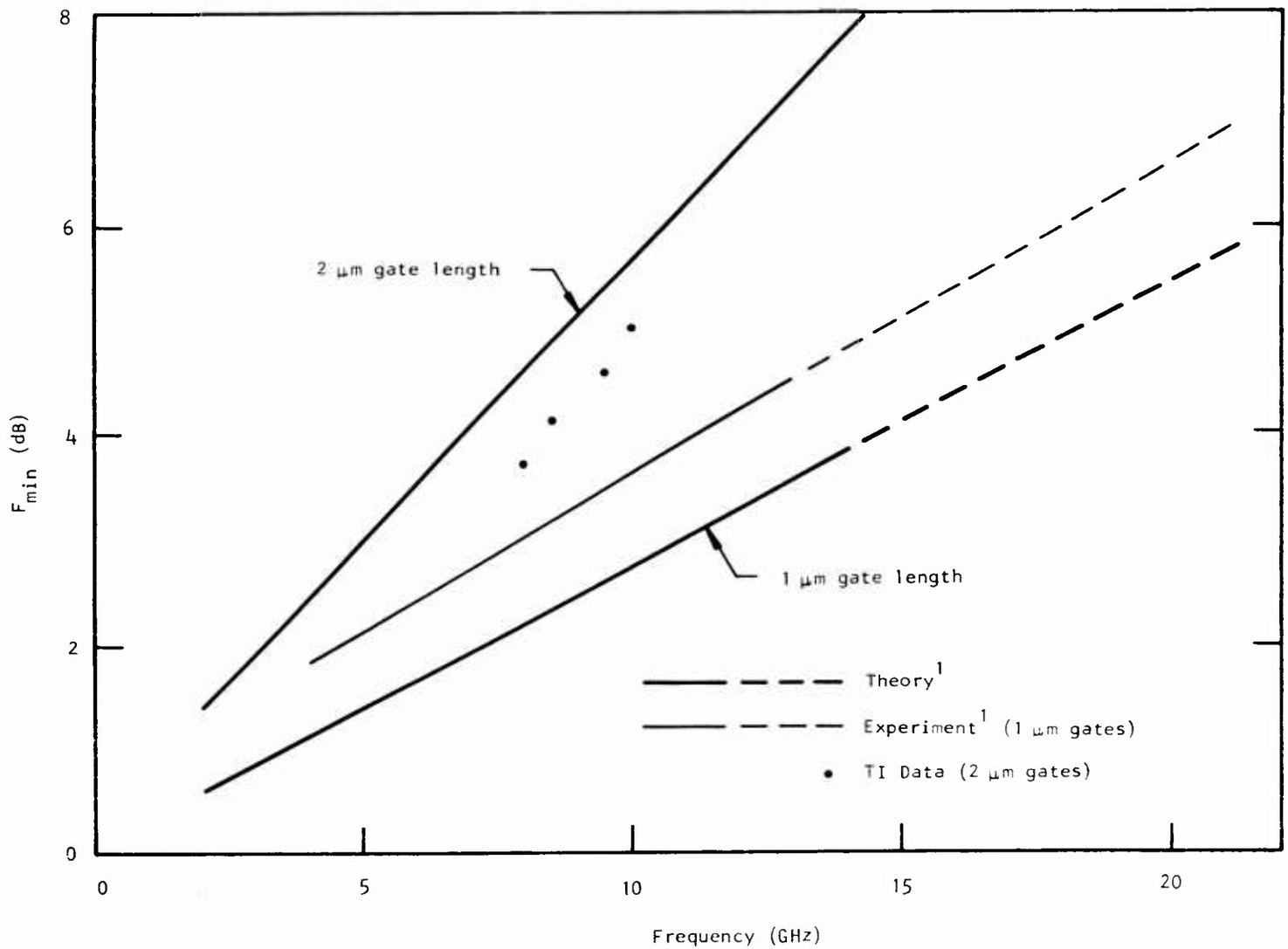


Figure 30 Frequency Dependence of Theoretical and Experimental Minimum Noise Figures for 1 μm and 2 μm Gate Length GaAs FETs

SECTION VI

MICROSTRIP AMPLIFIER DEVELOPMENT

The GaAs power FETs described in previous sections have been used to develop an X-band amplifier that can be used to drive power amplifiers in the transmitter chain of active-element, phased-array radar, ECM, and communication systems. The performance specifications are given in Table 7.

Table 7

X-BAND GaAs FET AMPLIFIER SPECIFICATIONS

Parameter	Specification
Center frequency	9.5 GHz
Bandpass (3 dB)	9.2 - 9.8 GHz
Gain	20 dB
Power Output	300 mW
Duty Cycle	cw
Input and Output Connectors	SMA 50 ohms

In addition to the X-band FET amplifier discussed above, a hybrid FET/IMPATT amplifier has been designed and tested. This amplifier consists of three FET stages and a final GaAs avalanche diode stage. Output power of 1 W at 26 dB gain can be obtained over the same frequency band with a 3 dB bandwidth of 600 MHz.

The microwave integrated circuit (MIC) work performed during the contract period has been directed toward the demonstration of the amplifiers described above. The essential phases of the FET amplifier fabrication task are shown in Figure 31. Large- and small-signal S-parameter measurements were performed during the device characterization task. The S-parameter data were used in two ways to arrive at an optimum matching network design. Both the frequency-dependent S-parameters and the deduced equivalent circuit were used for computer-aided network design.

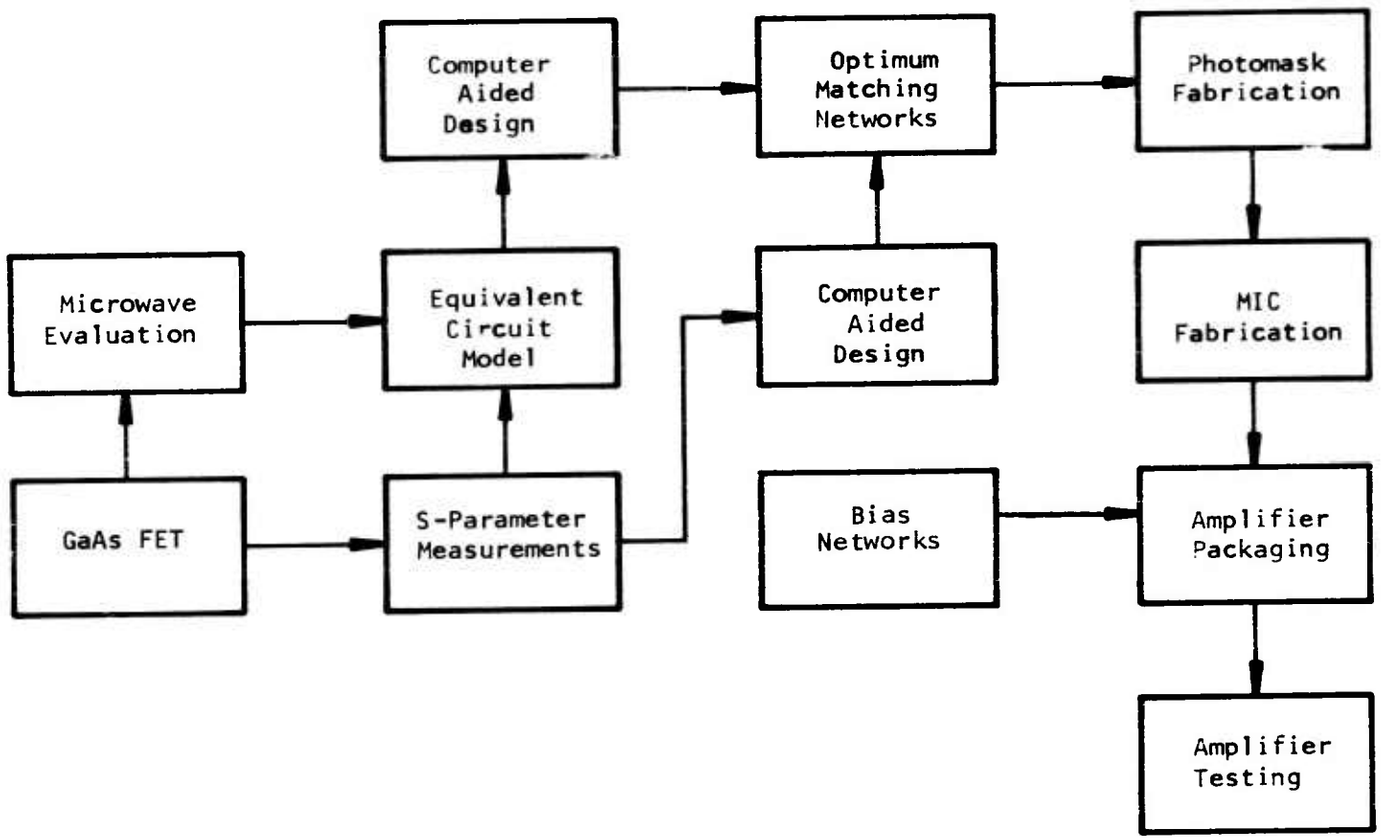


Figure 31 Flow Chart of the FET Amplifier Design Task

After the desired matching networks have been generated for the individual stage, the photomask and the microstrip circuit can be fabricated. The individual stages are then cascaded to achieve the desired gain and output power.

This section presents detailed discussions of the amplifier design approaches. Microwave performance results for the amplifiers developed under this contract are presented to conclude this section.

A. Device Characterization

A conventional test method providing input and output tuning flexibility can be used as the first step in the evaluation of the GaAs FET. It can provide the device characteristics of maximum available gain, output power, and power-added efficiency at the desired frequency for different sets of bias conditions. The experimental set-up for the device characterization was shown in Figure 23.

To completely characterize the microwave properties of the power FET device, it is necessary to measure the small-signal and large-signal S-parameters as a function of frequency, bias conditions, and rf input signal levels. While the small-signal S-parameters can be measured very rapidly with an automatic network analyzer, the large-signal measurement requires some minor modifications of the network analyzer to allow for higher rf incident power to drive the FET. A microstrip holder for the FET chip is available at Texas Instruments for this purpose. The FET chip is mounted upright on a gold-plated copper carrier. This same carrier is used for both device characterization and actual amplifier construction. In this way, the effects of parasitic reactances due to the mounting structure are the same in both cases.

The results of the small- and large-signal S-parameter measurements can be related to the microwave equivalent circuit elements shown in Figure 2. Although

this lumped-element equivalent circuit model has been derived from operating FETs in a small-signal, linear operating region, it has been experimentally verified as adequate for the large-signal case. As a first-order approximation, the elements of the equivalent circuit can be treated as a function of the input and output power levels. The maximum available gain at the desired output power level can be obtained only if the design of the input/output matching networks is based on an accurate knowledge of the device impedances at the corresponding signal levels.

Figures 32 and 33 show the input and output impedances of a power FET with a 1200 μm total gate width under small-signal conditions. The equivalent circuits are also shown in the insets. In these measurements the effects of the bond wire inductances were also included. These results indicate that the input circuit consists of a 3.5 ohm resistor in series with a 1.2 pF capacitor, while the output can be represented as a 10 ohm resistor in series with a 0.29 pF capacitor.

Large-signal S-parameter measurements have been carried out in a 50 ohm system for the power FETs with different dc bias and rf power levels. The network analyzer has been modified to allow for high incident rf power to be used in the measurement. Figure 34 shows plots of S_{11} and S_{22} as function of bias voltage and rf input levels for a 1200 μm gate-width FET (bondwire inductance included). It is found that of all the S-parameters, S_{22} and S_{21} are the most sensitive to the changes in rf drive levels. S_{11} is practically independent of the drive levels. Generally, the equivalent series resistance of the output increases with increasing rf signal levels, while the capacitive reactance decreases. Examination of the conventional lumped-element equivalent circuit of the FET, consisting of an RC parallel network in the output, shows that if this shunt resistance decreases with the signal level, the observed signal level dependence of S_{22} would result. One of the reasons S_{11} is insensitive to the signal level could be the near-unity reflection coefficient of the input in a 50 ohm system (the input

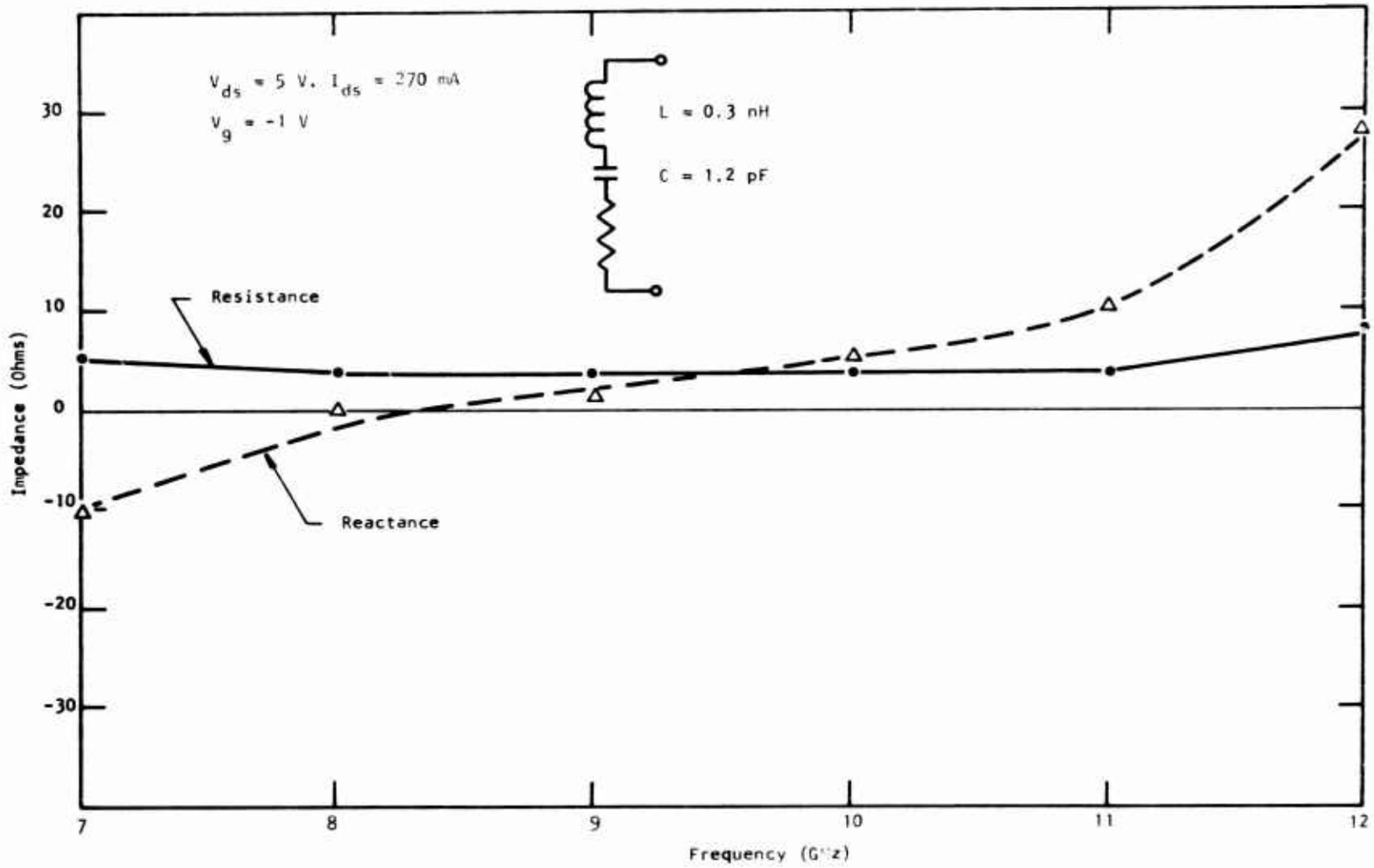


Figure 32 Input Impedance of a 1200 μm Gate Width FET as a Function of Frequency Under Optimum Bias Conditions

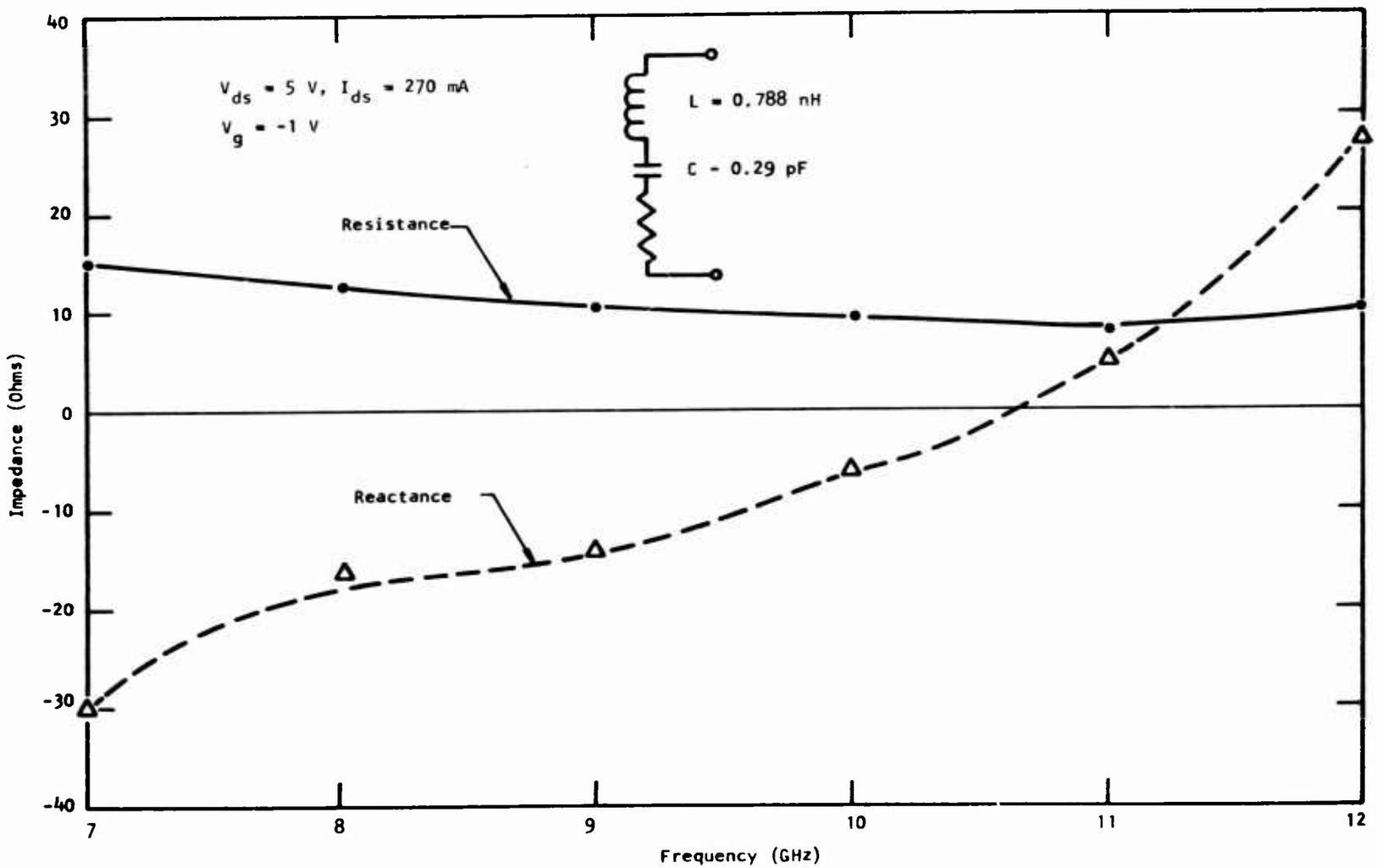


Figure 33 Output Impedance of a 1200 μm Gate Width FET as a Function of Frequency Under Optimum Bias Conditions

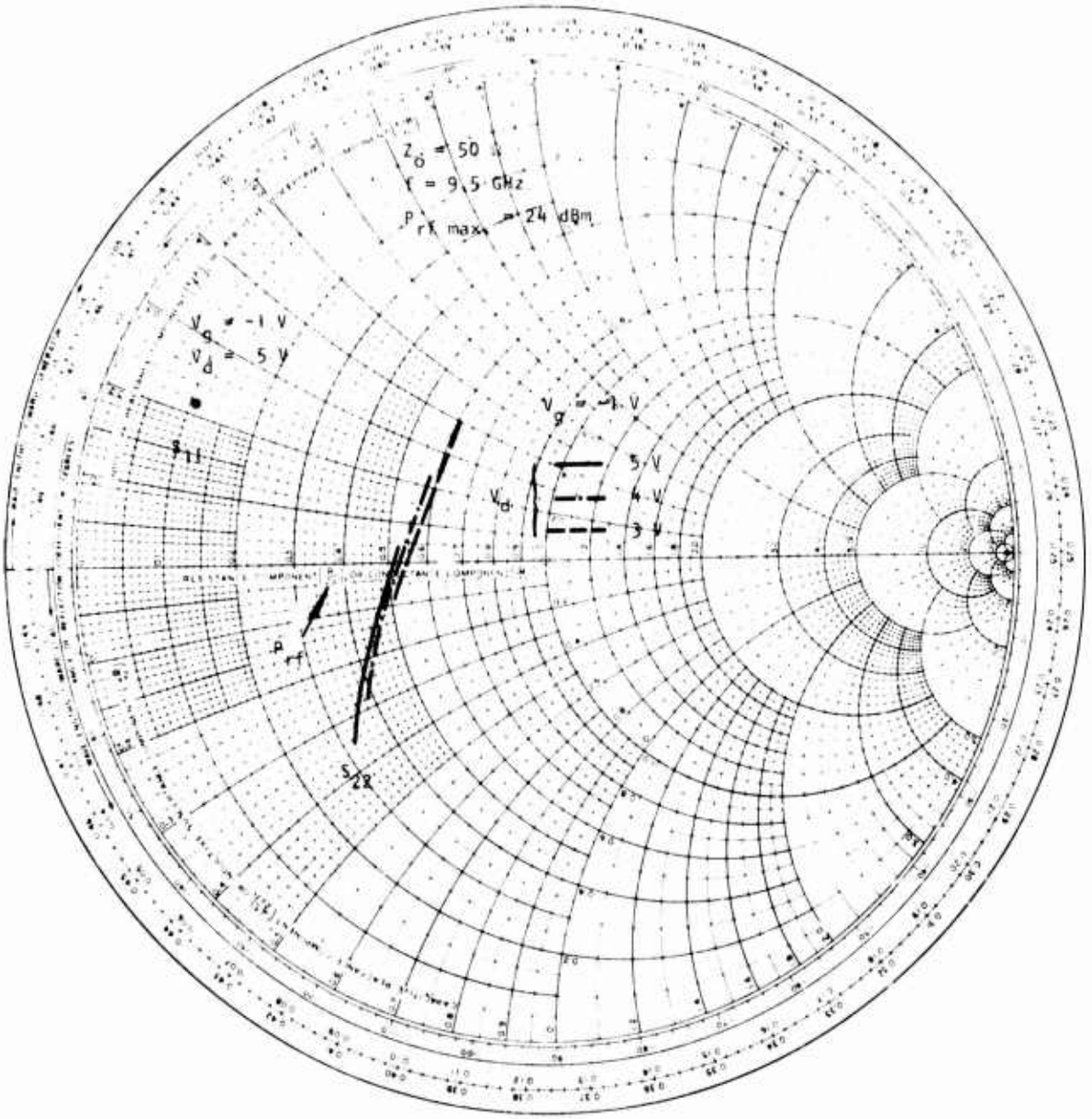


Figure 34 Effects of rf Signal Level on the S_{11} and S_{22} of a 1200 μm Gate Width FET

resistance of the power FET is quite low, on the order of 3 to 5 ohms). Significant rf voltage swing can be obtained either by increasing the incident rf power or by reducing the impedance of the measuring system. In this way, a more realistic correlation between the S-parameters and rf power level can be established.

B. FET Amplifier Design Theory

The transducer power gain is given by the following expression:

$$G = \frac{|S_{21}|^2 (1 - |\Gamma_s|^2)(1 - |\Gamma_L|^2)}{|(1-S_{11}\Gamma_s)(1-S_{22}\Gamma_L) - S_{21}S_{12}\Gamma_L\Gamma_s|^2} . \qquad (15)$$

Γ_s and Γ_L are the source and load reflection coefficients, respectively. Normally, since S_{12} for the GaAs FET is very small, the term containing S_{12} in the denominator of the right-hand side of the above equation can be neglected. In this case, the unilateral transducer gain reaches a maximum when $\Gamma_s = S_{11}^*$ and $\Gamma_L = S_{22}^*$. In other words, a simultaneous conjugate match needs to be provided for both the source and the load over the frequency band for maximum transducer gain.

Figure 35 shows a simplified block diagram of an FET amplifier with its associated input and output matching networks. The FET is completely characterized by the S-parameters. The S-parameters are, in general, functions of frequency, bias conditions, and rf signal levels. From Equation (15), it is seen that the essential task of the amplifier design is to find the desired source and load reflection coefficients, Γ_s and Γ_L, for a prescribed amplifier gain response. The input matching network performs the transformation of the generator impedance Z_o to an impedance corresponding to the desired Γ_s at the input of the FET. Similarly, the output matching network transforms the load

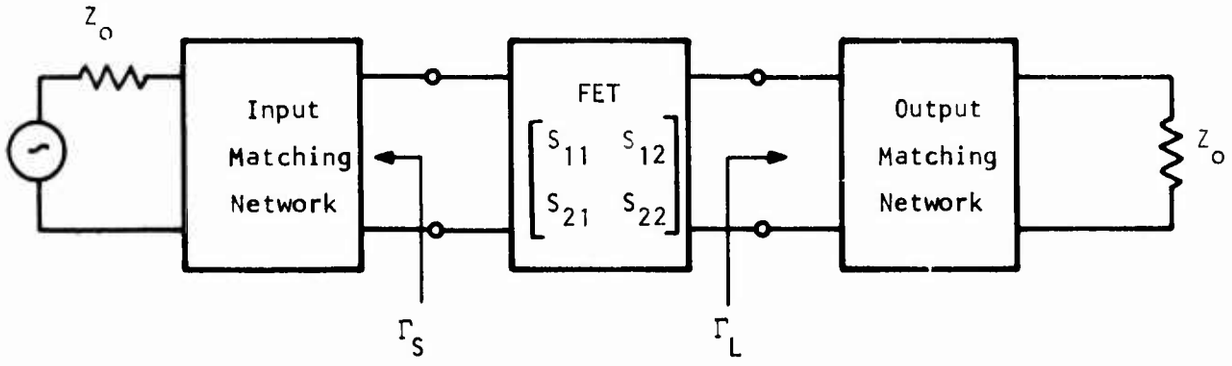


Figure 35 Simplified Block Diagram of an FET Amplifier

impedance Z_o (usually 50 ohms) to an impedance with the reflection coefficient Γ_L. When the desired Γ_s and Γ_L are known, the matching networks can be synthesized in terms of known circuit topologies.

C. Single-Stage FET Amplifier

The design approaches outlined above have been used in the development of a simple, compact microstrip circuit capable of wideband operation of FET amplifiers using devices with various gate widths. Figure 36 shows a photograph of the simple circuit. The circuit consists of two short sections of impedance transformers ($\sim 0.15\ \lambda$) and a short length of edge-coupled filter ($\sim 0.18\ \lambda$). This matching circuit is less than 0.300 inch long and has been used for the matching of the input and output impedances of the power FET. The edge-coupled filter section also serves as a dc block for the input and output of the amplifier. Microwave tuning has been accomplished by a selective bonding of gold straps to the "tuning pads" that can be seen in the photograph adjacent to the impedance transformers. A fairly wide range of circuit impedances with desirable reactance slope parameters can easily be obtained. The FET device was mounted upright on a Au-plated Cu block sandwiched between the input and output circuits. This device mounting scheme insures a good rf ground plane and allows for easy device and circuit replacement. Minimum thermal resistance was also obtained by mounting the FET directly on the copper block.

Figure 37 demonstrates the bandwidth capability of the circuit described above. A bandwidth of 3 GHz (7 to 10 GHz) and a gain of 6 ± 1 dB were achieved for a device with a gate width of 600 μm. With a 2400 μm gate-width device, an output power of 1 watt with 4 dB gain and 24.3% power-added efficiency was obtained at a frequency of 9.8 GHz.

D. Multistage Amplifiers

Prior to the final integration of the three-stage FET amplifier, FETs with various gate widths are tuned for maximum gain at the required rf input levels

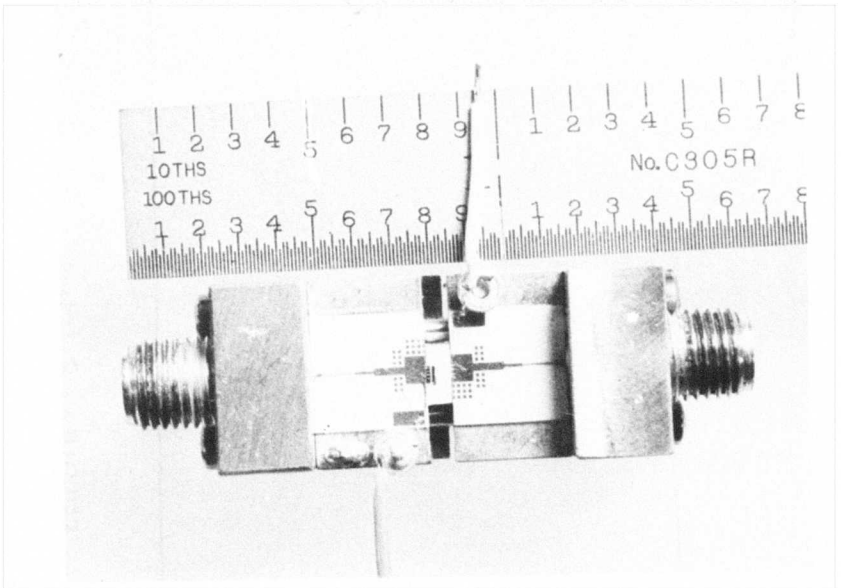


Figure 36 A Simple Microstrip FET Amplifier

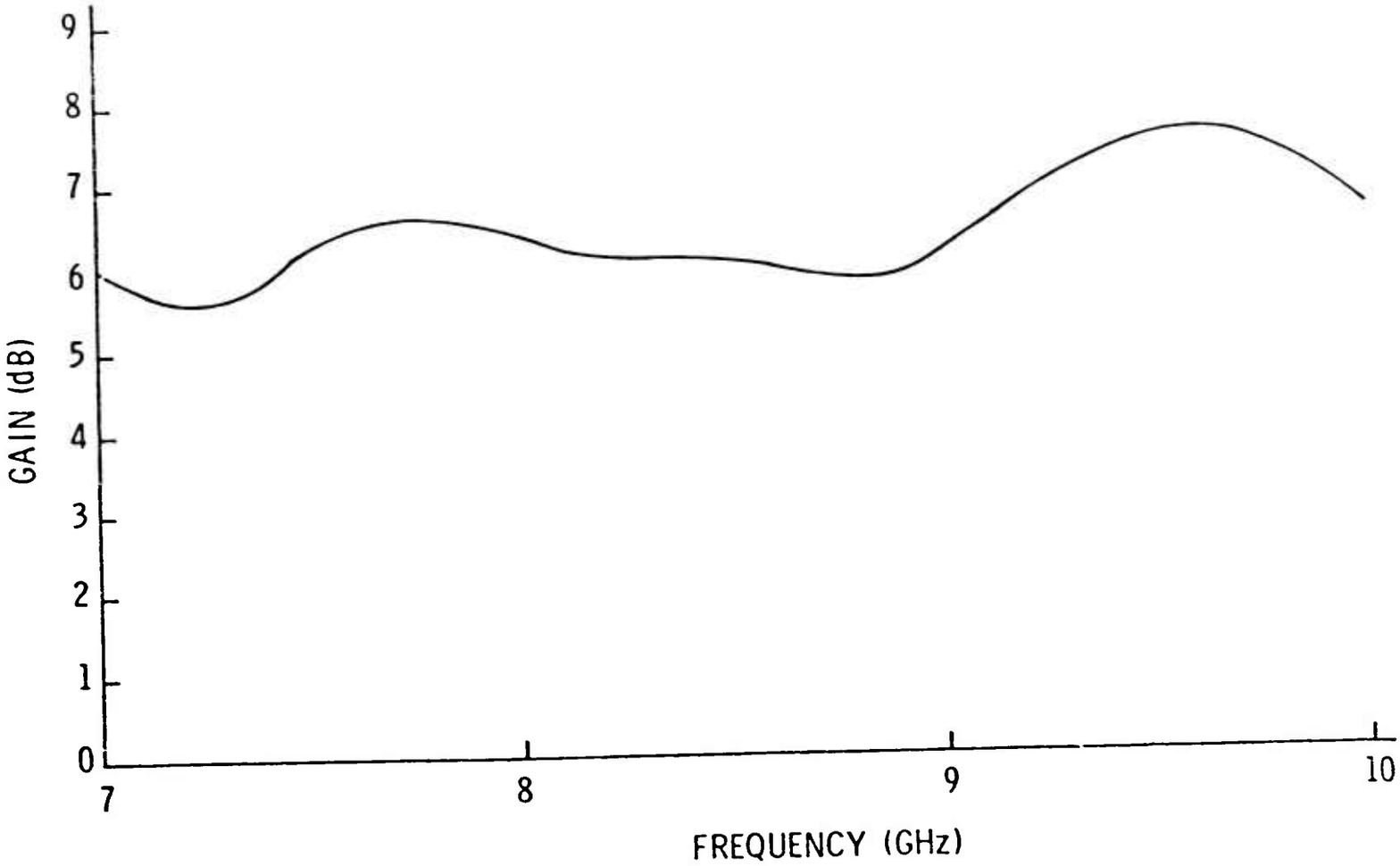


Figure 37 Gain-Frequency Response of a Single-Stage GaAs FET Amplifier

under optimum bias conditions. As discussed in Section VI.C, the circuit shown in Figure 36 was used exclusively for this purpose. To handle the increased output power requirement for the power amplifier stage(s), a proportionately larger gate-width device was used. Single-, two-, and three-cell FETs are used for the first, second, and third stages, respectively. The use of increasingly larger gate-width devices for higher power stages not only increases the reliability, but also enhances the linearity of the amplifier.

Figure 38 shows the gain compression characteristics of a prototype four-stage microstrip FET power amplifier. A linear gain of 20.4 dB and an output power of 350 mW (1 dB gain compression) were achieved at 9.8 GHz. At an increased drive level of 10 mW, the amplifier delivered 500 mW at 17 dB gain.

To achieve the one-watt output power goal, a single-stage, X-band IMPATT amplifier was constructed. A double-mesa, X-band IMPATT diode with a breakdown voltage of $\sim$ 60 volts was used for this purpose. An amplifier gain of 6 to 7 dB at an output power of 1 watt and 10% efficiency can easily be achieved for the desired frequency band.

A breadboard hybrid amplifier with IMPATT output stage was built by cascading the FET and IMPATT amplifiers described above.

E. Module Integration

Figure 39 shows a photograph of a completely integrated three-stage FET amplifier module. Cascading is achieved by removing the input/output OSM connectors used for testing the individual stage. Three stages are then cascaded by bonding a gold strap between the input and output transmission lines. Each of the amplifier stages is then screwed down to the amplifier housing from the bottom side. The bias network for each stage consists of simple RC network

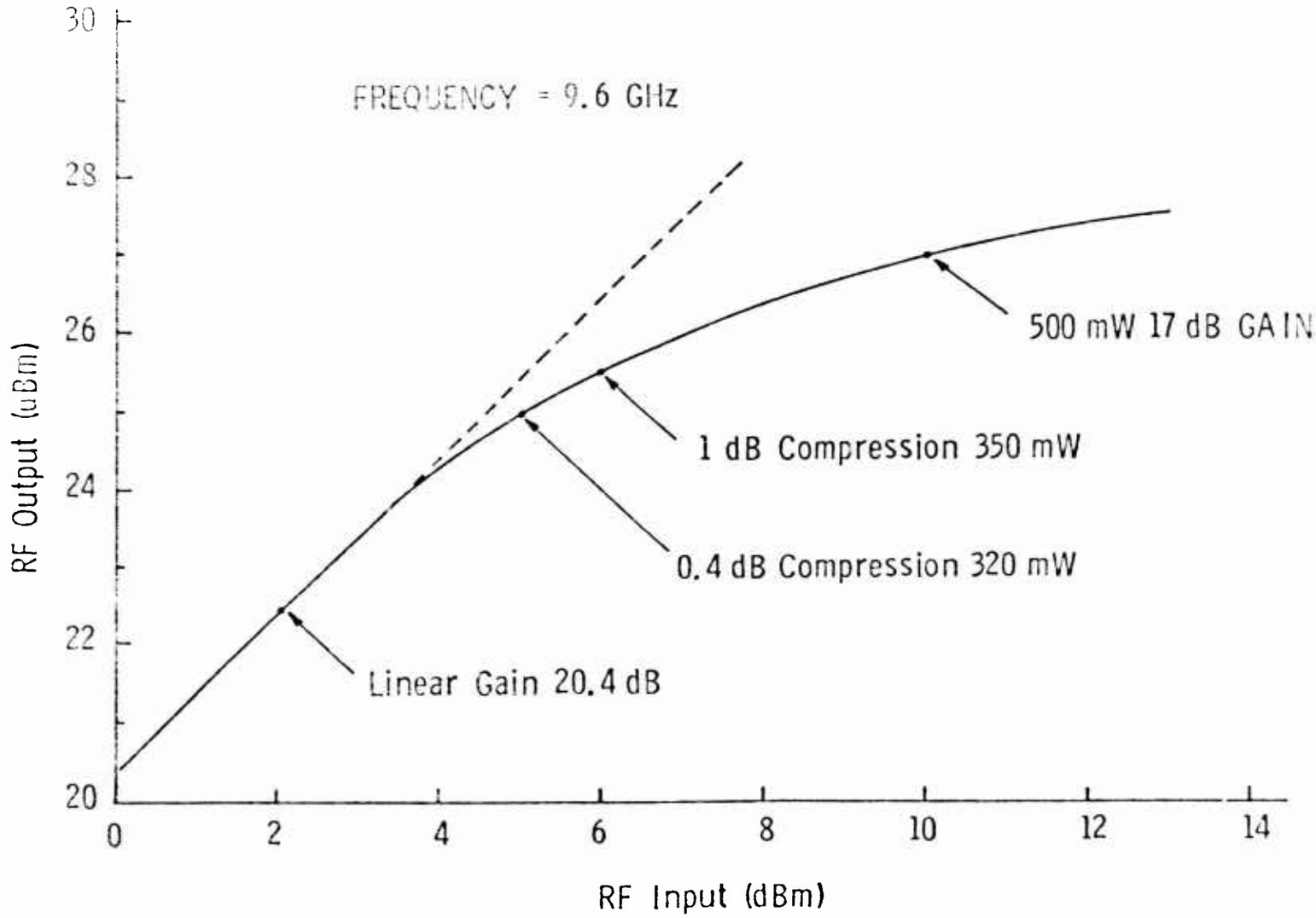


Figure 38 Gain Compression Characteristics of a Four-Stage Prototype FET Power Amplifier

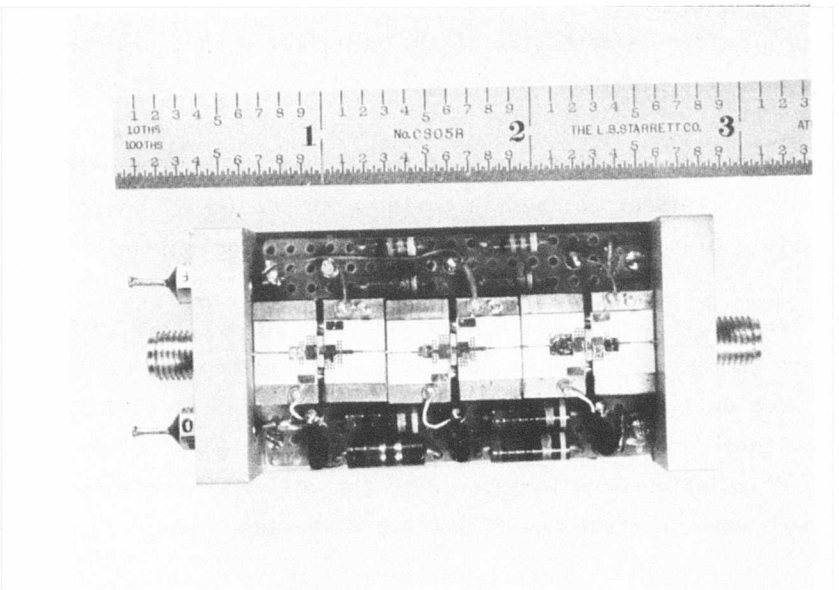


Figure 39 Photograph of Three-Stage Power FET Amplifier

for both the drain and gate. A 0.068 μF chip capacitor is placed near the bias choke of the gate to eliminate the low-frequency instabilities. The bias networks are provided on each side of the amplifier with a removable circuit board. Two bias pins are provided for the gate and drain dc supplies.

Figure 40 shows a photograph of the four-stage hybrid/IMPATT amplifier. A 50-ohm bias resistor is used in series with the IMPATT power supply to eliminate possible bias line oscillation under large-signal conditions.

At the completion of the GaAs power FET contract, two three-stage FET amplifiers (B1 and B2) and two FET (three-stage)/IMPATT hybrid amplifiers (D1 and D2) were delivered to AFAL for evaluation. Test data such as gain-frequency response, intermodulation distortion, input/output VSWR, noise figure and efficiency calculation were included with the delivered amplifiers. Representative performance data on these amplifiers are discussed below.

- Output Power - Frequency Response

Figure 41 shows the output power - frequency response of a three-stage FET amplifier (B1) as a function of drain voltage for a fixed rf input level of +5 dBm. At a drain voltage of 8 volts, an output power (cw) of 360 mW was achieved with a gain of 20.5 dB at 9.3 GHz. A gain of 20 $\pm$ 0.5 dB was obtained over the frequency range from 9.1 to 9.8 GHz. The 3 dB bandwidth is 1 GHz (8.9 to 9.9 GHz).

Figure 42 displays the output-power-frequency response of an FET (three-stage)/IMPATT hybrid amplifier. Output power of 1.2 watts with 26 dB gain was obtained at 9.5 GHz. The 3 dB bandwidth is 700 MHz (9.1 to 9.8 GHz).

- Input/Output VSWR

Input/output VSWR measurements were performed on the amplifiers that were delivered. In general, a better than 2.5:1 VSWR can be obtained within

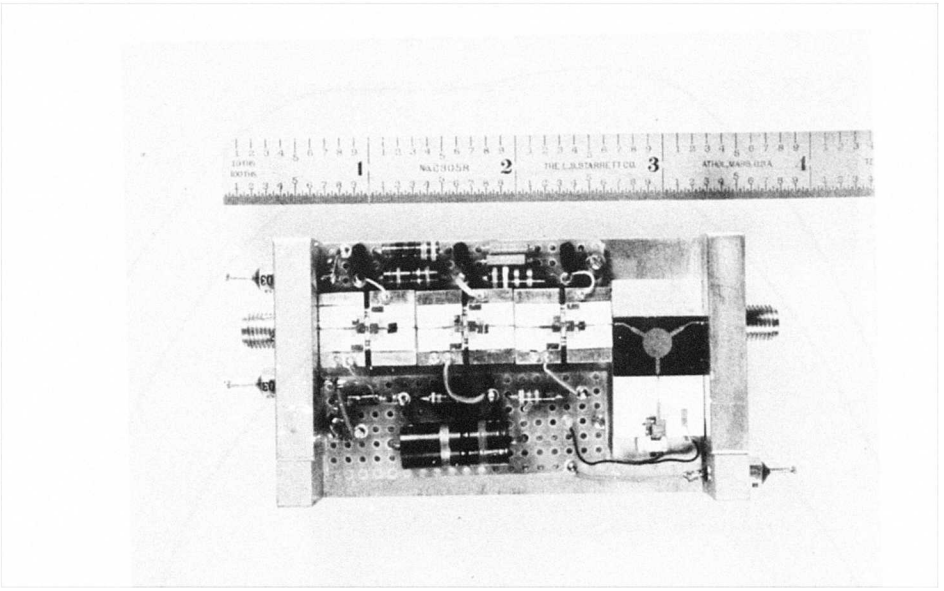


Figure 40 An FET (Three-Stage)/IMPATT Hybrid Amplifier

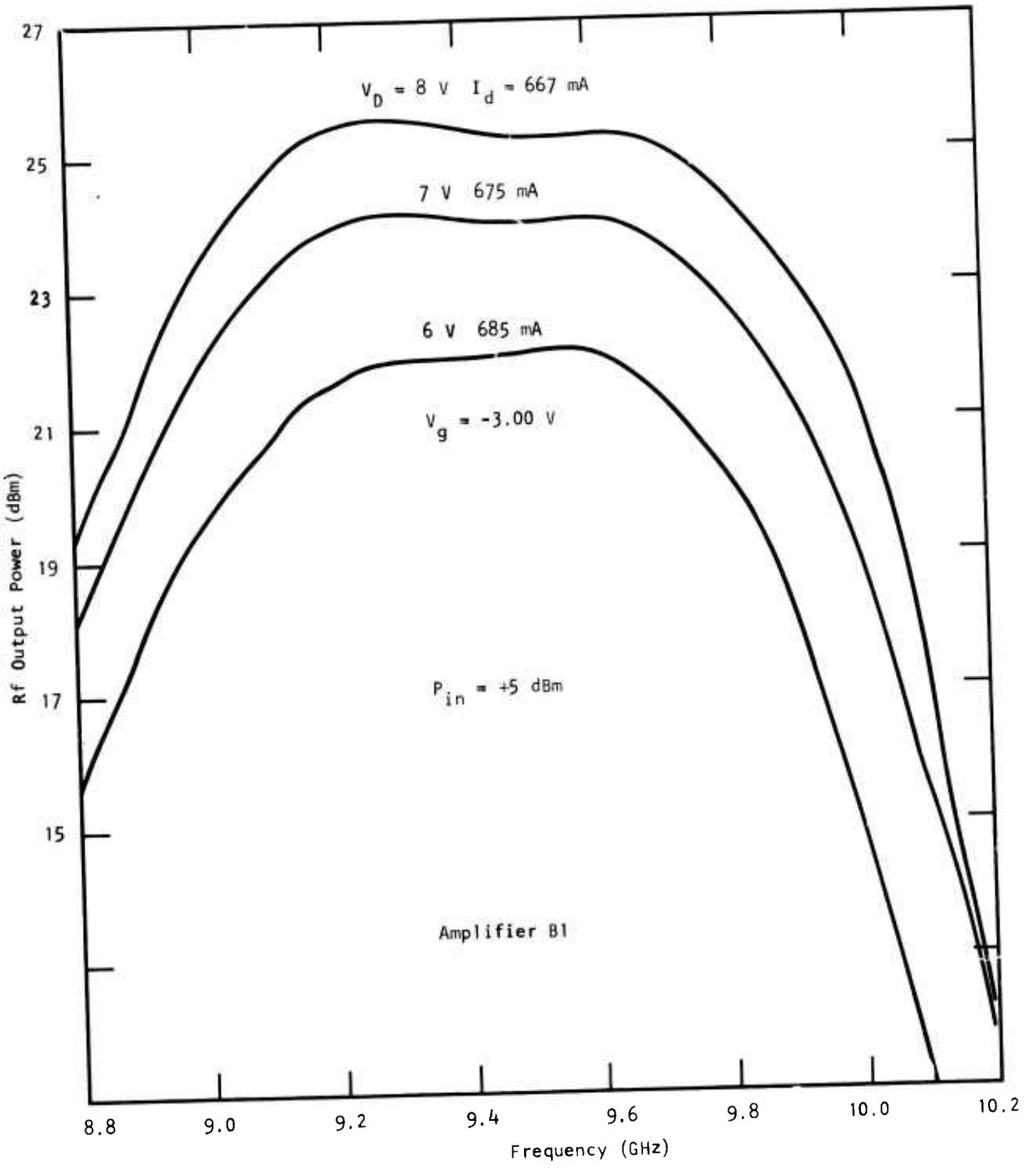


Figure 41 Output Power Versus Frequency Response of the FET Amplifier Shown in Figure 39

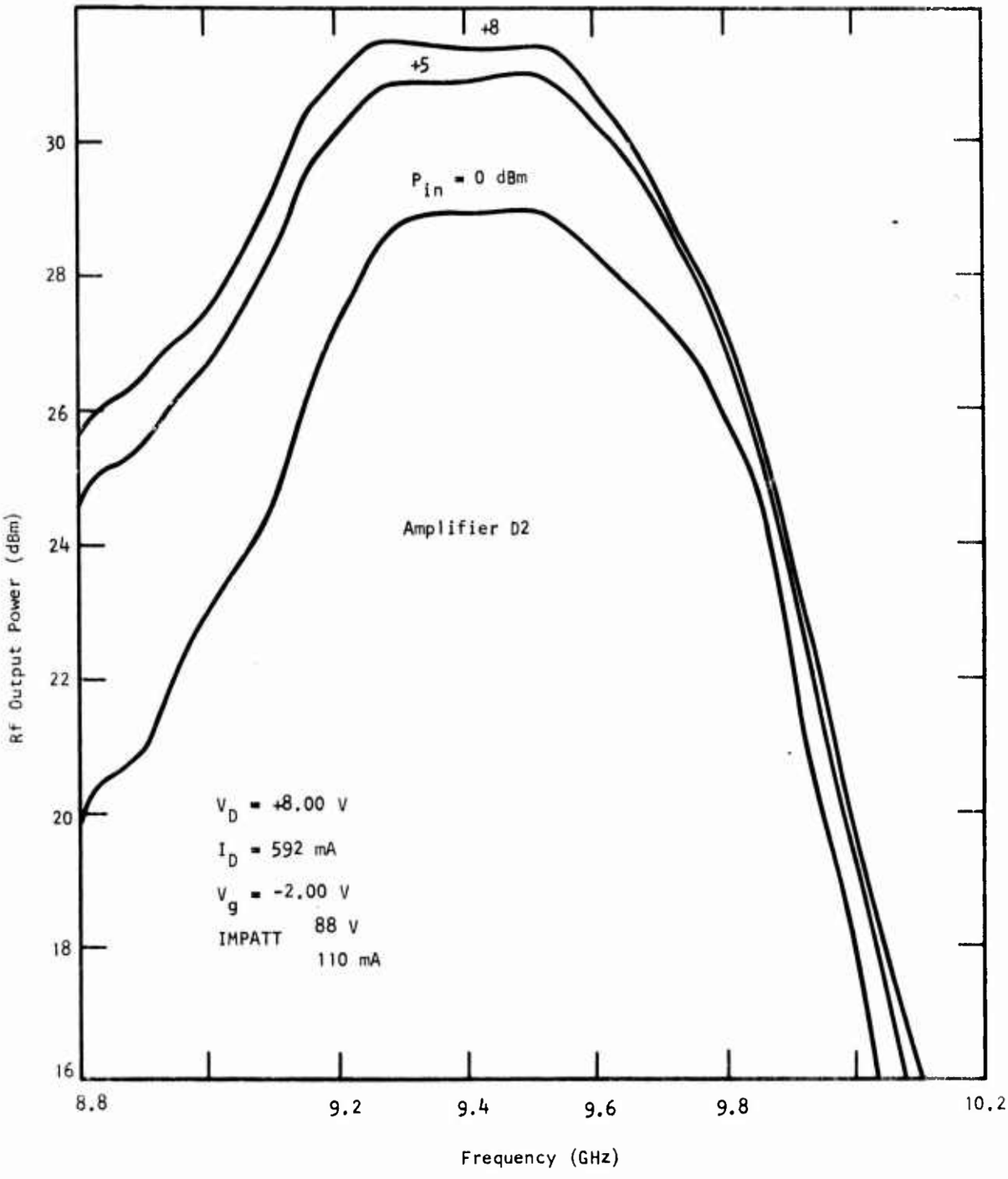


Figure 42 Output Power Versus Frequency Response of the FET/IMPATT Hybrid Amplifier Shown in Figure 40

the frequency band of the FET amplifier. However, a finite small-signal gain was measured when the output VSWR measurements on the hybrid amplifier were attempted. This is due to the mismatch between the output of the third stage of the FET amplifier and the input part of the circulator. This has the effect of reflecting a part of the measuring signal to the device port. This reflected signal is then amplified and circulated into the output port. For applications where a stringent output VSWR requirement is imposed, an output isolator can be installed to circumvent this problem.

- Efficiency

Bias circuit losses were included in the power-added efficiency for these amplifiers. Since these amplifiers were designed for class A operation, high efficiencies are not expected. An overall efficiency of 6 to 7% was measured for the three-stage FET amplifier. Power-added efficiency of 10 to 11% was achieved with the IMPATT stage alone. The highest efficiency measured for the hybrid amplifier was $\sim$ 8%.

- Intermodulation

Third-order intermodulation distortion is measured by injecting two equal amplitude signals separated in frequency by 10 and 50 MHz and located at the band edges and at band center. The input level of the two signals is increased from -20 dBm to +8 dBm while recording the amplitude of the third-order intermodulation product. Figures 43, 44, and 45 show the fundamental signal output and the third-order intermodulation product versus the input level at the lower band edge, upper band edge, and center frequency, respectively, for an FET amplifier. Figures 46, 47, and 48 present the same type of data for an FET/IMPATT amplifier. From these measurements it can be shown that:

(1) The third-order distortion is not sensitive to the frequency separation of the two input signals. This is especially true for the FET amplifier.

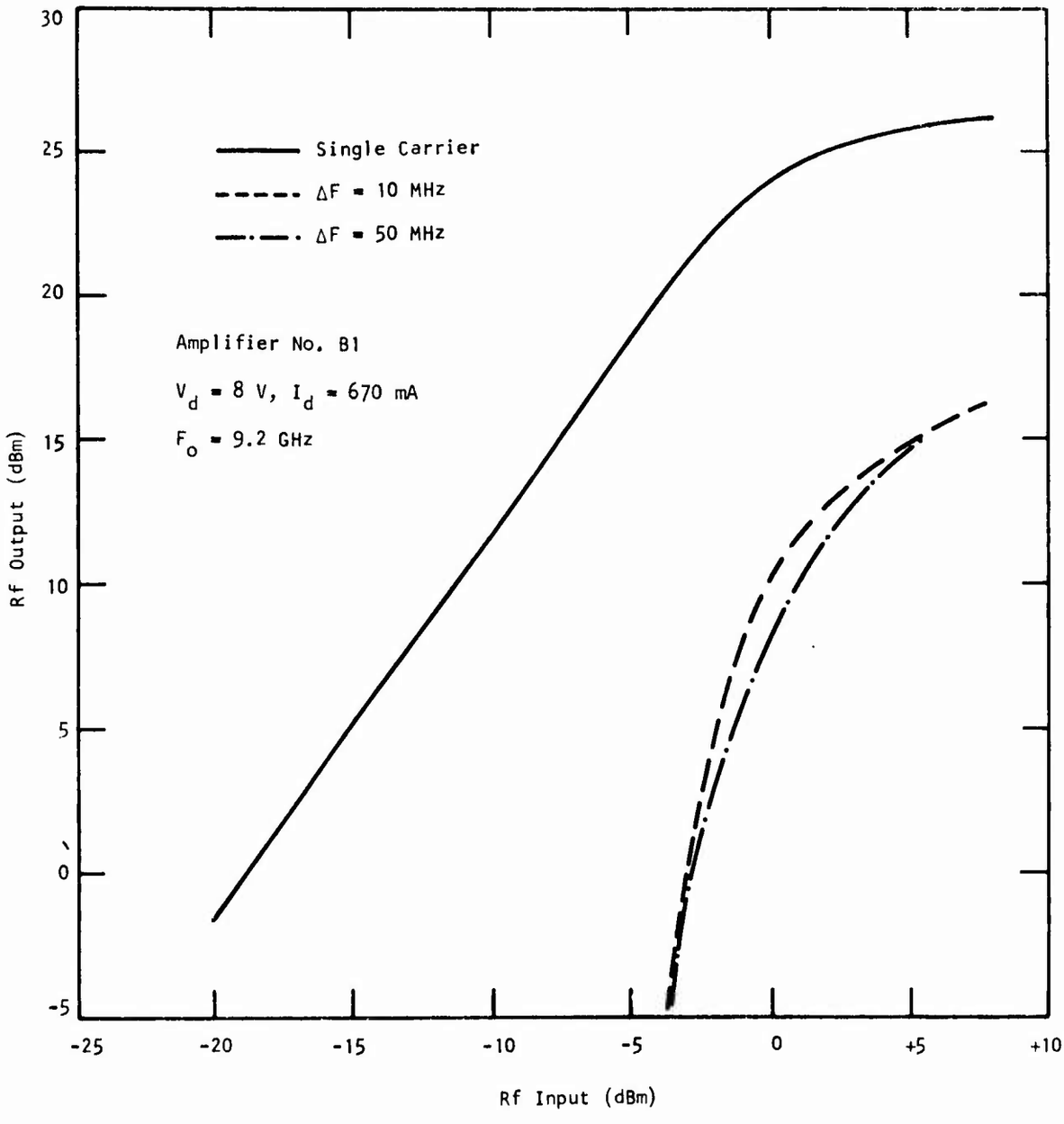


Figure 43 Third-Order Intermodulation Product vs Input Level at Lower Band Edge of the Three-Stage FET Amplifier

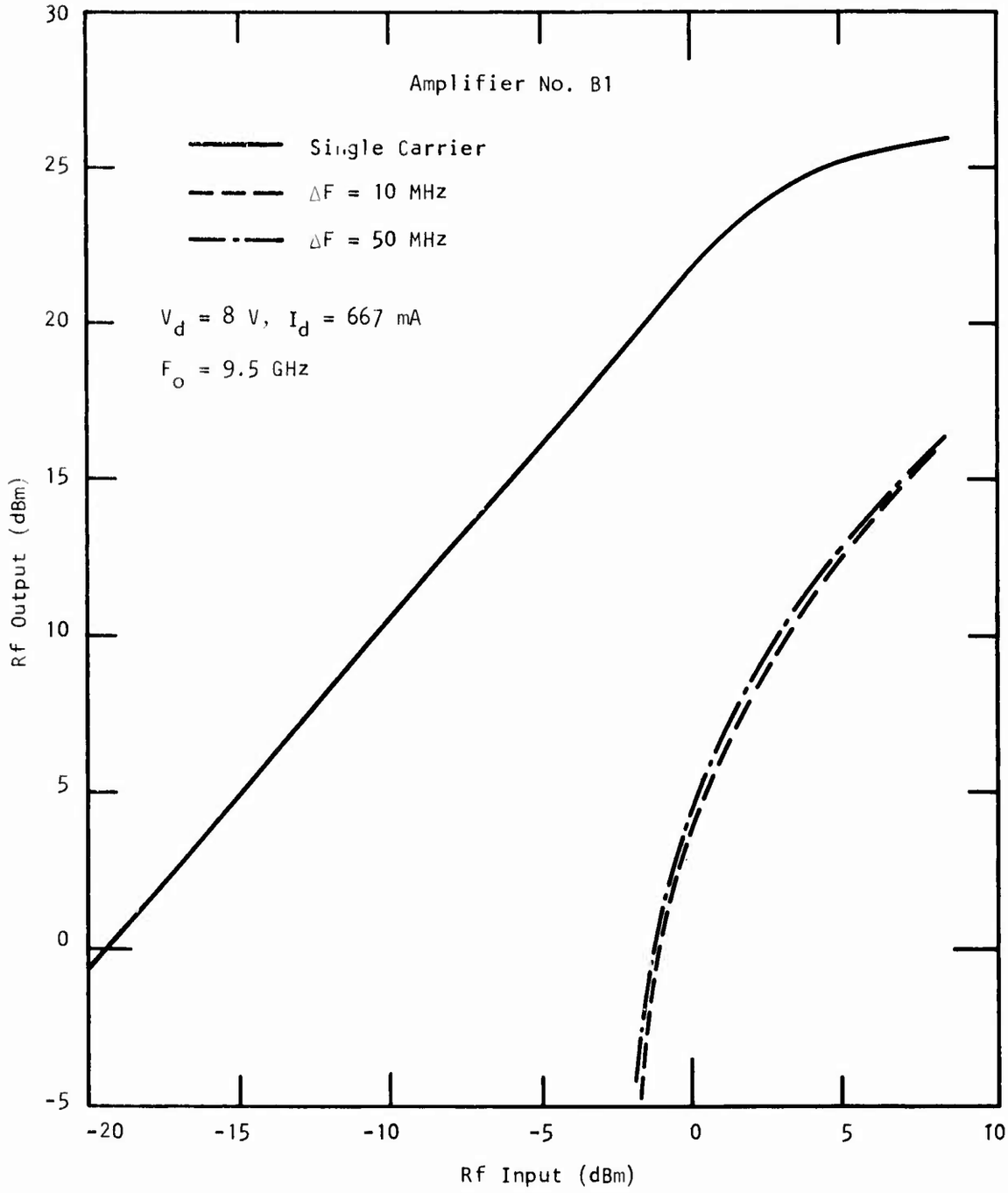


Figure 44 Third-Order Intermodulation Product vs Input Level at Band Center of the Three-Stage FET Amplifier

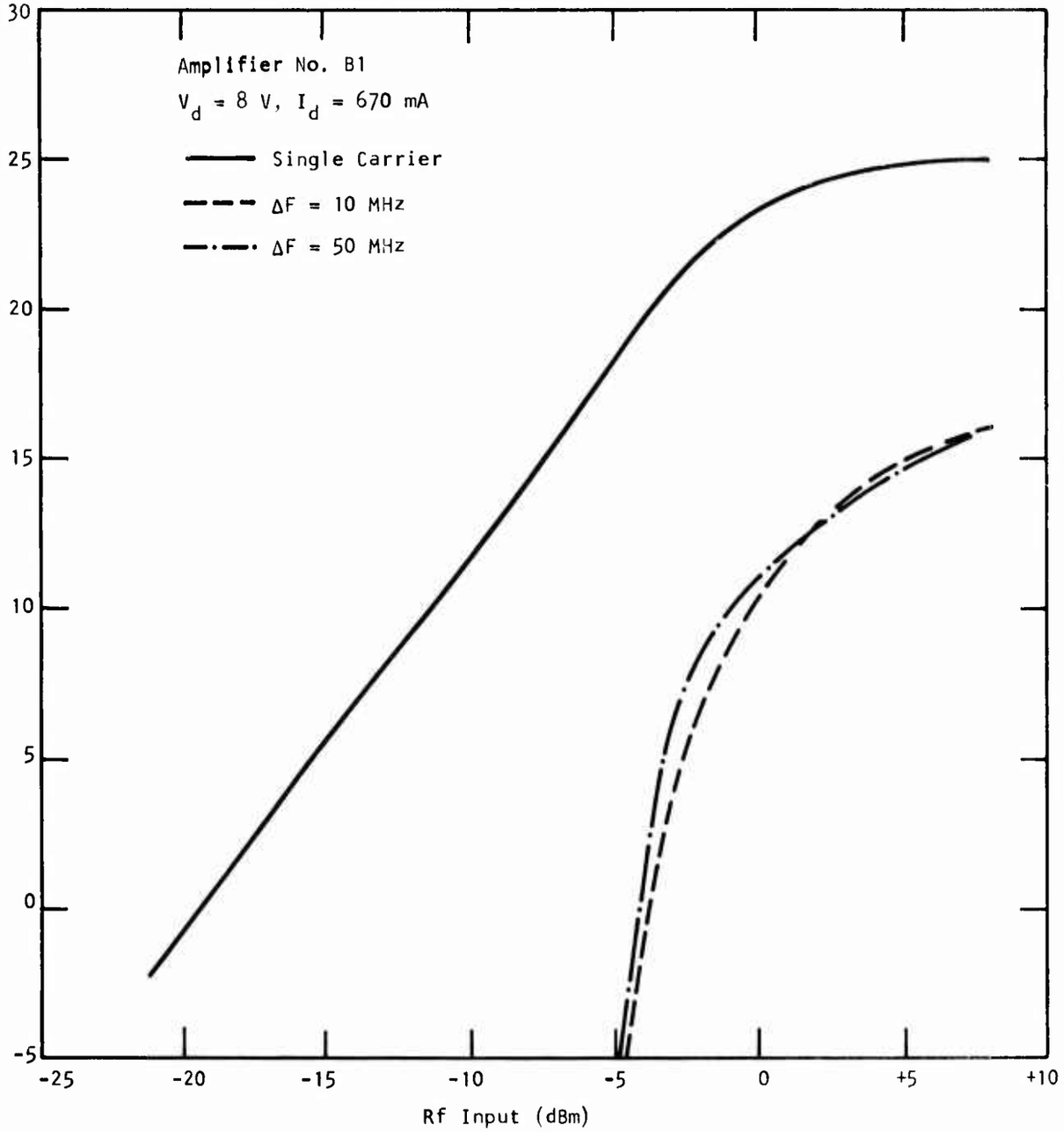


Figure 45 Third-Order Intermodulation Product vs Input Level at Band Center of the Three-Stage FET Amplifier

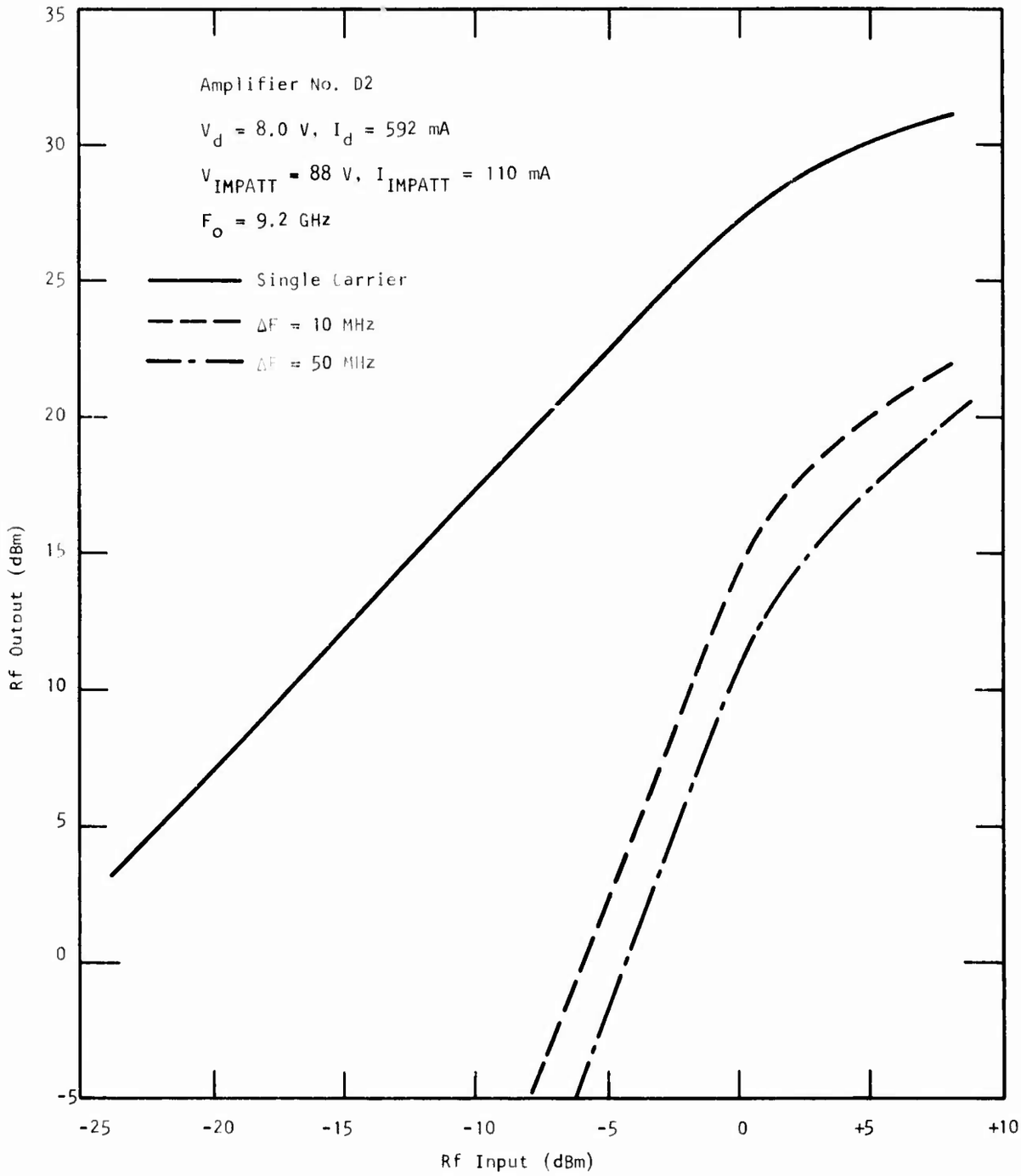


Figure 46 Third-Order Intermodulation Product vs Input Level at the Lower Band Edge of the Hybrid Amplifier

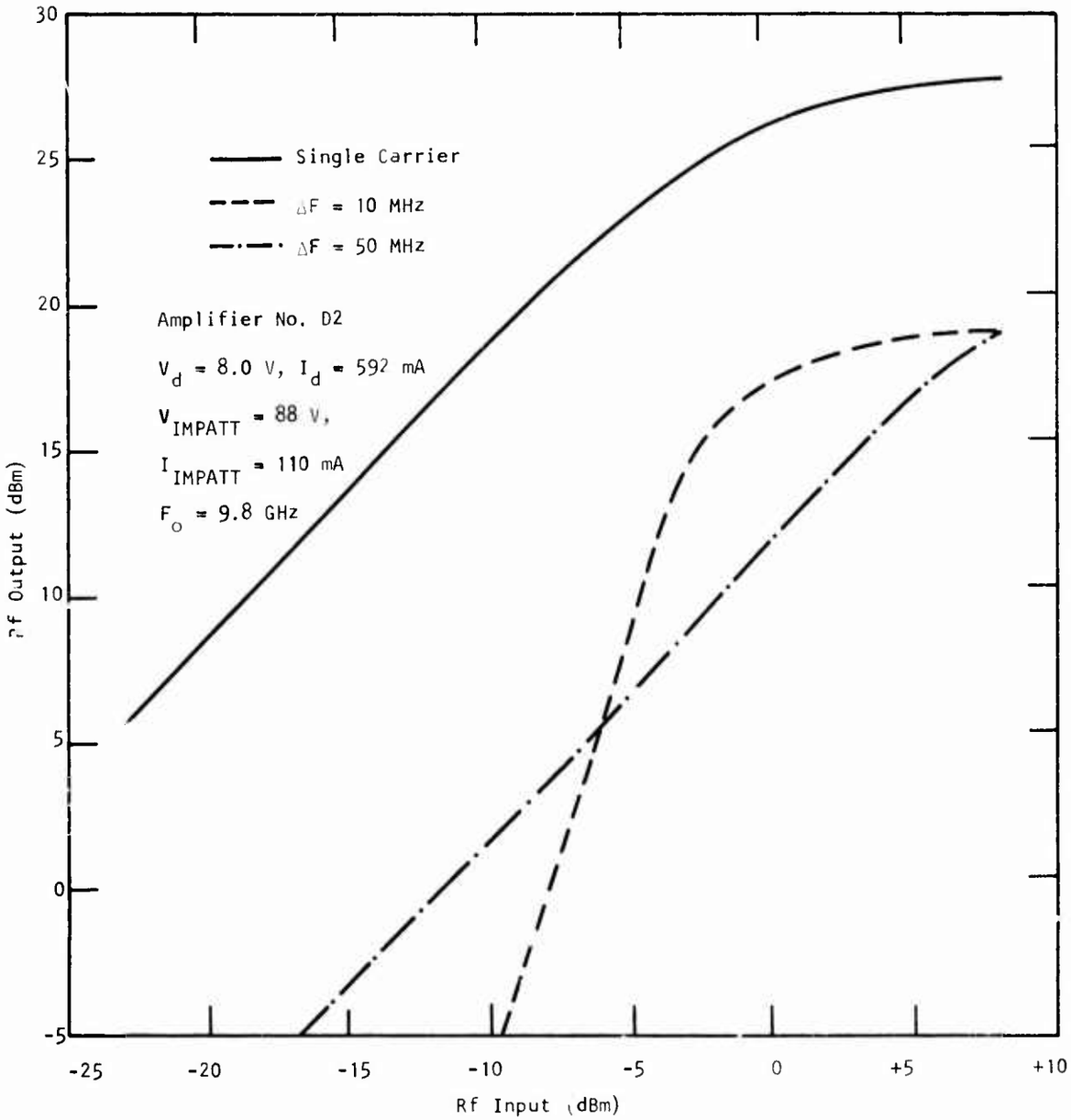


Figure 47 Third-Order Intermodulation Product vs Input Level at the Upper Band Edge of the Hybrid Amplifier

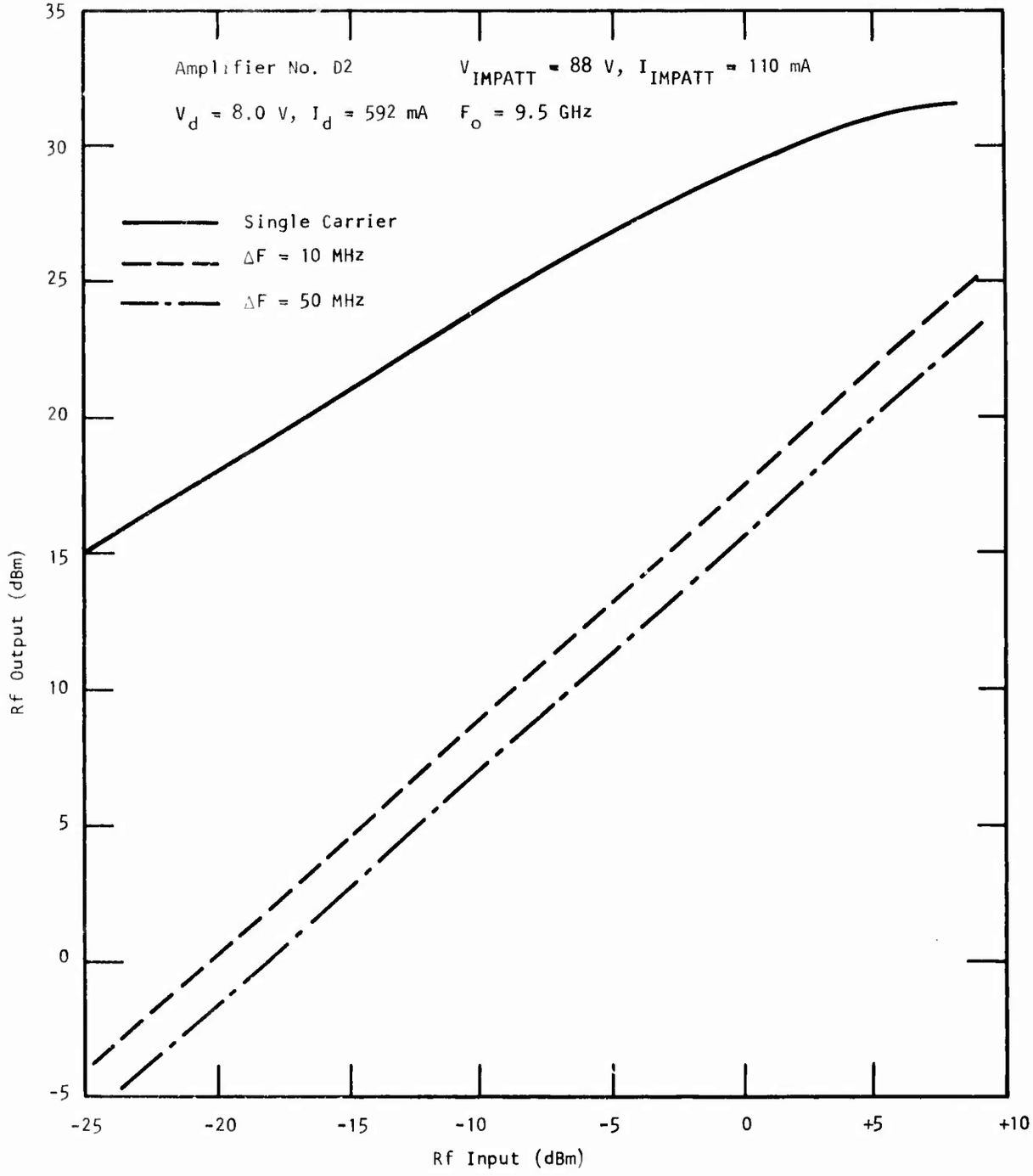


Figure 48 Third-Order Intermodulation Product vs Input Level at the Band Center of the Hybrid Amplifier

(2) The third-order distortion of the FET amplifier is essentially independent of frequency within the amplifier pass band. The output power is typically 20 dBm (100 mW) at a third-order intermodulation level of -20 dB.

(3) The distortion is more severe with the hybrid amplifier than with the FET amplifier alone for rf input levels between -20 dBm and 0 dBm. This is to be expected, since the highly nonlinear avalanche process of the IMPATT diodes will undoubtedly add to the third-order distortion even under medium signal conditions.

- Noise Figure

Small-signal noise figure measurements were made on the two three-stage FET amplifiers and on the two four-stage hybrid amplifiers at 9.2, 9.5, and 9.8 GHz. These measurements were made using the so-called Y-factor method in which a calibrated noise source, connected to the input of the amplifier under test, is turned on and off manually, and a superheterodyne receiver is used for the measurement of the resultant change in detected noise power from the unfired to the fired condition. The Y factor is just the ratio of the available noise power at the output of the receiver system with the noise source on to that of the available output noise power with the noise source off. The noise figure of the system, F_s, which includes the noise contributions of the amplifier under test and of the various amplifying stages of the receiver, is related to the Y factor by

$$F_s = \frac{(n - 1)}{Y - 1} \quad , \tag{16}$$

where (n - 1) is the excess noise ratio of the calibrated noise source. In these measurements an argon discharge tube in X-band waveguide with a fired excess noise ratio of 15.5 dB was used as the calibrated noise source.

A block diagram of the noise figure measuring system is shown in Figure 49. The blocks within the dashed lines represent the various components comprising the superheterodyne receiver. The local oscillator drives a pair of diodes in a balanced mixer, and the resultant down-converted noise power is amplified by the 30 MHz IF preamplifier (with an approximate 50 dB gain and a 4 MHz bandwidth). After passing through the precision IF attenuator, the signal is further amplified by the IF post-amplifier (with a 1 MHz bandwidth), detected, and finally displayed on the meter that shows the relative amplitude of the average detected noise power. The precision IF attenuator is used to measure the Y factor by the substitution method; i.e., with the noise source off, a datum on the detector meter is established; the noise source is then fired; and the datum is reestablished by inserting the required amount of attenuation. The Y factor is read directly off the calibrated attenuator dial. Note that in the above receiver system the image frequency response is included so that the detected noise power corresponds to the noise present in two 1 MHz windows situated symmetrically 30 MHz away from the L. O. frequency. Consequently, the resultant noise figure measurement is an average of the spot noise figures 30 MHz away on either side of the L. O. frequency. The isolator between the output of the amplifier under test and the input of the balanced mixer is necessary to prevent L. O. power from entering the output port of the amplifier under test. This is especially important in testing amplifiers having an IMPATT output stage, as will be explained later. The termination in front of the argon discharge tube provides a room temperature resistive termination to the amplifier under test during the unfired condition.

In order to retrieve the noise figure of the amplifier under test, F_1, from the measured overall noise figure of the system, F_s, Friis' formula is used. It is given by[15]

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots , \qquad (17)$$

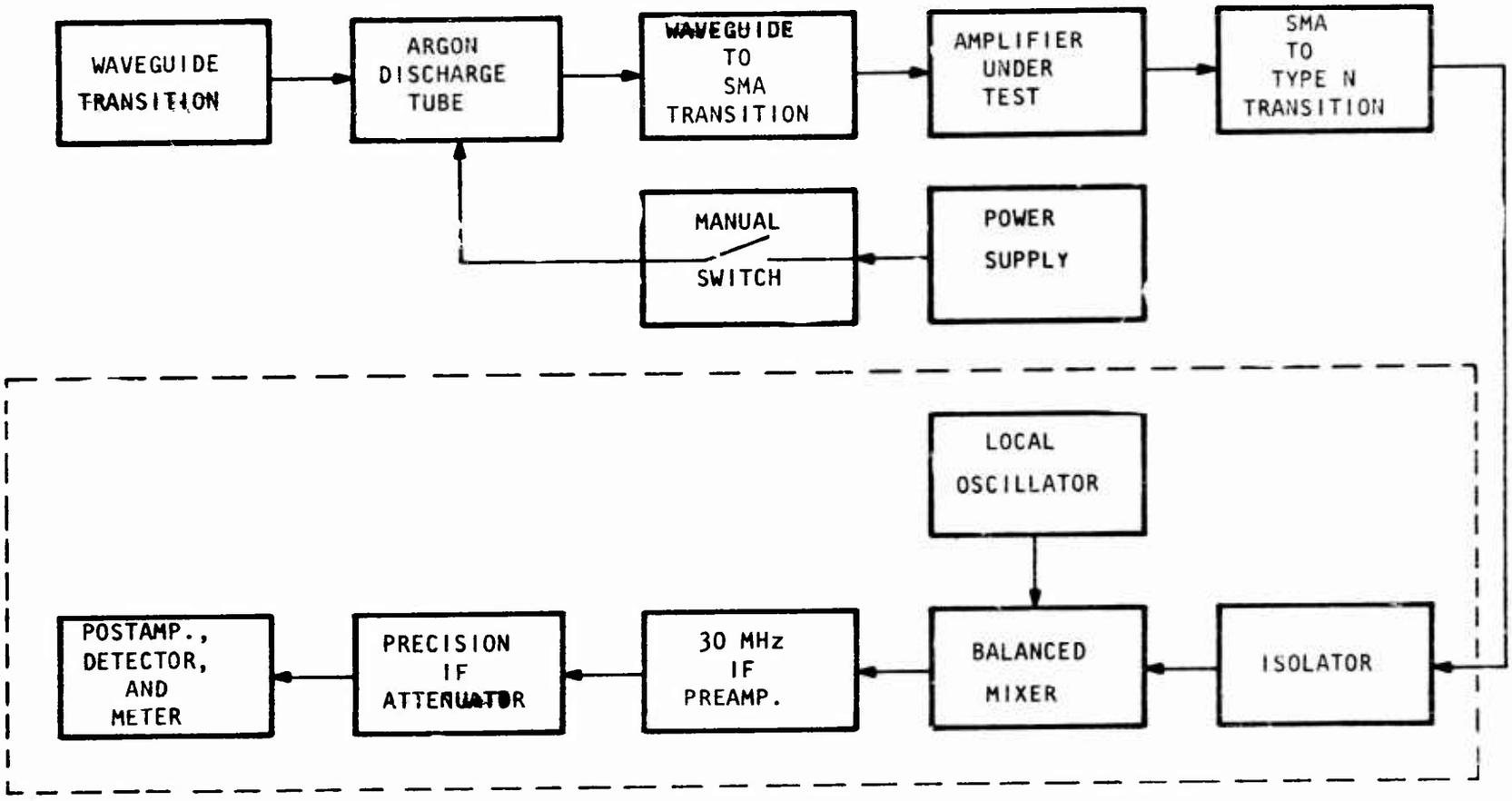


Figure 49 Block Diagram of Noise Figure Measurement System

where F is the overall noise figure, F_n is the noise figure of the nth stage, and G_n is the available gain of the nth stage. It can be seen from Equation (17) that if the gain, G_1, of the first stage is high, the measured overall noise figure closely approximates the noise figure of the first stage, F_1. In the noise measurements described here the noise figure, F_2, of the receiver alone (outlined by dashed lines in Figure 49) was measured at the three frequencies with the following results: F_2 = 10.7 dB @ 9.2 GHz; F_2 = 8.6 dB @ 9.5 GHz; F_2 = 9.0 dB @ 9.8 GHz. Therefore, the noise figure of the amplifier under test is given by

$$F_1 = F_s - \frac{F_2 - 1}{G_1} \qquad (18)$$

Since the small signal gain of the four amplifiers tested is at least 15 dB ($G_1 \cong 30$) and F_2 and the noise figure of the receiving system is about 10 dB, the second term in Equation (18) constitutes a very small correction when compared to F_s, and could, for all practical purposes, be neglected.

The best noise figure data were obtained from the three-stage amplifier (B2) which has a noise figure of 12.2, 13.4, and 13.8 dB at 9.2, 9.5 and 9.8 GHz, respectively. No adjustment of the drain or gate voltages from the nominal values of 8.0 V and -2.0 V, respectively, has been made. Considering that this amplifier was not tuned for optimum noise figure, these encouraging measurements show that an FET X-band amplifier with more than 300 mW of output power is capable of at least a 13 dB noise figure. These specifications are not easily achieved (excluding parametric amplifiers) by either tube or solid state amplifiers.

Amplifier B1 is also a three-stage FET that has more than 20 dB gain and an output power of 300 mW. However, this amplifier has much higher noise figures, ranging from 24 dB to more than 30 dB. It is believed that this is

due to the fact that no attempt has been made to tune for optimum noise performance, and that the high noise figure data for this amplifier are due to an improper input circuit in that it does not present the optimum source impedance for best noise figure to the first stage FET. Adjustment of the drain and gate voltage has some influence, but is not significant enough to lower the values to the noise figures measured for amplifier B2.

For the measurement of the noise figure of amplifiers D1 and D2, which have an IMPATT output stage, the isolator shown in Figure 19 is essential. Without the isolator any L. O. power entering the output circulator would be guided to the output matching circuitry of the last FET stage with only a few tenths of a dB loss through the circulator. Any reflection that takes place at this point would be amplified by the IMPATT stage with a gain of about 15 or 16 dB, and this power would be fed directly back to the mixer crystals of the balanced mixer, causing gross errors in the measured noise figure. In fact, if the balanced mixer has a significant input mismatch, oscillations at the L. O. frequency can take place. The isolator used in the measurements described here had 10 dB of isolation and proved adequate.

The noise figures of amplifier D1 and D2 have higher values than amplifier B2, but lower than amplifier B1. D1 has values ranging from 17 dB to 20 dB, depending on the bias voltage. The lower noise figures are generally obtained at reduced drain voltages, i.e., reduced from the nominal values of 8 volts suitable for maximum power and gain. Lowering the voltage too much, however, again increases the noise figure, and the best noise figures of about 17 dB are measured at a drain voltage of 6 volts and gate voltage of -2.0 V. The change in noise figure with bias is most probably due to changes in the input impedance of the FET stages, resulting in better or poorer source impedance combinations that affect noise figure performance.

Amplifier D2 exhibits noise figures ranging from about 14 to 20 dB, with the lower noise figures occurring for a reduced drain voltage of 7 volts. Increasing the gate voltage results in only a few tenths of a dB improvement in noise figure.

To assess the noise contribution from the IMPATT stage, several measurements were made with the IMPATT off while maintaining the same bias conditions on the FET stages. For amplifier D2 improvements in the noise figure ranged from 0.9 to 3.6 dB, while for amplifier D1 improvements from 1.9 to 3.6 dB were observed. Using a typical case of amplifier D1, a noise figure of 15.9 dB at 9.5 GHz was measured with the IMPATT off and the FET stages biased at V_o = 6 V and V_G = -2.0 V. With the same FET bias and with the IMPATT on, the noise figure increased to 19.2 dB. If Friis' formula,

$$F_{12} = F_1 + \frac{F_2 - 1}{G_1} \quad , \tag{19}$$

is applied, assuming F_{12} = 19.2 dB, F_1 = 15.9 dB, and G_1 = 17 dB (the small signal gain of the three FET stages), then one can approximate F_2, the noise figure of the IMPATT stage. Doing this yields a value for F_2 of about 33 dB, which indeed is a reasonable noise figure for a GaAs IMPATT stage. Therefore, a 2 or 3 dB degradation in noise figure (from an initial 16 dB noise figure FET amplifier) can be expected when an IMPATT output stage is added. Again, it should be noted that both amplifiers D1 and D2 were not tuned for optimum noise performance, but rather for output power and gain. However, since the IMPATT stage is relatively noisy, fairly significant improvements in the three-stage FET noise figure or gain will yield only modest improvements in the overall hybrid amplifier noise figure. If in the previous example the FET stages are improved by 3 dB in noise figure to 12.9 dB, or if the gain is increased by 3 dB to 20 dB, an improvement of only about 1 dB occurs in the overall hybrid amplifier noise figure.

The above noise figure data taken from the four amplifiers demonstrate the existence of relatively high power (> 300 mW), low noise (< 13 dB) FET amplifiers. Since no attempt was made to design for low noise amplifier performance, it is believed that still lower values of noise figure with comparable output power can be achieved if design considerations for low noise performance as well as power and gain are taken into account.

SECTION VII

CONCLUSIONS AND RECOMMENDATIONS

All the goals of this program were successfully achieved, and power amplifiers that meet the design specifications were delivered to AFAL. Output powers at X-band were achieved that are higher than any previously reported and are more than an order of magnitude higher than those achieved at Texas Instruments at the beginning of the program.

Although a number of changes were made in the device design and in material and device fabrication procedures during this program, two changes were primarily responsible for the dramatic improvement in performance. The first was the reduction of parasitic resistances relative to the channel resistance under the gate. This was accomplished through the use of AuGe/Ni source and drain contacts and by etching a groove under the gate prior to metallization. The second change was the elimination of the alumina device carrier by mounting the devices directly on Au-plated Cu blocks. This resulted in improved thermal and electrical device properties.

These changes in fabrication and mounting have not only led to greatly improved microwave performance, but they have also resulted in a high degree of reproducibility across a slice and from slice to slice.

Several means for improving FET performance at X-band have been identified. Present results indicate that higher gains could be achieved at a given power level by using shorter gates. Results obtained with two chips connected in parallel could be improved by fabricating devices with the same total gate width on a single chip. Additional improvement in thermal resistance could be achieved by thinning the GaAs substrate to 3 mils or less.

There have been reports of increased contact resistance for FETs that have been subjected to prolonged periods at elevated temperatures while under bias conditions. Changes may be required in the choice of contact metallization to minimize this effect. It is recommended that this area be investigated as a part of future work on power FETs.

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