PCB Layout: The Impact of Lightning and Power-Cross Transients

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Helpful data can ease the process of designing for immunity to lightning and power-cross events to meet the requirements of GR-1089-CORE.

With the continuing efforts to increase product functionality while decreasing product size, designers are being asked to place more and more functionality on individual printed circuit boards (PCBs). As PCBs become more densely populated, many new challenges arise.

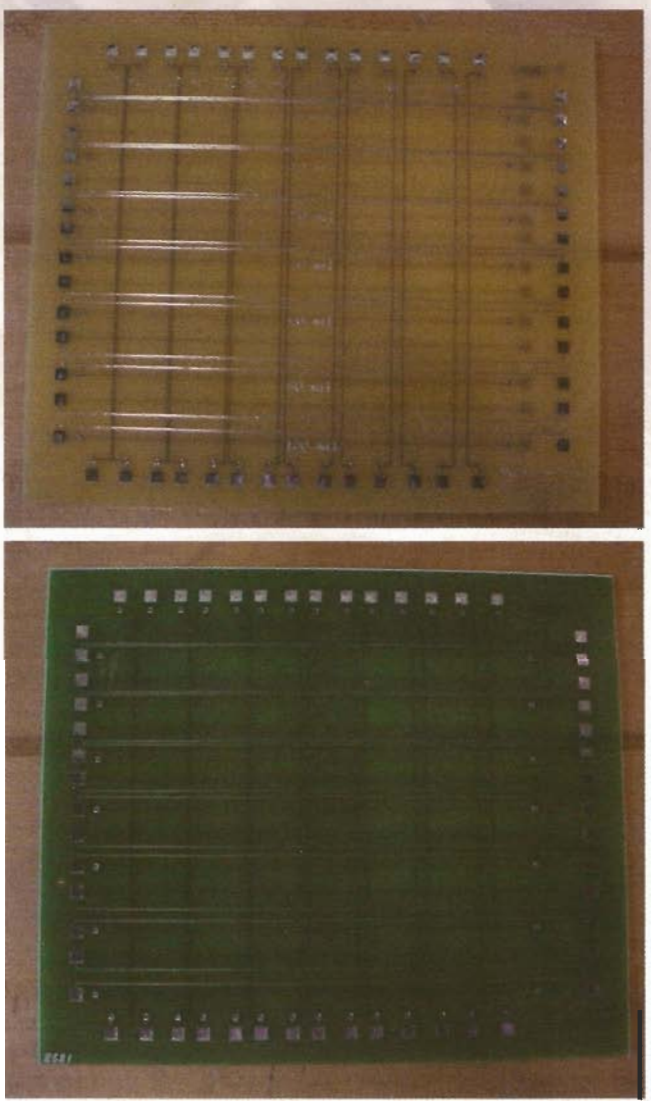
For boards containing circuits that interface with outside-plant tip/ring pairs, one such challenge is maintaining immunity to lightning strikes and unintentional power-line contact (power cross). This article explores this challenge as it relates to PCB layout. Through experimentation and analysis, this article provides designers with data to use as a tool when laying out circuits that will interface with outside plant wiring.

Limited Space

With product size decreased and component density increased, PCB real estate quickly becomes limited. Designers must decide on board dimensions, component placement, and layer count: factors that can affect both product performance and cost. This task is further complicated when the product in question contains circuits that could be exposed to external lightning and power-cross events.

Component and trace spacings are critical to avoid arcing during high-voltage transients. Trace width is critical to avoid blown traces during high-current transients. Although designers want to design products that are immune to such events, they do not want to overburden a design with placement and routing constraints that are excessive. To ensure optimum efficiency during board layout, designers must have a thorough understanding of the properties PCB traces exhibit during transient events. This article discusses the results of an experiment intended to quantify the physical characteristics of a multilayer PCB during high voltage and high current transients.

The findings were obtained by performing the following tests on multiple PCB test samples: 10 × 1000-microsecond, 1000-V, 100-A surge; 2 × 10-microsecond, 2500-V, 500-A surge, and one 600-V, 60-A power-cross transient. These events



Layout without solder mask (above) and with solder mask (below).

Trace Spacing (mil)	Surface Layer with Solder Mask (V)	Surface Layer No Solder Mask Clean (V)	Surface Layer No Solder Mask Hygro Dust (V)	Surface Layer No Solder Mask Flux (V)	Internal Layer (V)
7	3100	1320	620	250	>5000*
10	3500	1480	900	300	>5000*
20	3900	1620	1400	750	>5000*
40	4700	2300	2050	1300	>5000*
60	5000	3360	2820	2050	>5000*
80	>5000*	4160	3700	3000	>5000*
100	>5000*	4720	3850	3650	>5000*

*Note. Dielectric tester maximum voltage = 5000 V dc.

Table I. Trace dielectric properties, breakdown voltage.

Trace Thickness (mil)	Surface Layer Current No Solder Mask (A)	Surface Layer Current with Solder Mask (A)	Internal Layer Current (A)
7	600	900	400
10	900	>1000*	500
12	>1000*	>1000*	600
15	>1000*	>1000*	800
17	>1000*	>1000*	>1000*
20	>1000*	>1000*	>1000*
22	>1000*	>1000*	>1000*

*Note. Surge generator maximum 2 × 10 microseconds, current = 1000 A.

Table II. Trace current properties: 2 × 10 microseconds, 2500 V, 500 A, maximum current capacity.

were taken from Telcordia's GR-1089-CORE.[1] They represent the worst-case energy dissipation that a PCB can experience during formal testing and be expected to survive.

Although not required by GR-1089-CORE, it is advantageous for an overcurrent protection device to interrupt the 600-V, 60-A power-cross transient rather than the PCB traces. Interrupting the transient allows for repair of the product not only in the lab but also once installed in the field, which eliminates the cost of a new circuit pack.

The requirements detailed in GR-1089-CORE were developed around the performance characteristics of a standard 3-mil carbon block. The carbon block is considered to have the greatest let-through energy of all of the commonly used primary protectors in the telecommunications industry. Test samples were evaluated under various conditions to simulate not only ideal-case scenarios, but also real-world conditions a board might experience due to manufacturing issues and years of service in the field.

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Objectives

The experiment had five objectives, which are discussed below:

- To determine the minimum trace-to-trace spacing required on external and internal layers of a PCB to ensure no dielectric breakdown during the application of the 2500-V, 500-A, 2 × 10-microsecond first-level surge defined in GR-1089-CORE. To obtain values for a clean board, a board containing solder flux, and a board coated with the hygroscopic spray solution detailed in GR-63-CORE.[2]
- To determine the minimum trace-to-trace spacing required on external and internal layers of a PCB to ensure no dielectric breakdown during the application of the 1000-V, 100-A, 10 × 1000-microsecond first-level surge defined in GR-1089-CORE. To obtain values for a clean board, a board containing solder flux, and a board coated with the hygroscopic spray solution detailed in GR-63-CORE.
- To determine the minimum trace width required on external and internal layers of a PCB to ensure that a trace does not become an open circuit during the application of the 2500-V, 500-A, 2 × 10-microsecond first-level surge defined in GR-1089-CORE.
- To determine the minimum trace width required on external and internal layers of a PCB to ensure a trace does not become an open circuit during the application of the 1000-V, 100-A, 10 × 1000-microsecond first-level surge defined in

Trace Thickness (mil)	Surface Layer Current No Solder Mask (A)	Surface Layer Current with Solder Mask (A)	Internal Layer Current (A)
7	60	70	40
10	90	120	60
12	120	150	80
15	160	190	100
17	190	>200*	130
20	>200*	>200*	150
22	>200*	>200*	170

*Note. Surge generator maximum.

Table III. Trace current properties: 10 × 1000 microseconds, 1000 V, 100 A, maximum current capacity.

GR-1089-CORE.

- To determine the minimum trace width required on external and internal layers of a PCB to ensure the trace's fuse characteristics are greater than that of a Bussman Type MDQ 1-6/10-A fuse when subjected to the 600-V, 60-A second-level power-cross transient detailed in GR-1089-CORE.

Experiment

For this experiment, a four-layer PCB was designed by Underwriters Laboratories (UL) and fabricated by an outside board vendor. A four-layer board was chosen because it allowed for data collection on the surface as well as on the internal layers. Two batches of boards were fabricated, one with solder mask and one without. Each batch used the same trace layout. Figures 1–4 show a view of the trace layout for each layer. The photos show each type of board used. The physical specifications for the boards were as follows:

- Four-layer PCB measuring 4.00 × 4.75 in.
- Industry standard 0.062-in. FR-4 laminate.
- Standard 1-oz. finish copper weight.
- Dielectric constant of 4.6 (±0.2) for each layer.

Trace Thickness (mil)	Surface Layer No Solder Mask	Surface Layer with Solder Mask	Internal Layer
7	Trace	Trace	Trace
10	Trace	Trace	Trace
12	Trace	Trace	Trace
15	Trace	Fuse	Trace
17	Trace and Fuse	Fuse	Trace and Fuse
20	Fuse	Fuse	Trace and Fuse
22	Fuse	Fuse	Fuse

Table IV. Trace current properties: 600 V, 60 A, 5 seconds, interrupt device.

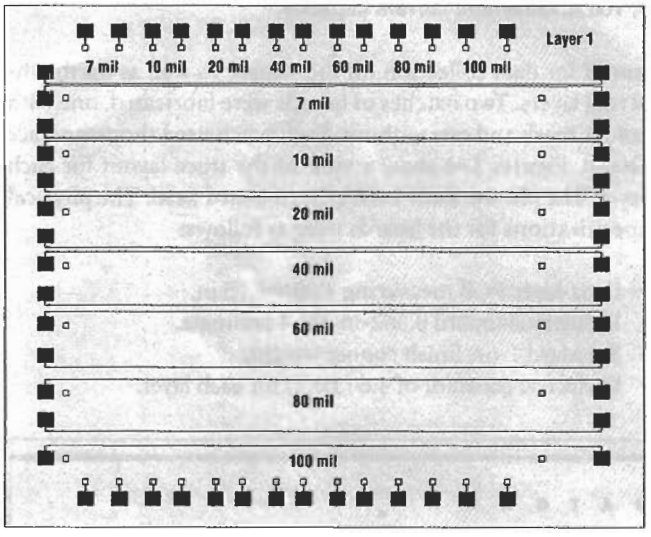

Figure 1. Trace layout, top layer. Varying trace spacing.

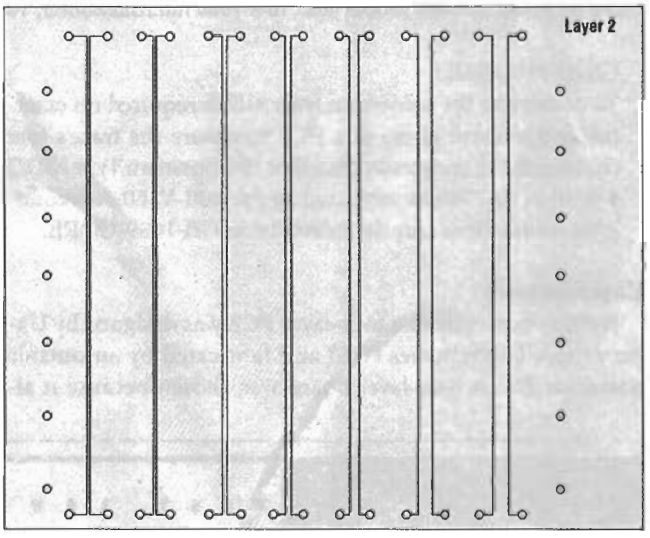

Figure 2. Trace layout, layer two. Varying trace spacing.

Dielectric Properties

To quantify the dielectric properties of the spaced traces on the PCBs, a calibrated dielectric withstand tester was used to apply a dc potential (maximum 5000 V) between the traces (see Figure 5). The following layers were evaluated:

- Surface layer with solder mask. The board was cleaned with flux cleaner to remove impurities.
- Surface layer with no solder mask. The board was cleaned with flux cleaner to remove impurities.
- Surface layer with no solder mask. The board was cleaned with flux cleaner to remove impurities and then coated with the hygroscopic dust solution described in GR-63-CORE. After drying for 24 hours, the board was then placed in a humidity chamber. The humidity was set at the value required to produce 1 MΩ on the IPC coupon detailed in GR-63-CORE. (IPC refers to Institute for Interconnecting and Packaging Electronic Circuits.)
- Surface layer with no solder mask. The board was cleaned with flux cleaner to remove impurities and then lightly coated with solder flux.
- Internal layer.

Current Properties

To quantify the current-carrying properties of the various traces, the boards were subjected to the 2500-V, 500-A, 2 × 10-microsecond lightning surge, the 1000-V, 100-A, 10 × 1000-microsecond lightning surge, and the 600-V, 60-A power-cross transient detailed in GR-1089-CORE. Tables I–IV and Figures 6–8 present the data gathered from the experiment.

A KeyTek (Lowell, MA) ECAT surge generator was used to produce the lightning waveforms, and a UL-built power-cross generator was used to produce the power-cross transient. Lightning waveforms were monitored using a calibrated digital oscilloscope (see Figure 9).

Power-cross values were monitored using calibrated digital meters (see Figure 10). The following layers were evaluated: surface layer with no solder mask, surface layer with solder mask, and internal layer.

Analysis

The experiment revealed minimum trace-to-trace spacing required on external and internal layers of a PCB. The minimum spacings to ensure no dielectric breakdown during the application of the 2500-V, 500-A, 2 × 10-microsecond first-level surge defined in GR-1089-CORE are as follows:

- < 7 mil for a surface-layer trace with solder mask.
- > 40 mil for a surface-layer trace with no solder mask and which is clean (free of dust and solder flux).
- > 40 mil for a surface-layer trace with no solder mask and

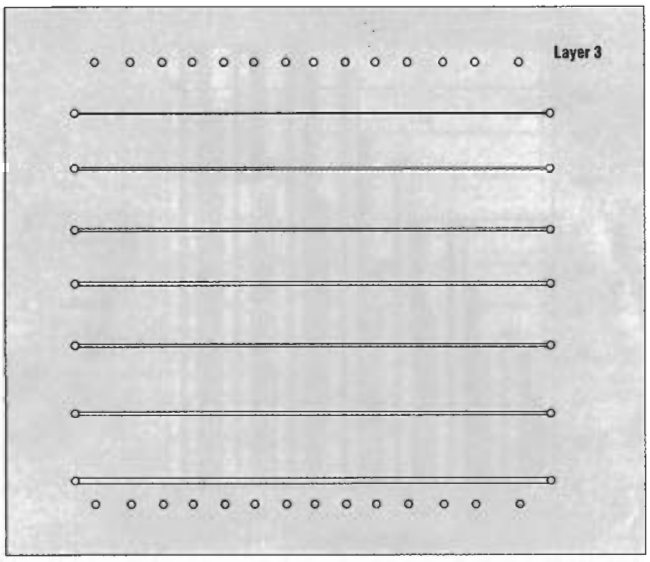

Figure 3. Trace layout, layer three. Varying trace widths.

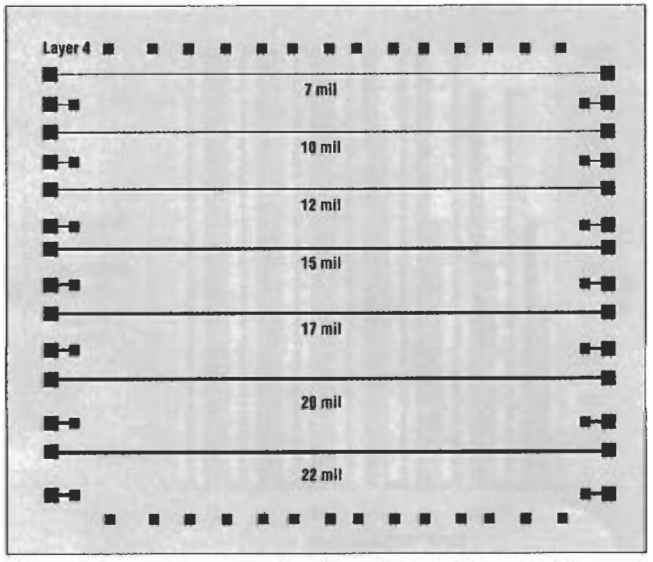

Figure 4. Trace layout, bottom layer. Varying trace widths.

that has been exposed to the hygroscopic dust spray detailed in GR-63-CORE.
- > 60 mil for a surface-layer trace with no solder mask and that has been exposed to solder flux.
- < 7 mil for an internal-layer trace.

To ensure no dielectric breakdown during the application of the 1000-V, 100-A, 10 × 1000-microsecond first-level surge, the minimum trace-to-trace spacings are as follows:

- < 7 mil for a surface-layer trace with solder mask.
- Minimum 7 mil for a surface-layer trace with no solder mask and that is clean (free of dust and solder flux).
- > 10 mil for a surface-layer trace with no solder mask and that has been exposed to the hygroscopic dust spray detailed in GR-63-CORE.
- > 20 mil for a surface-layer trace with no solder mask and that has been exposed to solder flux.
- < 7 mil for an internal-layer trace.

The experiment also revealed the minimum trace width required on external and internal layers of a PCB. To ensure a trace does not become an open circuit during the application of the 2500-V, 500-A, 2 × 10-microsecond first-level surge defined in GR-1089-CORE, the following trace widths are required, depending on the layer:

- Minimum 7 mil for a surface-layer trace with no solder mask.
- < 7 mil for a surface-layer trace with solder mask.
- Minimum 10 mil for an internal-layer trace.

To ensure a trace does not become an open circuit during the application of the 1000-V, 100-A, 10 × 1000-microsecond first-level surge, the following minimum trace widths are required on external and internal layers of a PCB:

- > 10 mil for a surface-layer trace with no solder mask.
- > 7 mil for a surface-layer trace with solder mask.
- Minimum 15 mil for an internal-layer trace.

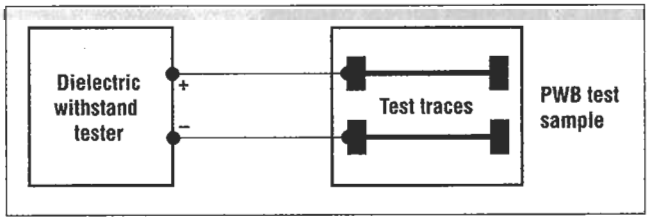

Figure 5. A calibrated withstand tester was used to apply a dc potential between the traces.

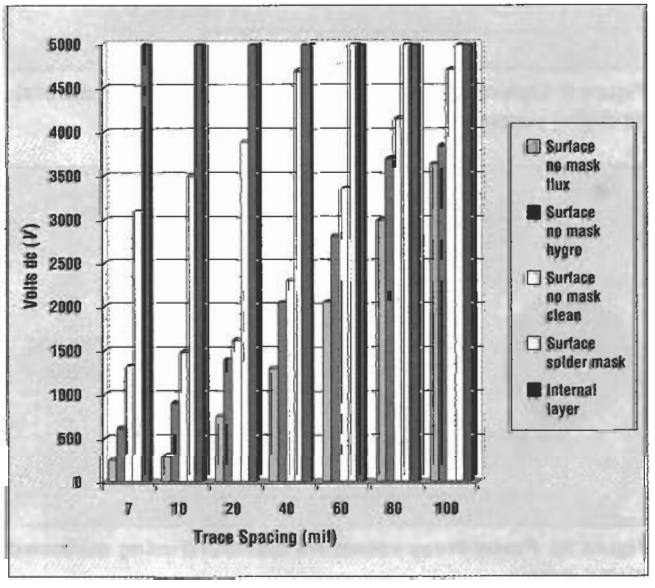

Figure 6. Trace dielectric properties, breakdown voltage.

A minimum trace width is required on external and internal layers of a PCB. This minimum trace width ensures the trace's fuse characteristics are greater than that of a Bussman Type MDQ 1-6/10A fuse when subjected to the 600-V, 60-A second-level power-cross transient detailed in GR-1089-CORE. The following minimum widths are required:

- Minimum 20 mil for a surface-layer trace with no solder mask.

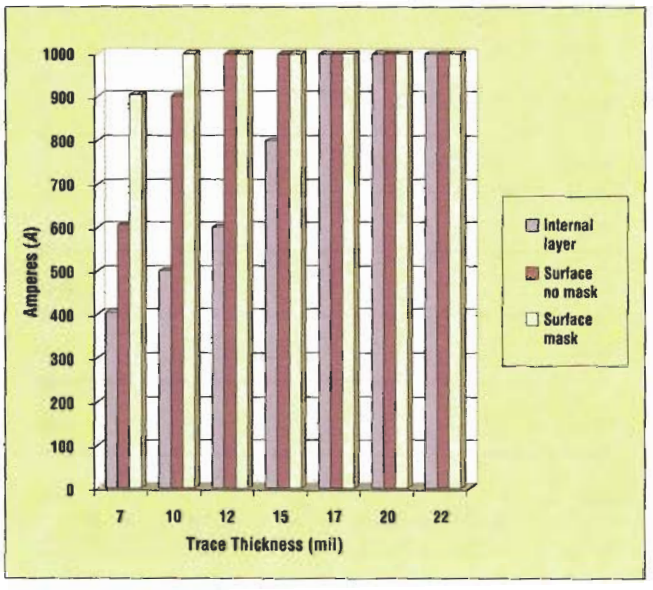

Figure 7. Trace current properties: 2 × 10 microseconds, 2500 V, 500 A, maximum current capacity.

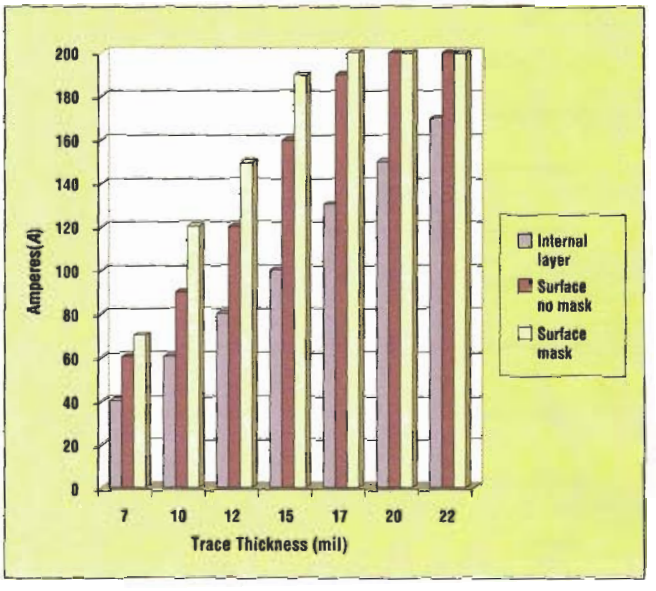

Figure 8. Trace current properties: 10 × 1000 microseconds, 1000 V, 100 A, maximum current capacity.

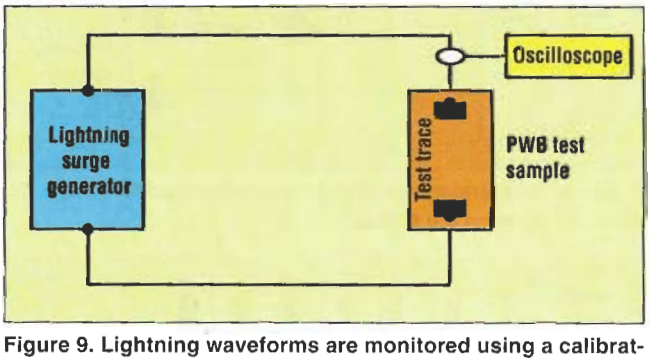

Figure 9. Lightning waveforms are monitored using a calibrated digital oscilloscope.

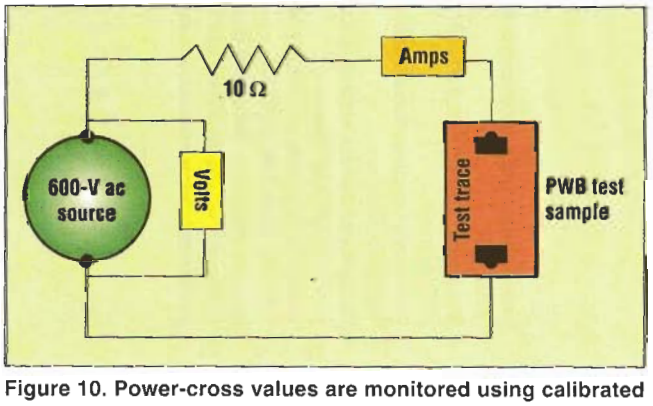

Figure 10. Power-cross values are monitored using calibrated digital meters.

- Minimum 15 mil for a surface-layer trace with solder mask.
- Minimum 22 mil for an internal-layer trace.

Several observations were made from the data. Surface-layer traces with no solder mask have a lower dielectric breakdown voltage than surface-layer traces with solder mask. Internal-layer traces have a higher dielectric breakdown voltage than surface-layer traces. Surface-layer impurities lower the dielectric breakdown voltage, and surface-layer traces with no solder mask have a lower current-carrying capacity than surface-layer traces with solder mask. Finally, internal-layer traces have a lower current-carrying capacity than surface layers.

Conclusion

The information presented in this article is not meant to be a rule book for designers to use when laying out circuits exposed to external transients. Rather, it should be used as one of many tools to successfully design a circuit that is immune to surge and power-cross transients.

Although this experiment concentrated on the impact that both high voltage and high current transients have on PCB traces, these data can be used to aid in component selection, component placement, and connector pin assignments. Surge suppression devices and overcurrent protection may help reduce the trace spacing and width constraints presented in this article. By coordinating these devices with the data provided in this article, arcing and blown traces should be avoided during formal testing and, hopefully, during field service as well.

Surge suppression devices may help reduce trace spacing and width constraints.

References

1. Bellcore GR-1089-CORE, Issue 2, Rev. 1, "Electromagnetic Compatibility and Electrical Safety—Generic Criteria for Network Telecommunications Equipment," Telcordia Technologies, Morristown, NJ, February 1999.
2. Bellcore GR-63-CORE, Issue 1, "NEBS Requirements: Physical Protection," Telcordia Technologies, Morristown, NJ, October 1995.

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