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A MODULATED SCR ZERO-POINT SWITCHING CIRCUIT

By employing SCR devices in a zero-point switching mode, the circuit designer can greatly reduce the problem of excessive RFI generation usually found in SCR phase control circuits. This note describes the zero-point switching concept, and provides a circuit design example (AC controller - DC half-wave controller) illustrating the salient considerations, and typical circuit performance.

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INTRODUCTION

Conventional SCR phase control circuits will generate varying magnitudes of RFI depending upon the circuit's mode of operation. Every time an SCR is switched on at some phase angle above 0° or less than 180°, the switching transient will produce RFI. These transients can be detrimental either directly or indirectly to circuits operating in the same area. In order to hold these transients to a minimum, two conditions should be met; first, the applied voltage should always be turned on as it passes through the zero point, and, secondly, the circuit should be switched off as the current passes through zero. In an SCR circuit controlling AC power, the latter of these two conditions is met automatically with the natural commutation of the SCR. Therefore, if the control circuitry is designed in a manner so as to always gate the SCR at the voltage zero crossover point, the energy delivered to the load will be free of RFI due to SCR switching.

DESIGN EXAMPLE: ZERO-POINT SWITCHING CIRCUIT

The circuit in figure one has been designed to overcome the problem of RF1 due to SCR switching transients. The circuit is a design example only, and not intended for any specific application. The circuit employs the SCR devices in a zero point switching capacity, hence, in this circuit the energy delivered to the load is controllable. The circuit configuration is that of an AC controller, but by eliminating the slave fired thyristor (SCR_2), the circuit can control DC half-wave power. The design dictates the firing of SCR_1 always at the beginning of the positive half cycle. The heart of the circuit is a line synchronized UJT (Motorola 2N4870) astable multivibrator with variable "on" and "off" periods. The multivibrator action is provided by Q_1, Q_2, and the timing networks of C_2 with (R_7 + R_8) and (R_9 + R_{10}). In order to illustrate this action, assume for the time being that the wiper of potentiometer R_6 is disconnected to allow the UJT to free run. When the circuit is actuated at t = 0 by the DC supply, the base of Q_2 will be forward biased to a point that will drive the transistor into saturation. Capacitor C_2 will begin to charge at a rate that is primarily determined by (R_7 + R_8). The emitter base, junction of Q_1 will be in a blocking mode. C_2 will continue to charge to a voltage equal to V_P for the UJT at which time triggering will occur. Upon triggering of the UJT, the voltage across C_2 will reverse bias the base of Q_2, turning it off. This condition will prevail for a time that is dependent on the discharge rate of C_2 as controlled by (R_9 + R_{10}). When C_2 has discharged to a point that will again forward bias the base of Q_2, the transistor will switch into conduction, drawing the emitter current of Q_1 below the minimum holding current, thereby turning it off. This brings the circuit back to the state it was in at t = 0, and the sequence of events will be repeated. By utilizing the collector-to-emitter voltage of Q_2, the circuit exhibits a controllable "on"-"off" output of the astable multivibrator type. This output can be used to modulate the gate drive of SCR_1 to control the energy output. In this circuit the multivibrator controls an emitter follower stage that supplies gate drive to an inexpensive commercial SCR device. The multivibrator is modified to control the switching action of the UJT to perform the zero point firing characteristic. This is accomplished by synchronizing the circuit so that the UJT will only trigger during the negative half cycle, thereby assuring the availability of gate power at the crossover of the positive half cycle. Synchronization to the negative cycle is done in the following manner: The emitter of Q_1 is clamped just below V_P by potentiometer R_6 for the V_{BB} voltage obtained from the 20 volts on the positive half cycle. Synchronization comes about by partially back-biasing the V_{BB} network R_4 and R_5 by the voltage dropped across R_3 during the negative cycle. The reduction in V_{BB} during the negative cycle is sufficient to allow the clamped V_E of the UJT to equal or exceed V_P for these conditions, and the device will trigger. With the components values given, the "on" period is from 1 to ≈ 50 cycles, and the "off" period is from 1 to 5 cycles.

When operating as an AC controller, SCR2 is slave fired by the load voltage of SCR_1. Whenever SCR_1 conducts, C_3 charges and maintains a sufficient charge long enough into the next half cycle to assure the firing of SCR_2, regardless of the loads phase shift. This technique gives a symmetrical output of complete cycles.

The given circuit configuration and component values of figure one allow operation of from 20% to 98% total energy. Figures 2 through 5 (oscilloscope traces from the output of circuit one) show just a few of the possible combinations obtainable. In figures two and three, one cycle on-one cycle off and five cycles on five cycles off, respectively, the circuit is delivering 50% of the total energy. In both figures two and three the on-time is equal to the off-time. The period of time between "energy outputs" for figure 3 is greater than figure two, however. Figure four, one cycle on-five cycles off, shows circuit operation delivering 20% of the total energy. The operational mode illustrated in figure 4 represents the maximum off-time (and minimum on-time) obtainable with this particular circuit. Figure 5 illustrates the five cycles on-one cycle off mode of operation. In this mode 80% total energy is available. Figure 7 shows the voltage and current waveforms of an inductive load. It can be seen that since the voltage was turned on at zero, the inductive load was not presented the usual step-function transient, and, consequently, no spike was created. This accounts for the non-existance of switching transients. Figure 6 shows that no noticeable crossover distortion is present. The additional gate drive from the final transistor allows the low-cost SCR to be turned-on with no crossover distortion.

In order to assure performance stability and maintain a wide latitude of control, the following criteria should be utilized if possible. The UJT should exhibit a high intrinsic stand-off ratio η (eta) and have a low I_p. This will improve the on and off time constants and make the circuit less sensitive to minor supply fluctuation. The emitter follower stage used to drive the control SCR can be eliminated by using a sensitive gate SCR. The gate signal can then be taken directly across transistor Q_2. By eliminating this stage, the zener supply is not loaded as heavily, and the ripple content will be reduced. By reducing the ripple, the tolerances for negative cycle actuation has a wider latitude. Also, the zener can be reduced in wattage giving a sizable cost saving along with the savings of eliminating the transistor stage.

OTHER CONSIDERATIONS

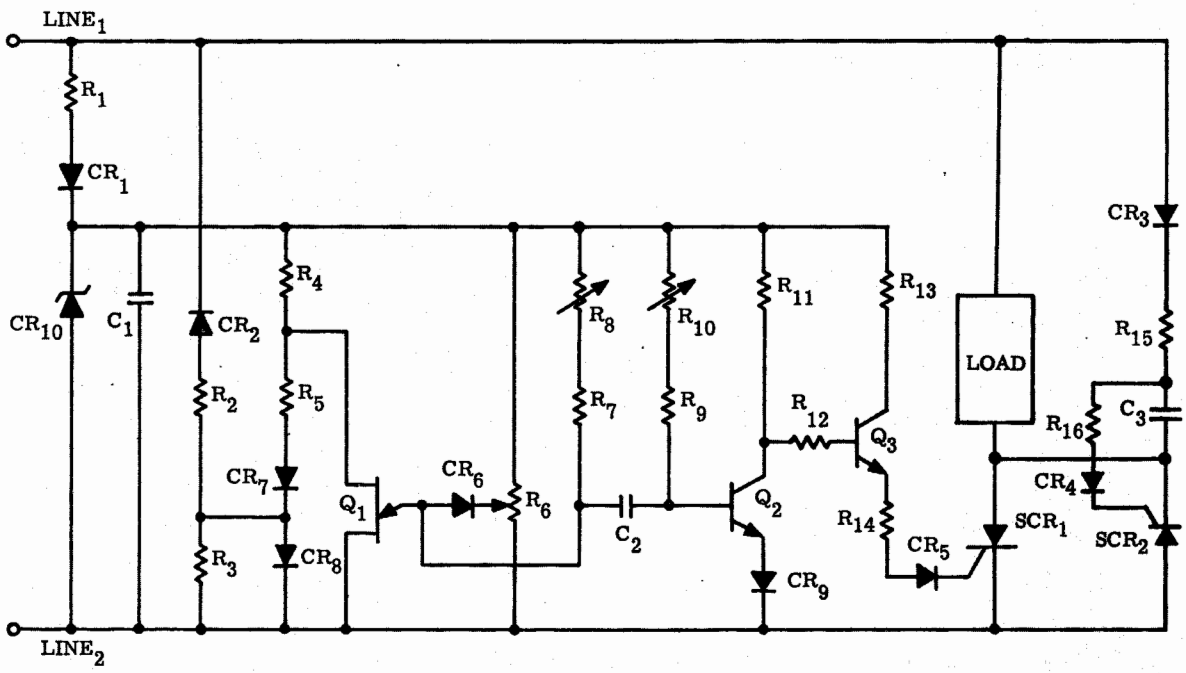
Aside from the switching transient RFI reduction, this circuit offers many other desirable features. The di/dt factor that constantly plagues the SCR circuit design engineer is minimized in this type of operation. In a con-

ventional phase control circuit, surge currents, created by turning on an SCR at a high voltage level can cause deterioration and eventually destruction in a device if not properly compensated for. With zero point switch, the rate of change in current is strictly dependent upon the load characteristic to a pure sine wave, and not a step function. Because the circuit is designed for an output with an integral number of complete cycles, it can be used to supply a transformer. A word of caution though; under open circuit conditions the energizing current of a transformer may not be sufficient to maintain a stable condition for the inverse parallel SCRs. If a transformer is used with this circuit, it is either necessary to have it loaded or use a dummy load across the primary. The proper load resistance will be within the limits given by the two following equations:

$$Z_{load\ (min)} = \frac{V_{AC}}{I_{load\ (min)}} \qquad Z_{load\ (max)} = \frac{V_{AC}}{I_{load\ (max)}}$$

For the given circuit, $I_{load\ (min)} = 1.0A$, and $I_{load\ (max)} = 8.0A$. The maximum current is limited by the current carrying capability of the SCR; the minimum current will have to be determined experimentally.

A MODULATED SCR ZERO POINT SWITCHING CIRCUIT



C_1 - 200 μF
C_2 - 5 μF
C_3 - 50 μF
CR_1, CR_2, CR_3 - 1N4004
CR_4, CR_5, CR_6, CR_7, CR_8, CR_9 - 1N4001
CR_{10} - 1N2984, 20v, 3.5w
R_1 - 1 k, 10 w
R_2 - 6.8 k
R_3 - 1 k
R_4 - 390 Ω
R_5 - 4.3 k
R_6 - 10 k
R_7 - 3 k
R_8 - 3 k POT
R_9 - 6.2 k
R_{10} - 500 k POT
R_{11} - 10 k
R_{12} - 33 k
R_{13} - 560 Ω
R_{14} - 33 Ω
R_{15} - 5.1 k
R_{16} - 47
SCR_1 - 2N4442
SCR_2 - 2N4442
Q_1 - 2N4870
Q_2, Q_3 - 2N3903

FIGURE 1 — A MODULATED SCR ZERO-POINT SWITCHING CIRCUIT

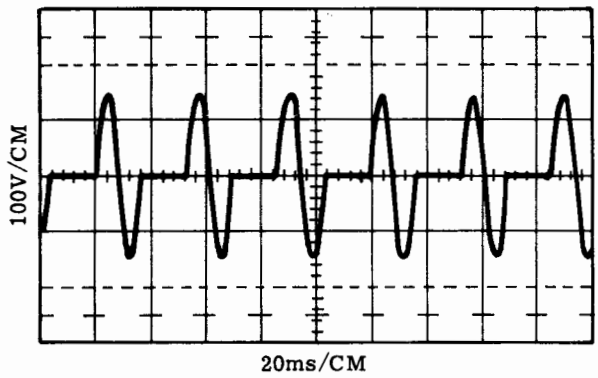


FIGURE 2 — ONE CYCLE ON — ONE CYCLE OFF

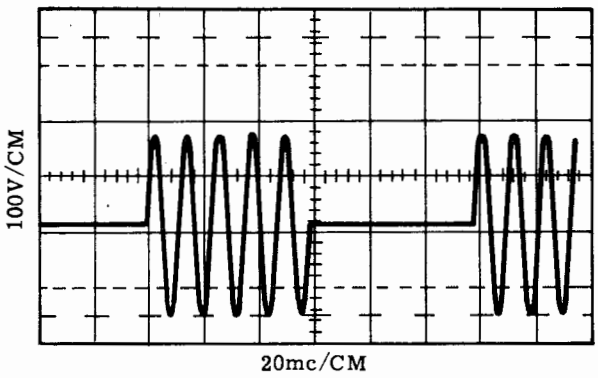


FIGURE 3 — FIVE CYCLES ON — FIVE CYCLES OFF

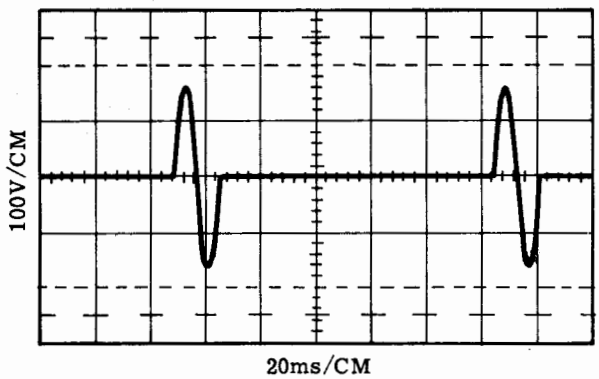


FIGURE 4 — ONE CYCLE ON — FIVE CYCLES OFF

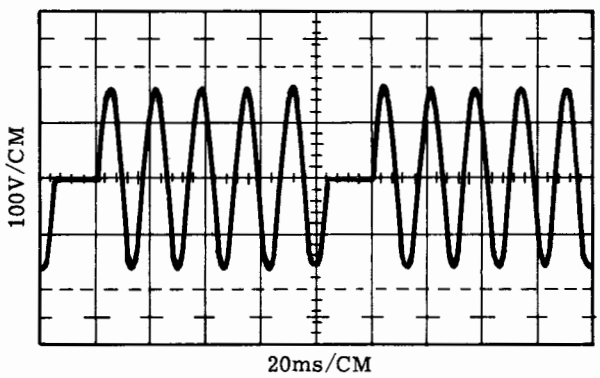


FIGURE 5 — FIVE CYCLES ON — ONE CYCLE OFF

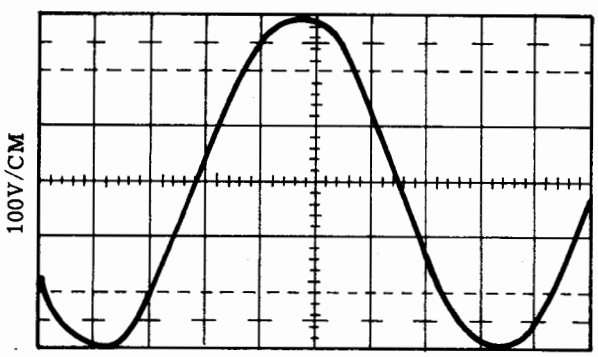


FIGURE 6 — INDUCTIVE LOAD

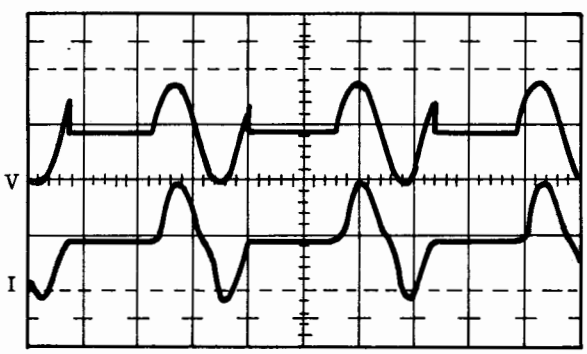


FIGURE 7 — CROSSOVER DISTORTION