

Interleaving dc/dc converters boost efficiency and voltage

THOUGH SOMEWHAT MORE COMPLEX THAN SINGLE-PHASE DESIGNS, INTERLEAVED-BOOST CONVERTERS RUN COOLER, OCCUPY LESS SPACE, AND CAN COST LESS.

Boost power supplies are popular for creating higher dc voltages from low-voltage inputs. As the power demands from these supplies increase, however, a single power stage may be insufficient. This article presents an interleaved-boost approach, which, compared with a single-boost converter, both analytically and empirically provides efficiency, size, and cost advantages. The article also compares test results of 250W, single-phase and interleaved-boost power supplies. The interleaved-boost topology provides superior performance, albeit with increased complexity.

The motivation for the work this article describes was the selection of a power-supply topology for an ink-jet printer's solenoid driver. The input voltage was 12V dc; the required output was 37V dc at 7A. The supply's input current could exceed 20A. It was initially unclear whether a single power stage or a multi-phase stage was most appropriate. As in buck regulators, currents could be high enough to make duplicate power stages desirable; they spread the dissipated heat around the pc board and reduce the stress on many of the circuit components. The work discussed included evaluation of single- and two-phase-boost topologies.

Table 1 presents the power-supply requirements. To maintain the desired output voltage within a small margin, this supply is subject to substantial current surges as the solenoid energizes and de-energizes. In addition, high efficiency is important for maintaining an acceptable temperature rise. The 37V, 7A output delivers more than 250W to the load. Even with an efficiency of 91%, the power supply dissipates 25W, requiring multiple heat sinks. Moreover, the supply's size and cost were important, although no specific requirements were provided.

Figure 1 compares two power supplies. The top supply is the single-phase design with a single input inductor. The circuit below it is the two-phase design. The single-phase design requires approximately 18 in.² of pc-board area, whereas the interleaved design requires 14 in.² The largest differences in area between the two approaches are in the inductors, output capacitors, and heat sinks. The maximum height of the interleaved inductors is also less than that of those in the single-phase design.

Figure 2 shows the schematics of the single-phase- and interleaved-boost converters. In the single-phase design, applying a

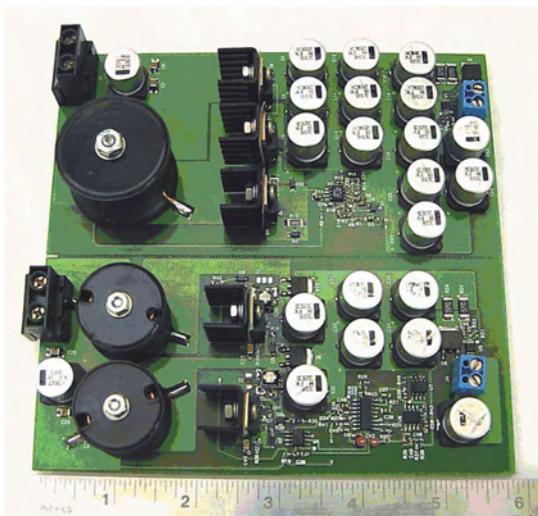


Figure 1 A converter with a single-phase topology (top) is larger than a converter with a two-phase topology (bottom) that produces the same output voltage and current.

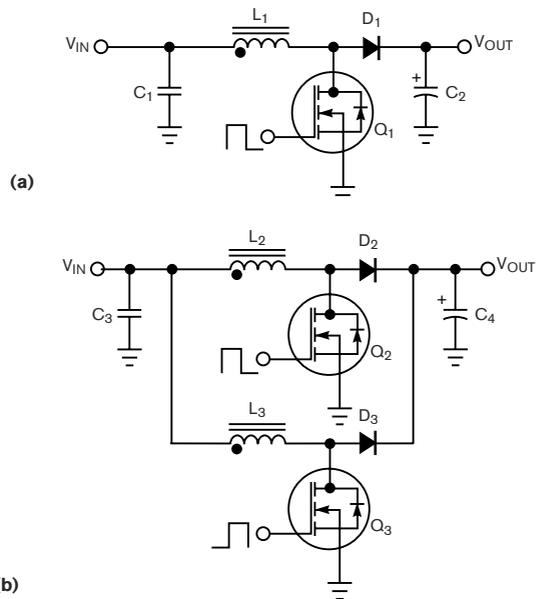


Figure 2 The single-phase supply (a) is simpler than the interleaved-boost supply (b).

gate voltage to FET Q_1 pulls the drain potential to ground, applying the input voltage across inductor L_1 and causing current to ramp up. During the ramp time, output capacitor C_2 must alone supply the load current. When Q_1 turns off, the voltage across L_1 reverses polarity to maintain current flow. This scenario forces the switch node more positive than the input voltage and forward-biases diode D_1 , charging output capacitor C_2 and supplying the output current. For each of the two switching states, the inductor's volt-microsecond product must balance. That is, $d/f_s \times V_{IN} = (1-d)/f_s \times (V_{OUT} - V_{IN})$, yielding the relation $V_{OUT} = V_{IN}/(1-d)$, where d is the duty ratio, f_s is the switching frequency, V_{IN} is the input voltage, and V_{OUT} is the output voltage. This expression is valid in CCM (continuous-conduction mode), in which the inductor current remains positive at all times.

Each phase of the interleaved-boost converter (Figure 2) works in the same way that this single-phase-boost converter does. The two power stages operate 180° out of phase, canceling the ripple current in the input and the output capacitors. The interleaved-boost approach uses forced current-sharing between the power stages to equalize the power that the stages deliver. Without this feature, one power stage could deliver substantially more power than the other, which would defeat the ripple cancellation.

DESIGN ANALYSIS

Figure 3 shows how interleaving benefits input-capacitor ripple-current cancellation. The two power stages operating 180° out of phase provide a two-to-one reduction in peak-to-peak ripple current. Because the interleaved-boost converter's combined input-ripple current equals that of the single-phase converter, the two-phase design's individual-phase ripple currents can each be twice as large as that of the single-phase design. The individual interleaved power stages operate at the same frequency as the single-phase design, 100 kHz, but the effective input- and output-ripple frequency is 200 kHz. The interleaved-design calculation used a frequency of 100 kHz and twice the ripple current of the single-phase design, yielding half the inductance. Because the two-phase design's effective input-capacitor ripple current was the same as that of the single-phase design, the two designs used an equal number of input capacitors. Ripple cancellation allows a choice of which components to reduce in number. Using two inductors, each having the same value as that in the single-phase design, halves the input-capacitance requirements. In a boost design, however, the inductor requirements are generally more critical than those of the input capacitors.

Interleaving benefits the output capacitors in about the same way as it affects the input capacitors. Figure 4 shows the sin-

TABLE 2 SINGLE-PHASE VERSUS INTERLEAVED INDUCTOR

	Single phase	Interleaved
No. of inductors	One	Two
Inductance specification (mH)	27	10
Inductor-current specification (A)	21	10.5
Total LI^2 specification (mH \times A 2)	11,907	2205
Height (in.)	1.6	1.1
Total actual volume (in. 3)	2	1.8
LI^2 /volume (actual)	6075	1225
Actual resistance (V)	0.008	0.006
Total loss (W)	5.8	1.2

TABLE 1 ELECTRICAL SPECIFICATIONS OF AN INK-JET-PRINTER POWER SUPPLY

Parameter	Specification
Input voltage	10.8 to 13.2V
Output voltage	37V
Output current	7A maximum
Load step	1 to 7A
Efficiency	91% minimum

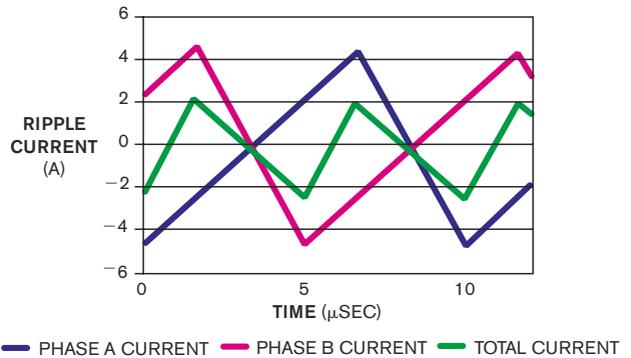


Figure 3 Because the two-phase converter's input-ripple currents are in phase opposition, the total input-ripple current is smaller than that of either phase.

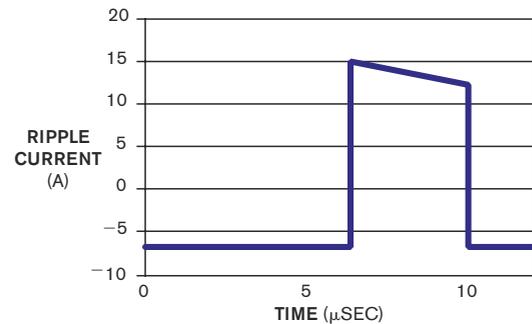


Figure 4 In the single-phase converter, the output-filter capacitor supplies all of the output current during the FET's on-time. During the off-time, however, a current of $I_{OUT} \times d/(1-d)$, or 14A, flows into the capacitor to recharge it.

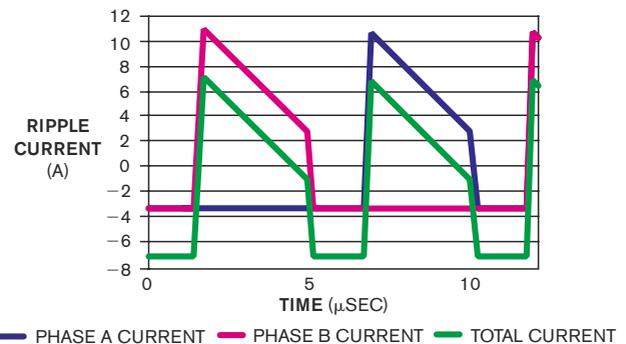


Figure 5 Interleaving reduces the two-phase converter's output-capacitor ripple current.

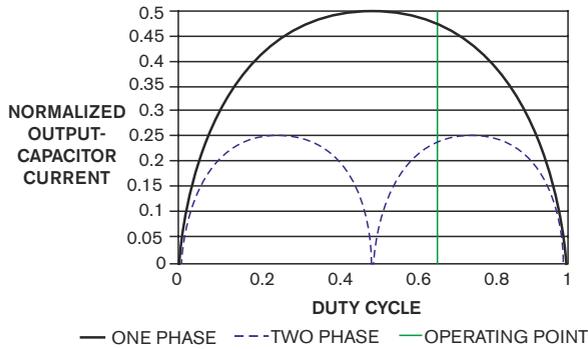


Figure 6 This interleaved-boost converter's output-capacitor ripple current is only half as great as that of a single-phase converter.

gle-phase output-capacitor ripple current. In this design, this waveform's rms current is approximately $I_{pp} \times (d \times (1-d))$, or 10A rms. The inductor slope, which appears at the top of the waveform, does not significantly add to the total rms current. This capacitor supplies all of the output current during the FET's on-time. During the off-time, however, a current of $I_{OUT} \times d / (1-d)$, or 14A, flows into the capacitor to recharge it. In designs that use aluminum-electrolytic output capacitors, capacitor ripple-current ratings determine the required number of capacitors.

Figure 5 shows the interleaved-boost converter's individual and combined output-capacitor currents. Not counting the inductor slope, the phase A and B currents' peak-to-peak amplitudes are half those of the single-phase design because the duty

TABLE 3 INTERLEAVED VERSUS SINGLE-PHASE DESIGN

	Interleaved design	Single-phase design
Circuit area (in. ²)	14	18
Height (in.)	1.2	1.6
Full-load efficiency (%)	93.8	91.6
Full-load loss (W)	16	23
No. of power components	15	19
No. of heat sinks	Two	Three
No. of control components	53	30

cycle of the current flowing into the output capacitors is twice that of the single-phase design. In **Figure 5**, the rms value of the combined or total waveform is 5A, allowing half the number of output capacitors to maintain a ripple voltage no greater than that of the single-phase design.

Figure 6 shows the ripple-current cancellation that you can obtain at various duty cycles. The vertical line indicates the operational duty cycle and shows the interleaved-boost circuit's two-to-one rms-current reduction compared with that of the single-phase circuit. A 50% duty cycle can provide perfect cancellation.

Figures 7 and **8** show the completed single-phase- and interleaved-boost-converter designs. In the single-phase design, a UCC38C43 PWM (pulse-width-modulation) controller operating in voltage mode drives a pair of MOSFETs. Because the boost converter offers no way to limit the output current in the event of a short circuit, a TPS2490 hot-swap circuit with over-current protection was added during testing to halt current flow during overcurrent faults. **Figure 8** illustrates the interleaved design using a UCC38220 dual-interleaved PWM controller.

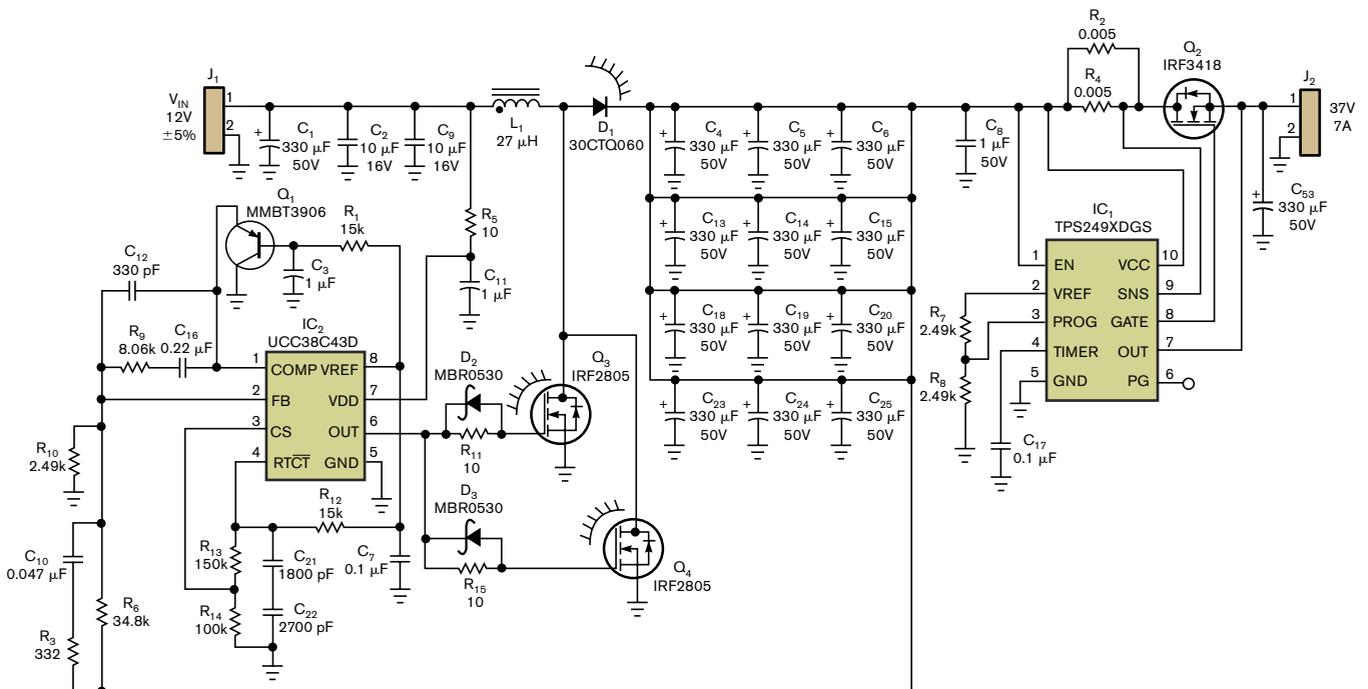


Figure 7 This single-phase-boost converter uses only two ICs, one FET, and one inductor, but it includes 13 large aluminum-electrolytic capacitors.

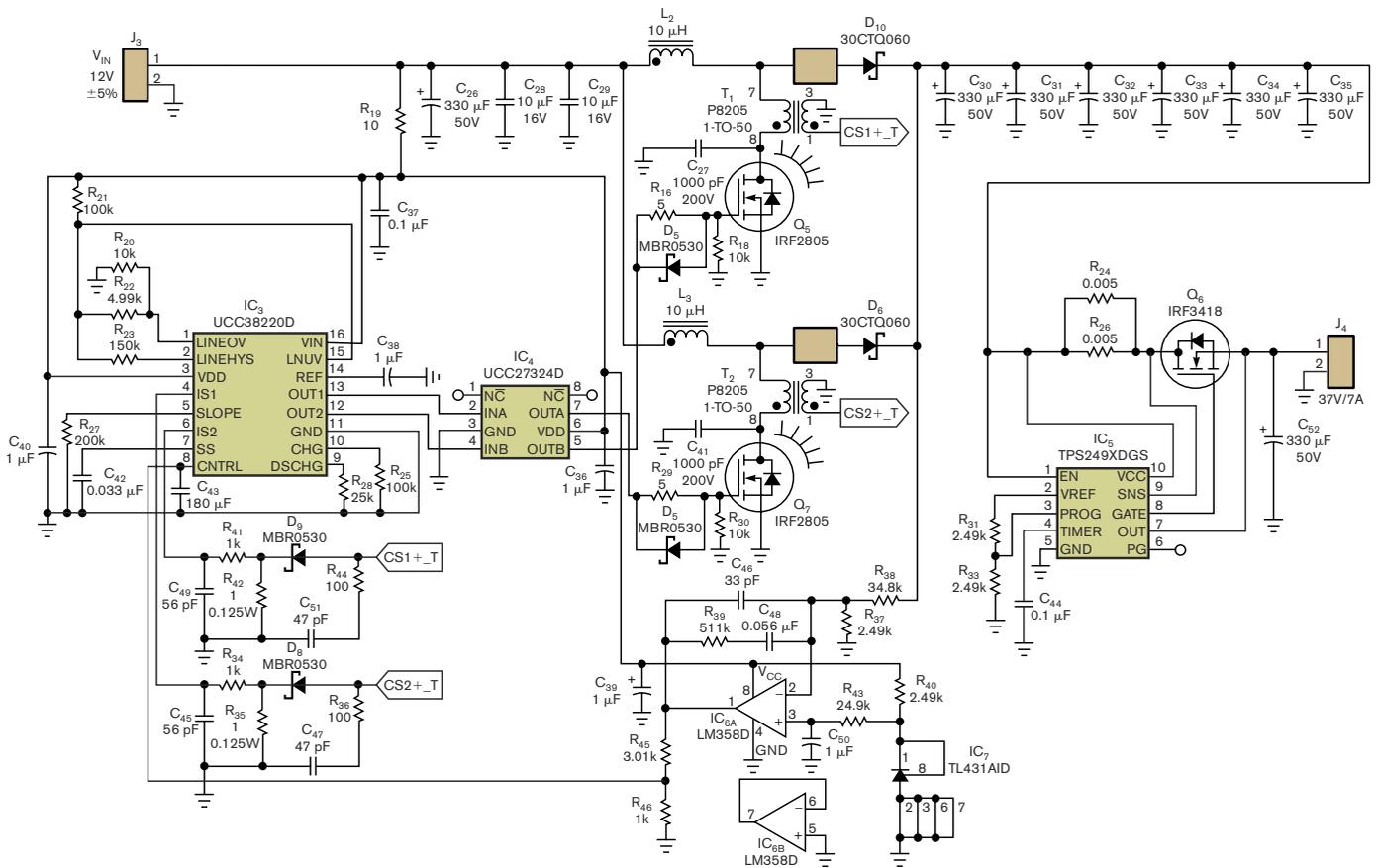


Figure 8 This interleaved design halves the output-capacitor requirements.

Low-cost transformers in the drain leads of Q_5 and Q_7 sense the FET current. The controller forces equal current in the two phases. Reduced current in the rectifiers eliminates the need for heat sinks and lowers assembly costs.

EXPERIMENTAL RESULTS

The above scenario compared the two designs for efficiency, input- and output-ripple voltage, and transient loading. In most situations, the two-phase approach exhibited better performance than did the single-phase approach. **Figure 9** compares the efficiency of the two approaches. Both meet the target 91% efficiency; however, at full load, the two-phase approach's efficiency is more than 2% better. Although this improvement may sound insubstantial, the difference in losses between the two supplies is significant. The single-phase design dissipates 23W, whereas the two-phase approach dissipates only 16W, significantly affecting the choice of heat sink and the thermal design.

The single-phase curve's early maximum and rapid decline indicate that the design has significant conduction losses. The big differences between the two designs are the losses in the inductor, boost diode, output capacitors, and pc board. **Table 2** compares the inductor requirements and designs' performance. The two-phase approach uses significantly less inductance than does the single-phase approach, and each inductor carries half the current. Energy-storage requirements and temperature rise

determine an inductor's volume. The formula $\frac{1}{2} \times L \times I^2$ determines energy storage. **Table 2** shows that the energy storage of the single-phase design is five times that of the two-phase approach. Therefore, if the temperature rise of the inductors had been equal, the single-phase inductor would have been five times as large.

Rather than keeping the energy density equal, the designers chose to allow a higher temperature rise in the single-phase design, sacrificing some efficiency by using an inductor with higher losses; consequently, losses in the single-phase design are about 5W higher. Output capacitors accounted for about 1W of the power-loss difference. Ripple current in each of the output capacitors produced about 100 mW of dissipation, and the single-phase approach needed approximately six more capacitors than did the two-phase design. The two-phase approach required the use of two diodes in the power stage, with each carrying half of the total current. Consequently, the diodes exhibited a lower voltage drop, resulting in approximately 1W less loss.

Figure 10 shows the input- and output-voltage-ripple measurements. **Figure 10a** is the single-phase converter, and **Figure 10b** is the interleaved converter. The upper traces, which show the output-ripple voltage, illustrate several key points. The inductor current flowing through the output capacitor's ESR (equivalent series resistance) mainly determines ripple voltage. The traces in **Figure 10b** show the higher frequency ripple that

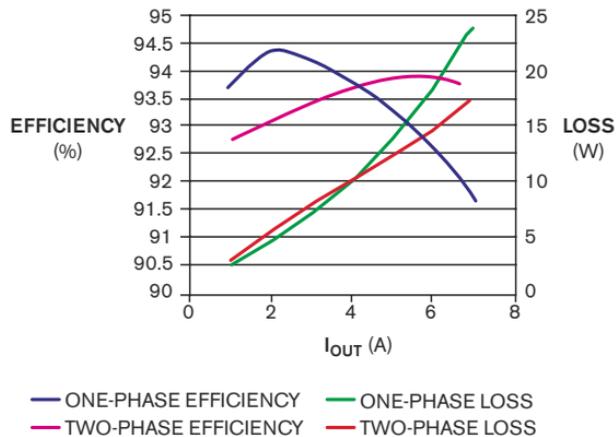


Figure 9 The two-phase converter is more efficient than the single-phase unit at output currents greater than 4A.

the interleaved approach achieves. In **Figure 10a**, the top of the ripple is nearly flat because of the large value of the boost inductor. In **Figure 10b**, the slope is significant because of the large change in inductor current during the power-switch off-time. The lower traces also show the input-ripple voltage's higher frequency with the two-phase approach.

Just as with buck regulators, interleaved-boost regulators can

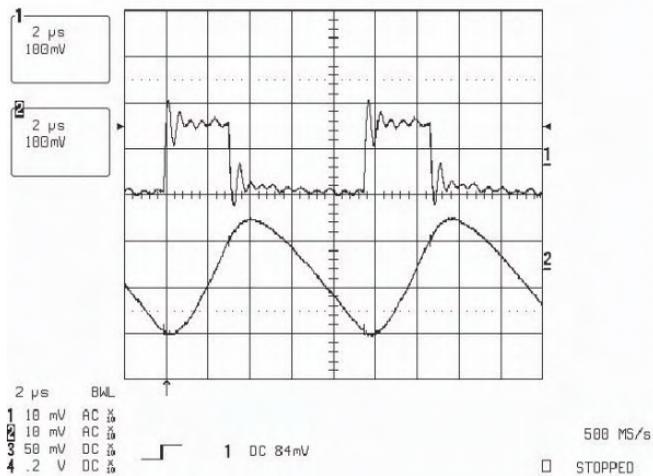
provide performance benefits over single-phase designs. **Table 3** compares the completed single-phase-boost design with the interleaved-boost approach. The interleaved-boost circuit is smaller, shorter, and more efficient. The fact that it has fewer output capacitors is largely due to lower output-ripple current, which results in lower cost and lower power dissipation. This circuit also significantly reduces the energy-storage requirement of the combined input inductors, thus reducing the magnetic volumes, heights, and dissipations. The multi-phase approach reduced the overall power dissipation by 30% and spread that dissipation over a larger board area, allowing better thermal management. The main drawback of the multi-phase approach is added circuit complexity, requiring measurement and balancing of each phase current as the larger number of control components illustrates.**EDN**

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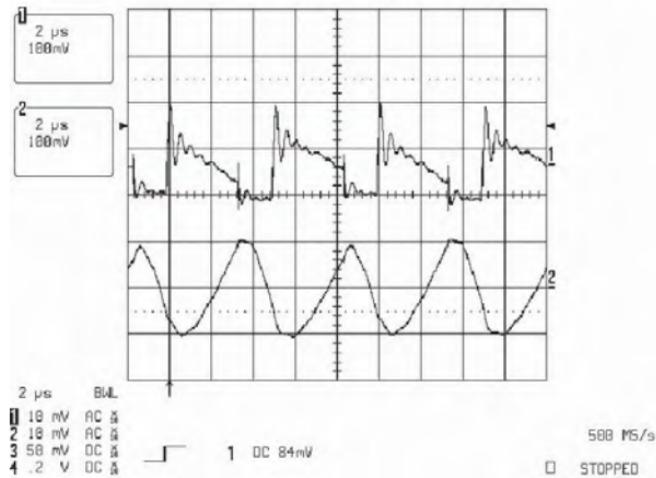
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(a)



(b)

Figure 10 The output-ripple voltage (upper traces in (a) and (b)) illustrates several points. For example, the higher frequency of the interleaved converter's ripple current eases filtering.

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