Is System-Level ESD Testing Valid for ICs?

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A study to evaluate the applicability of IEC-61000-4-2 testing at the semiconductor device level finds that results depend more on variations in test setup than in ESD sensitivity.

Electronic system designs often include transient protection to ensure system robustness for electrostatic discharge (ESD) events. Adding external ESD protection without compromising system I/O speed, sensitivity and signal integrity can be difficult since each device added to the signal line can introduce extra parasitic elements that may affect signal transmission. Additional devices on the circuit board also can increase cost and real estate. Because of this, manufacturers of electronic systems are now relying more on the IC manufacturers for protection against ESD events to reduce the need for stand-alone ESD protection devices within their systems.

To confirm that the ICs tied directly to the outside world are in fact ESD tolerant, many system manufacturers now require their component suppliers to perform system-level tests on semiconductor devices such as ICs and modules.

However, there are a few reasons why these system-level ESD tests are inappropriate for device-level testing. First, system-level tests are typically performed at the points where a piece of equipment interfaces to the outside world, typically at a connector or other port. But many ICs and modules are not tied directly to any I/O interface.

A second problem is that the test procedures are not defined at the component level. Semiconductor device manufacturers are forced to devise test procedures based on their own interpretation of a system-level test standard. Consequently, ESD test results vary from one chip vendor to another, even if they are testing the same components.

Perhaps the most troubling aspect of applying system-level ESD tests at the device level, a third problem, is the question of whether the system-level tests being performed on ICs and modules have any correlation to real-world applications.

Although much has been written with regard to the inappropriate nature of this test, very little data has been presented. Such data is needed to resolve this ongoing issue. So, to address these concerns, a one-year comprehensive study was conducted on the applicability of the popular system-level test (IEC-61000-4-2) when applied at the device level. Although the study included primarily power ICs, which were used as the devices under test, the functionality of these devices is secondary, and the results of the study should apply broadly to other types of semiconductor devices.

To conduct this study, a set of well-defined test procedures was established that could form the basis for a standard IEC-61000-4-2 device-level test. Though these test procedures are described in brief here, a complete

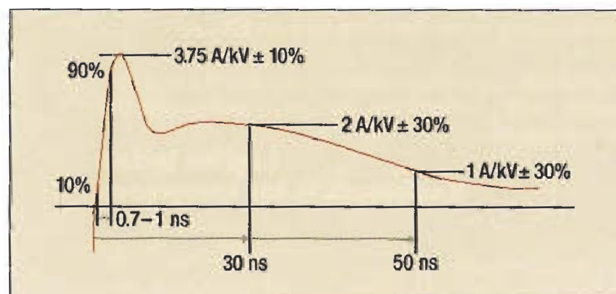

Fig. 1. *This required IEC-61000-4-2 test waveform is generated by the ESD simulator gun during contact-level testing.*

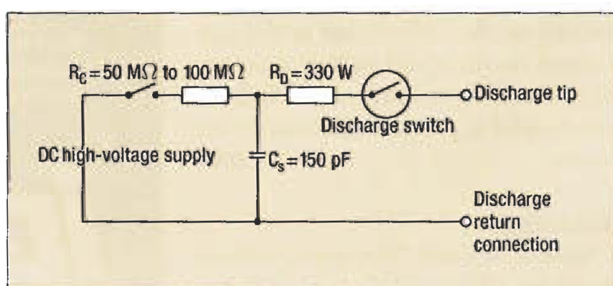

Fig. 2. *This circuit is defined in the IEC 61000-4-2 specification.*

description of how to build the test setup used in the study is beyond the scope of this article. Instead, this article presents the results of the study and their implications for device and system designers.

IEC-61000-4-2 Testing

The IEC-61000-4-2 standard was designed to test the ESD vulnerability of completed systems. However, a recent trend among system manufacturers has them requiring that their suppliers apply this test standard to individual components and/or pc boards. But in trying to fulfill this requirement, manufacturers of ICs (and discretes) are immediately confronted with a problem: The completed system (as well as the pc board on which the IC will eventually be located) is typically not designed, qualified and available at the point in time when the ICs are being qualified.

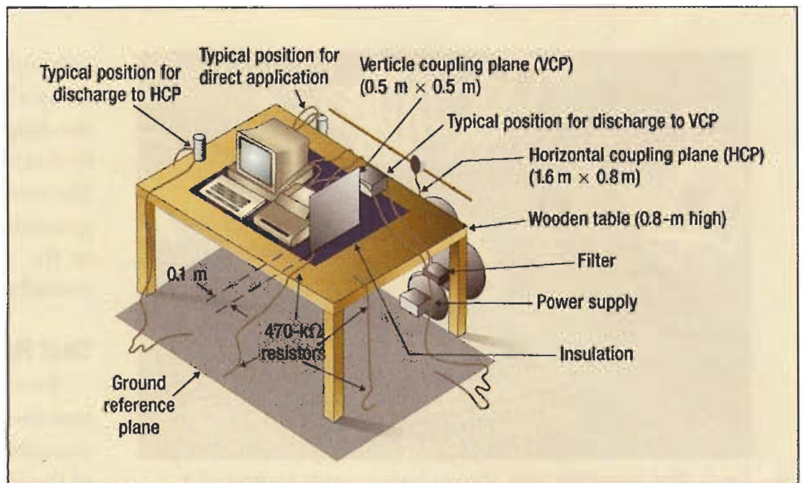

Fig. 3. *The IEC 61000-4-2 system test setup includes a tabletop setup (shown here) as well as a floor standing setup (not shown).*

Typically, those processes run in parallel rather than consecutively. So in lieu of testing ICs in the target system, alternate test vehicles are necessary. To comply with the request for IEC-61000-4-2 testing, IC manufacturers must develop their own interpretation of the test standard, possibly resulting in inaccurate reporting of component ESD sensitivity as well as a possible false sense of ESD robustness at the system level.

Misapplying test standards can lead to extra cost being built into a product with little or no benefit to the customer. In addition, misunderstandings between IC vendors and manufacturers can arise, because the system-level test standards give no guidance as to how the test should be conducted for IC chips or modules.

In the absence of a well-thought-out written test procedure, the person running the test must essentially invent a procedure that would normally be part of the standard governing the test and would take years to develop. Unless the test procedure is carefully documented and adequately represents the end application, the results of the test are of little value because they are strongly affected by the test method used.[1]

To further understand this issue and develop a standardized test methodology (if needed), a comprehensive one-year study was undertaken that included an in-depth analysis of variations of the current IEC-61000-4-2 test methodology and how they can affect the outcome of the test. Those variations included the size of the pc board used during testing, trace length and width, pc-board layers, types of connectors, layout and other design-related factors such as the inclusion and location of ESD protection devices such as transient voltage suppressor (TVS) devices.

Tests were performed with the device in both unpowered and powered states. Other variations included how the pc board, device and test gun were grounded during testing. Also taken into consideration was the ESD gun used to create the IEC-61000-4-2 compliant waveform, location on the pc board where the discharges were applied during testing, placement of the cables and contact versus air discharge test results. One additional question addressed in this study is whether any correlation exists between device-level ESD tests and those results found when IEC testing is applied to individual devices or pc boards.

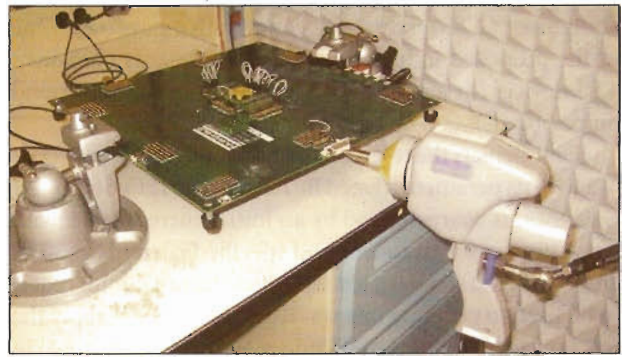

Fig. 4. *This IEC 61000-4-2 proposed test board was used during testing.*

IEC Proposed Test Boards

Two IEC proposed test boards were designed and applied during this study. Testing also was conducted using an application board and stop-sign-style automatic test

Level	Indicated voltage (kV)	First peak current of discharge, ±10 (A)	Rise time (t_R) with discharge switch (ns)	Current (±30%) at 30 ns (A)	Current (±30%) at 60 ns (A)
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

Table 1. *Parameters for the IEC-61000-4-2 test waveform depicted in Fig. 1.*

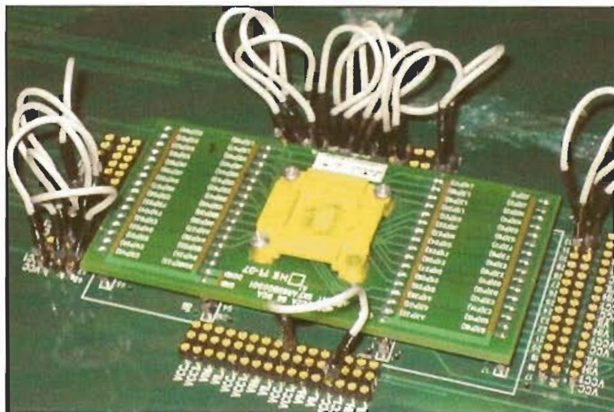

Fig. 5. *The daughter card shown here permits testing of a variety of package types up to 64 pins. Jumpers allowed for testing of specific pins tied to a connector.*

equipment (ATE) fixture for comparative purposes. One of the proposed industry-standard test boards contained TVS devices (to replicate TVS protection commonly found on pc boards), and one did not.

Fig. 1 depicts the test waveform specified by IEC-61000-4-2 with its parameters listed in Table 1. The IEC-61000-4-2 waveform is characterized by an initial current spike with a rise time of 0.7 ns to 1 ns and specified currents at 30 ns and 60 ns. The standard also specifies the test circuit that is to be used to generate this waveform (Fig. 2). To apply the test waveform to the devices under test, the setup shown in Fig. 3 was constructed. These figures are abstracted from the IEC-61000-4-2 specification, which was originally issued in 1995 and reissued in 1998 and 2000.

The proposed industry-standard test board used in the study was approximately 12 inches square and contained eight different types of connectors to replicate real-world applications (Fig. 4). It also used a daughter card and socket setup (Fig. 5) to accept any package type up to 64 pins, although larger pin counts could easily be included. This setup allows for easy testing, although the tradeoff of using the daughter card and test socket in lieu of soldering or press fit directly onto the pc board includes additional parasitics. The board itself contained four layers and included isolated ground and power. Figs. 6 and 7 show how the contact test to the connector and an IC pin connected directly to a connector on a pc board is performed.

Test Results

Results found during this comprehensive study indicate that the pc-board design and layout were one of the major contributing factors — not necessarily the ESD sensitivity of the individual component under test — in determining the test results when IEC-61000-4-2 testing is performed at the device level.

Other conclusions based on the application of the current IEC-61000-4-2 test standard to ICs were:

- The human body model (HBM) does not correlate to IEC 61000-4-2 when applied to devices.
- The charged device model (CDM) does not correlate to IEC 61000-4-2 when applied to devices.
- IEC 61000-4-2 when applied to ICs is not a good predictor of future ESD or electrical overstress (EOS) field fails.
- IEC 61000-4-2 test results can be more dependent on pc-board design and layout rather than an IC's designed-in ESD protection.
- Since IEC 61000-4-2 is a system-level test (and not a device level), test results when applied to an IC will vary widely depending on the test protocols followed, including placement of the probe and cables during testing.
- IEC 61000-4-2 should not apply to devices unless detailed IC test protocols are added to the specification.
- Device-level HBM and CDM are the best predictors of future device reliability.

It also was noted that absolutely no correlation was found to exist between the valid device-level ESD test results (CDM as well as HBM) and IEC-61000-4-2 testing when applied to the device. The data shown in Table 2 supports these findings.

Furthermore, statistically significant variations in test results also were found between the various waveform-compliant testers, even when applying the identical test methodology, circuit board and devices. Some testers found to be in compliance with IEC-61000-4-2 had considerable ringing and

Device	HBM (kV)	CDM (kV)	IEC at edge (kV)		IEC at connector (kV)		IEC at pin (kV)		IEC at topside (kV)	
			Contact	Air	Contact	Air	Contact	Air	Contact	Air
A	0.4	> 2	8	15	30	30	2.5	2.5	30	30
B	0.5	> 2	15	30	30	30	25	25	30	30
C	6	> 2	25	8	10	15	2.5	12	20	8
D	1.5	1.5	20	25	8	8	1	8	8	8
E	5	2.5	8	8	< 4	< 4	< 2.5	5	8	8
F	7	> 2	15	15	2	2	5	5	20	8
G	3	> 2	8	20	30	20	20	15	15	15
H	3	> 2	8	15	2	2.5	1	2.5	2	8
I	7.5	> 2	15	8	8	15	5	10	15	15
J	12	> 2	30	30	15	20	5	15	20	20
K	8	> 2	30	30	30	30	30	30	30	30
L	7.5	> 2	12	—	25	—	10	—	30	—
M	8	1.5	15	—	15	—	8	—	20	—

Table 2. *Correlation between HBM, CDM and IEC.*

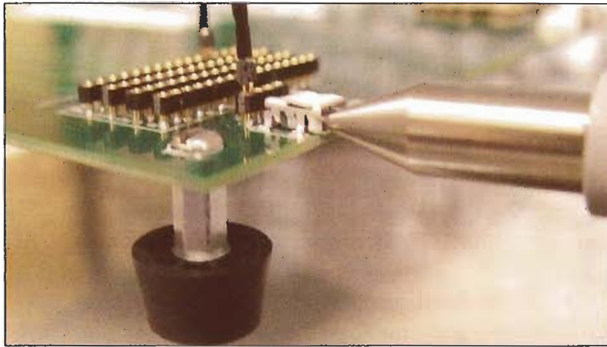

Fig. 6. *The contact discharge is being applied directly to a pin via a mini USB connector.*

high-frequency components that were not detected with 1-GHz instrumentation. These simulators may cause failures in products that would not have otherwise occurred if a different compliant tester had been used.

As stated earlier, in order for the IEC-61000-4-2 test to be of any comparative value when applied to device-level testing, a standardized test method needs to be defined and applied. That standard must include the specific layout and design of the pc board used during testing as well as the test protocols. The test method developed for the study described here could serve as the basis for a potential standard for IEC-61000-4-2 testing at the device level.

However, in lieu of having yet another device-level

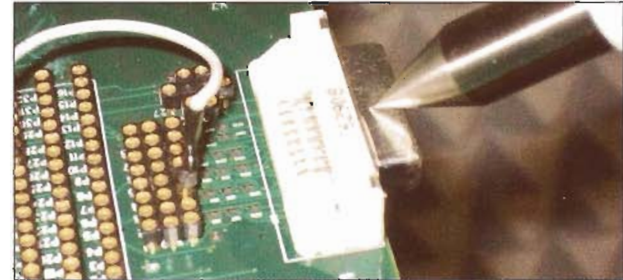

Fig. 7. *The contact discharge is being applied to the HDMI connector on the proposed IEC test board.*

ESD test, a better approach for the industry may be to make better use of existing tests. Data collected from more than 1 million products in the field indicates that the best long-term system reliability was linked directly to the device-level HBM and CDM test results coupled with an appropriate system design rather than using the system-level IEC test standard and applying it to a device. Once the system has been designed and assembled, the IEC 61000-4-2 test standard can then be applied as it was intended. **PETech**

Reference

1. Smith, Doug. "Misapplication of Test Standards," Technical Tidbit, June 2004, www.emcesd.com/tt2004/tt060104.htm.