

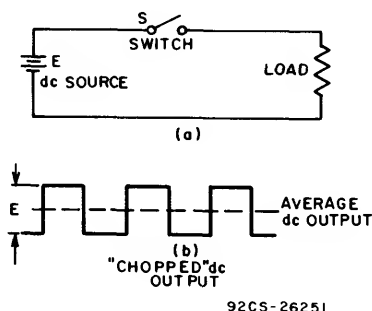
Power Conversion

In many applications, the optimum value of voltage is not available from the primary power source. In such instances, dc-to-dc converters or dc-to-ac inverters may be used, with or without regulation, to provide the optimum voltage for a given circuit design.

An **inverter** is a power-conversion device used to transform dc power to ac power. If the ac output is rectified and filtered to provide dc again, the over-all circuit is referred to as a **converter**. The purpose of the converter is then to change the magnitude of the available dc voltage.

BASIC CIRCUIT ELEMENTS

Power-conversion circuits, both inverters and converters, consist basically of some type of "chopper". Fig. 137(a) shows a simple chopper circuit. In this circuit, a switch S is connected between the load and a dc voltage source E . If the switch is alternately closed and opened, the output voltage across the load will be as shown in Fig. 137(b). If the on-off intervals are equal, the average voltage across the load is equal to $E/2$. The average voltage across the load can be varied by varying the ratio of the on-to-off time of the switch, by periodically varying the repetition rate, or by a combination of these factors. If a filter is



92CS-26251

Fig. 137 - Simple chopper circuit and output-voltage waveform.

added between the switch and the load, the fluctuations in the output can be suppressed, and the circuit becomes a true dc-to-dc stepdown transformer (or converter).

In practice, the switch shown in Fig. 137 may be replaced by a power transistor, in which case the switch is opened or closed by application of the appropriate polarity signal to the transistor base. The chopping or switching function in the inverter circuit is usually performed by high-speed transistors connected in series with the primary winding of the output transformer.

The design of the transformer is an important consideration because this component determines the size and frequency of the converter (or inverter), influences the amount of regulation required after the conversion or inversion is completed, and provides the transformation ratio necessary to assure that the desired value of output voltage is delivered to the load circuit.

Inverters may be used to drive any equipment which requires an ac supply, such as motors, ac radios, television receivers, or fluorescent lighting. In addition, an inverter can be used to drive electromechanical transducers in ultrasonic equipment, such as ultrasonic cleaners and sonar detection devices. Similarly, converters may be used to provide the operating voltages for equipment that requires a dc supply.

Transistor inverters can be made very light in weight and small in size. They are also highly efficient circuits and, unlike their mechanical counterparts, have no moving components.

TYPES OF INVERTERS AND CONVERTERS

Several types of transistor circuits may be used to convert a steady-state dc voltage into either an ac voltage (inversion) or another dc

voltage (conversion). The simplest converter circuit is the blocking-oscillator, or ringing-choke, power converter which consists of one transistor and one transformer. More complex circuits use two transistors and one or two transformers.

In the ringing-choke type of dc-to-dc converter, a blocking oscillator (chopper circuit) is transformer-coupled to a half-wave rectifier type of output circuit. The rectifier converts the pulsating oscillator output into a fixed-value dc output voltage.

When the oscillator transistor conducts (as a result of either a forward bias or external drive), energy is transferred to the collector inductance presented by the primary winding of the transformer. The voltage induced across the transformer is fed back (from a separate feedback winding) to the transistor base through a resistor. This voltage increases the conduction of the transistor until it is driven into saturation. A rectifier diode in series with the secondary winding of the transformer is oriented so that no power is delivered to the load circuit during this portion of the oscillator cycle.

Fig. 138(a) shows the basic configuration for a practical ringing-choke converter, which is basically a one-transistor, one-transformer circuit. Fig. 138(b) shows the waveforms obtained during an operating cycle.

During the "on" or conduction period of the transistor (t_{on}), energy is drawn from the battery and stored in the inductance of the transformer. When the transistor switches off, this energy is delivered to the load. At the start of t_{on} , the transistor is driven into saturation, and a substantially constant voltage, waveform A in Fig. 138(b), is impressed across the primary by the battery. This primary voltage produces a linearly increasing current in the collector-primary circuit, waveform B. This increasing current induces substantially constant voltages in the base windings, shown by waveform C, and in the secondary winding.

The resulting base current is substantially constant and has a maximum value determined by the base-winding voltage, the external base resistance R_B , and the input conductance of the transistor. Because the polarity of the secondary voltage does not permit the rectifier diode to conduct, the secondary is open-circuited. Therefore, during the conduction period of the transistor t_{on} , the load is supplied only by energy stored in the output capacitor

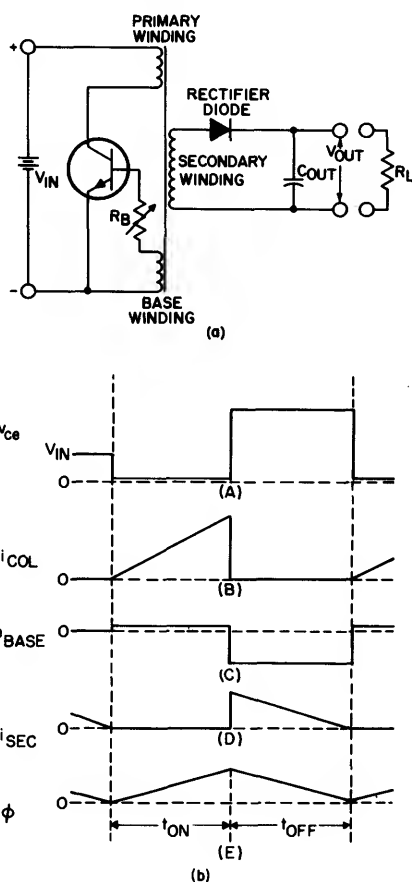


Fig. 138 - Ringing-choke converter circuit: (a) Schematic diagram; (b) Typical operating waveforms in a ringing-choke converter—(A) primary voltage; (B) primary current; (C) base-to-emitter voltage; (D) secondary current; (E) magnetic flux in transformer core.

C_{OUT} .

The collector-primary current increases until it reaches a maximum value I_P which is determined by the maximum base current and base voltage supplied to the transistor. At this instant, the transistor starts to move out of its saturated condition with the result that the collector-primary current and the voltage across the transformer windings rapidly decrease, and "switch-off" occurs.

After the transistor has switched off, the circuit starts to "ring", i.e., the energy stored in the transformer inductance starts to discharge into the stray capacitance of the circuit,

with the result that the voltages across the primary, base, and secondary windings reverse polarity. These reverse voltages rapidly increase until the voltage across the secondary winding exceeds the voltage across the output capacitor. At this instant the diode rectifier starts to conduct and to transfer the energy stored in the inductance of the transformer to the output capacitor and load. Because the output capacitor tends to hold the secondary voltage substantially constant, the secondary current decreases at a substantially constant rate, as shown by waveform D in Fig. 138(b). When this current reaches zero, the transistor switches on again, and the cycle of operation repeats.

The operating efficiency of the ringing-choke inverter is low, and the circuit, therefore, is used primarily in low-power applications. In addition, because power is delivered to the output circuit for only a small fraction of the oscillator cycle (i.e., when the transistor is not conducting), the circuit has a relatively high ripple factor which substantially increases output filtering requirements. This converter, however, provides definite advantages to the system designer in terms of design simplicity and compactness.

Transistor power inverter/converters are generally required to drive either a resistive or an inductive load. Each load affects the

transistor somewhat differently with respect to over-all switching power losses. There are essentially four classes of inverter/converter circuits commonly used:

1. Forward inverter
2. Flyback inverter
3. Push-pull switching inverter
4. Half-bridge or full-bridge inverter

Flyback and push-pull inverters are discussed below as illustrations of resistive and inductive loading.

Flyback Inverter

Fig. 139(a) shows a typical flyback converter circuit which uses a single transistor as the switching device. The transistor is driven with a positive rectangular input pulse of controllable width and constant period. In this circuit, when the base control or drive pulse turns on the transistor, a current I_P builds up in the primary winding (which serves as a choke) of transformer T1, as shown in Fig. 139(b). The secondary winding of the transformer is phased so that the diode D1 blocks the flow of secondary current at this time. The primary or collector current I_P rises linearly, provided the winding series resistance is low, to a final value determined by the primary winding L_1 , the supply voltage V_{CC} , and the turn-on duration t_{on} of the transistor. The transistor is considered to be inductively loaded. Energy is

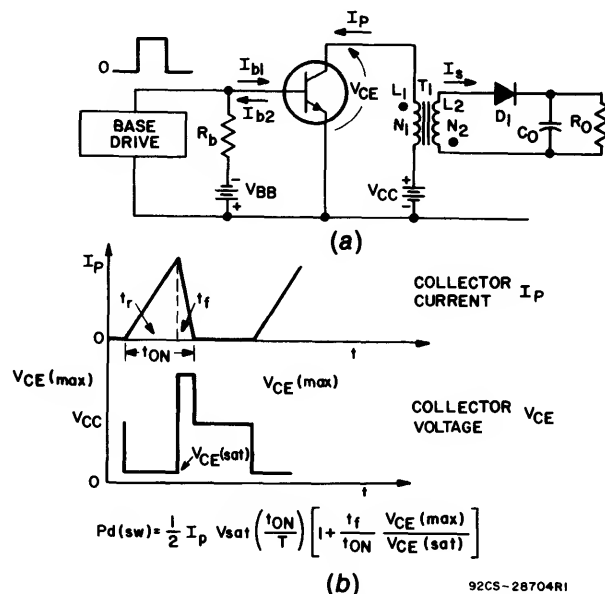


Fig. 139 - Flyback inverter circuit and waveforms.

stored in the primary winding during the on-time of the transistor. The maximum amount of energy stored must be sufficient to support the secondary load requirements. This energy is released into the secondary side after the transistor is turned off, and secondary current flows through the diode D1 into the filter capacitor C_0 and the load. In this circuit, however, the transistor is subjected to certain electrical stresses during the switching process which, if not clearly understood and controlled, can result in serious device degradation or failure.

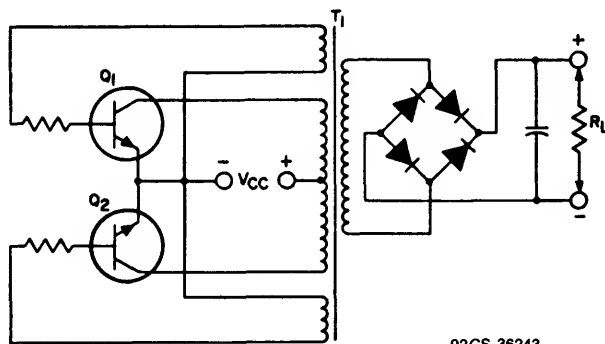
Push-Pull Transformer-Coupled Inverters and Converters

The **push-pull switching inverter** is probably the most widely used type of power-conversion circuit. For inverter applications, the circuit provides a square-wave ac output. When the inverter is used to provide dc-to-dc conversion, the square-wave voltage is usually applied to a full-wave bridge rectifier and filter. Fig. 140 shows the basic configuration for a push-pull switching converter. The single saturable transformer controls circuit switching and provides the desired voltage transformation for the square-wave output delivered to the bridge rectifier. The rectifier and filter convert the square-wave voltage into a smooth, fixed-amplitude dc output voltage.

When the voltage V_{CC} is applied to the converter circuit, current tends to flow through both switching transistors Q_1 and Q_2 . It is very unlikely, however, that a perfect balance can be achieved between corresponding active and passive components of the two transistor sections; therefore, the initial flow of current

through one of the transistors is slightly larger than that through the other transistor. If transistor Q_1 is assumed to conduct more heavily initially, the rise in current through its collector inductance causes a voltage to be induced in the feedback windings of transformer T_1 which supply the base drive to transistors Q_1 and Q_2 . The base-drive voltages are in the proper polarity to increase the current through Q_1 and to decrease the current through Q_2 . As a result of regenerative action, the conduction of Q_1 is rapidly increased, and Q_2 is quickly driven to cutoff.

The increased current through Q_1 causes the core of the collector inductance to saturate. The inductance no longer impedes the rise in current, and the transistor current increases sharply into the saturation region. For this condition, the magnetic field about the collector inductance is constant, and no voltage is induced in the feedback windings of transformer T_1 . With the cutoff base voltage removed, current is allowed to flow through transistor Q_2 . The increase in current through the collector inductance of this transistor causes voltages to be induced in the feedback windings in the polarity that increases the current through Q_2 and decreases the current through Q_1 . This effect is aided by the collapsing magnetic field about the collector inductance of Q_1 that results from the decrease in current through this transistor. The feedback voltages produced by this collapsing field quickly drive Q_1 beyond cutoff and further increase the conduction of Q_2 until the core of the collector inductance for this transistor saturates to initiate a new cycle of operation. The square wave of voltage produced by the



92CS-36243

Fig. 140 - Basic circuit configuration of a single-transformer push-pull switching converter.

switching action of transistors Q_1 and Q_2 is coupled by transformer T_1 to the bridge rectifier and filter, which develop a smooth, constant-amplitude dc voltage across the load resistance R_L . The small ripple produced by the square wave greatly simplifies filter requirements.

Push-pull transformer-coupled converters with full-wave rectification provide power to the load continuously and are, therefore, well suited for low-impedance, high-power applications. The push-pull configuration provides high efficiency and good regulation. In driven inverters such as that shown in Fig. 141(a), the output power transistor is switched by a multivibrator drive which is usually controlled by logic circuitry. Controlled-drive push-pull inverters are useful for precision systems requiring carefully controlled frequency or pulse-width control. Careful control of the input-drive pulse width, as in pulse-width-modulated switching systems, eliminates common-mode conduction between the transistors. Good load regulation can also be achieved.

As the switching-drive circuit in Fig. 141(a) alternately saturates and cuts off each transistor switch, an alternating voltage is generated across the winding of transformer T_1

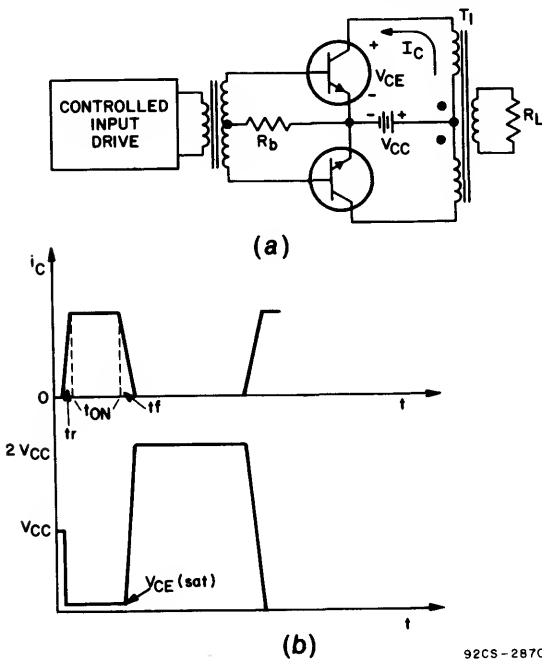


Fig. 141 - Driven inverter circuit and waveforms.

and delivered to the output circuit. A voltage equal to the dc supply voltage V_{CC} less the $V_{CE(sat)}$ of the conducting transistor is directly impressed across one-half the primary winding of T_1 . The voltage impressed across the non-conducting transistor is approximately twice the amplitude of V_{CC} . Although the voltages across the primary and secondary windings are always a square wave, no matter what load is used, the current waveform in the primary is not a square wave if other than a resistive load is used.

Fig. 142 shows a **four-transistor, single-transformer bridge configuration** that is often used in inverter or converter applications. In this type of circuit, the primary winding of the output transformer is simpler and the breakdown-voltage requirements of the transistors are reduced to one-half those of the transistors in the push-pull converter shown in Fig. 140.

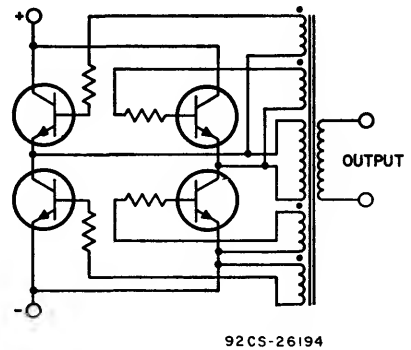
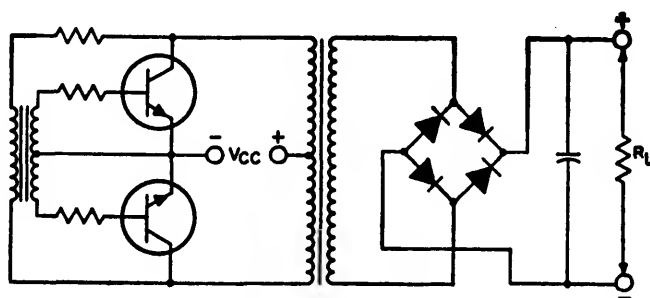


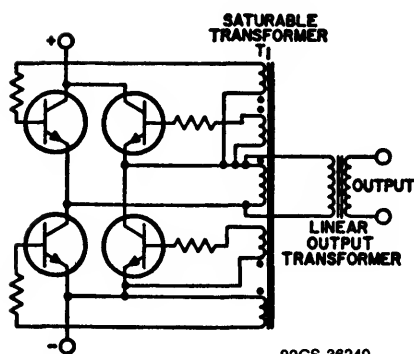
Fig. 142 - Basic circuit configuration of a four-transistor, single-transformer bridge inverter.

Fig. 143 shows the schematic diagram for a **two-transistor, two-transformer converter**. In this circuit, a small saturable transformer provides the base drive for the switching transistors, and a nonsaturable output transformer provides the coupling and desired voltage transformation of the output delivered to the load circuit. With the exception that it uses a separate saturable transformer, rather than feedback windings on the output transformer, to provide base drive for the transistors, this converter is very similar in its operation to the basic push-pull converter shown in Fig. 140. The saturable-transformer technique may also be applied in the design of a bridge converter, as shown in Fig. 144.



92CS-36242

Fig. 143 - Basic circuit configuration of a two-transformer push-pull switching converter.



92CS-36240

Fig. 144 - Basic configuration of a four-transistor bridge inverter that uses a saturable output transformer.

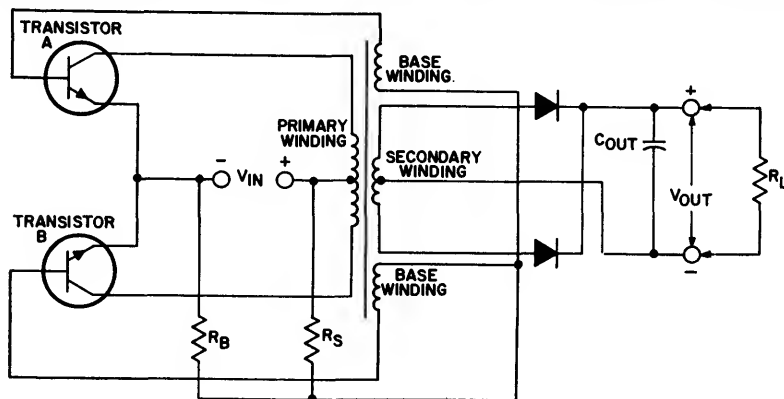
DESIGN OF PRACTICAL TRANSISTOR INVERTERS

The design of practical inverter (or con-

verter) circuits involves, essentially, selection of the proper transistors and design of the transformers to be used. The particular requirements for the transistors and transformers to be used are specified by the individual circuit design. The following paragraphs discuss the design of three basic inverter circuits: the simple one-transistor, one-transformer (ringing-choke) type and two push-pull switching converters (a two-transistor, one-transformer type and a two-transistor, two-transformer type). The operation of each circuit is described. For design equations and sample designs, refer to **RCA Solid State Power Circuits Handbook, SP-52 Series**.

Two-Transistor, One-Transformer Converter

Fig. 145 shows a push-pull, transformer-coupled, dc-to-dc converter that uses one transformer and two transistors. Fig. 146 shows the waveforms obtained from this



92CS-26181

Fig. 145 - Two-transistor, one-transformer push-pull switching converter.

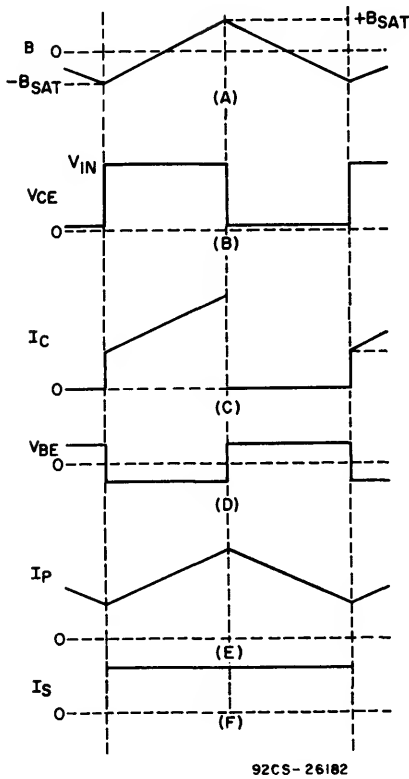


Fig. 146 - Typical operating waveforms for a two-transistor, one-transformer switching converter: (A) flux density in transformer core; (B) collector voltage of one transistor; (C) collector current of one transistor; (D) base voltage of one transistor; (E) primary current; (F) secondary current.

circuit during one complete operating cycle.

During a complete cycle, the flux density in the transformer core varies between the saturation value in one direction and the saturation value in the opposite direction, as shown by waveform A in Fig. 146. At the start of the conduction period for one transistor, the flux density in the core is at either its maximum negative value ($-B_{sat}$) or its maximum positive value ($+B_{sat}$).

For example, transistor A switches "on" at $-B_{sat}$. During conduction of transistor A, the flux density changes from its initial level of $-B_{sat}$ and becomes positive as energy is simultaneously stored in the inductance of the transformer and supplied to the load by the

battery. When the flux density reaches $+B_{sat}$, transistor A is switched off and transistor B is switched on. The transformer assures that energy is supplied to the load at a constant rate during the entire period that transistor A conducts. This energy-transformation cycle is repeated when transistor B conducts.

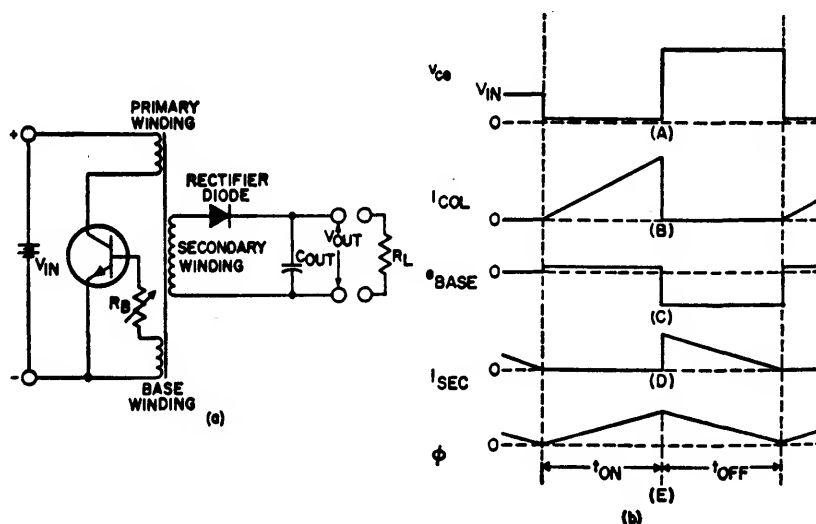
Initially, sufficient bias is applied to saturate transistor A. As a result, a substantially constant voltage, waveform B in Fig. 146, is impressed across the upper half of the primary winding by the dc source V_{in} . This bias voltage can be a temporary bias, a small fixed bias, or even a small forward bias developed across the bias winding as a result of leakage and saturation current flowing in the transformer primary. The constant primary voltage causes a dc component and a linearly increasing component of current, waveform C in Fig. 146, to flow through transistor A. As in the ringing-choke converter, the linearly increasing primary current induces substantially constant voltages, waveform D in Fig. 146, in the base winding and secondary winding. The induced voltage in the base winding limits the maximum value of the base current and, therefore, of the collector current.

In the push-pull transformer-coupled converter, the transition to switch-off is initiated when the transformer begins to saturate. As long as the transistor is not saturated, the product of the transformer inductance and the time rate of change of the collector current remains constant. When the transformer core saturates, however, the inductance decreases rapidly toward zero, with the result that the time rate of change of the collector current increases towards infinity. When the collector current reaches its maximum value, transistor A moves out of saturation and the winding voltages decrease and then reverse and thereby cause transistor A to switch off. The reversal of the winding voltages switches transistor B on, and the switching operation is repeated.

One-Transistor, One-Transformer Converter

Fig. 147(a) shows the basic configuration for a practical circuit of a ringing-choke converter, which is basically a one-transistor, one-transformer circuit. Fig. 147(b) shows the waveforms obtained during an operating cycle.

During the "on" or conduction period of the transistor (t_{on}), energy is drawn from the battery and stored in the inductance of the transformer. When the transistor switches off,



92CS-36241

Fig. 147 - Ringing-choke converter circuit: (a) Schematic diagram; (b) Typical operating waveforms in a ringing-choke converter—(A) primary voltage; (B) primary current; (C) base-to-emitter voltage; (D) secondary current; (E) magnetic flux in transformer core.

this energy is delivered to the load. At the start of t_{on} , the transistor is driven into saturation, and a substantially constant voltage, waveform A in Fig. 147(b), is impressed across the primary by the battery. This primary voltage produces a linearly increasing current in the collector-primary circuit, waveform B. This increasing current induces substantially constant voltages in the base windings, shown by waveform C, and in the secondary winding.

The resulting base current is substantially constant and has a maximum value determined by the base-winding voltage, the external base resistance R_B , and the input conductance of the transistor. Because the polarity of the secondary voltage does not permit the rectifier diode to conduct, the secondary is open-circuited. Therefore, during the conduction period of the transistor t_{on} , the load is supplied only by energy stored in the output capacitor C_{out} .

The collector-primary current increases until it reaches a maximum value I_P which is determined by the maximum base current and base voltage supplied to the transistor. At this

instant, the transistor starts to move out of its saturated condition with the result that the collector-primary current and the voltage across the transformer windings rapidly decrease, and "switch-off" occurs.

After the transistor has switched off, the circuit starts to "ring", i.e., the energy stored in the transformer inductance starts to discharge into the stray capacitance of the circuit, with the result that the voltages across the primary, base, and secondary windings reverse polarity. These reverse voltages rapidly increase until the voltage across the secondary winding exceeds the voltage across the output capacitor. At this instant the diode rectifier starts to conduct and to transfer the energy stored in the inductance of the transformer to the output capacitor and load. Because the output capacitor tends to hold the secondary voltage substantially constant, the secondary current decreases at a substantially constant rate, as shown by waveform D in Fig. 147(b). When this current reaches zero the transistor switches on again, and the cycle of operation repeats.

Two-Transistor, Two-Transformer Inverters

There are three basic disadvantages associated with the two-transistor, one-transformer inverter. First, the peak collector current is independent of the load. This current, therefore, depends on the available base voltage, the gain of the transistor, and the input characteristic of the transistor. Second, because of the dependence of the peak current on transistor characteristics, the circuit performance depends on the particular transistor used because there is a wide spread in transistor characteristics. Third, the transformer, which is relatively large must use expensive square-loop material and must have a high value of flux density at saturation. These disadvantages can be overcome by the use of two transformers in various circuit arrangements, such as that shown in Fig. 148.

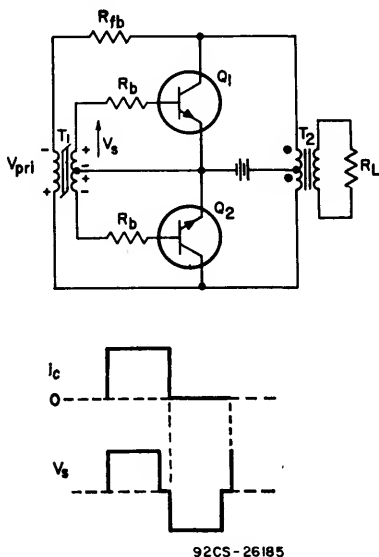


Fig. 148 - Two-transistor, two-transformer push-pull switching inverter.

In this type of circuit, a saturable base-drive transformer T_1 controls the inverter switching operation at base-circuit power levels. The linearly operating output transformer transfers the output power to the load. Because the output transformer T_2 is not allowed to saturate, the peak collector current of each transistor is determined principally by the value of the load impedance. This feature provides high circuit efficiency. The operation of the inverter circuit is described as follows.

It is assumed that, because of a small unbalance in the circuit, one of the transistors, Q_1 for example, initially conducts more heavily than the other. The resulting increase in the voltage across the primary of output transformer T_2 is applied to the primary of base-drive transformer T_1 in series with the feedback resistor R_{fb} . The secondary windings of transformer T_1 are arranged so that transistor Q_1 is driven to saturation. As transformer T_1 saturates, the rapidly increasing primary current causes a greater voltage drop across feedback resistor R_{fb} . This increased voltage reduces the voltage applied to the primary of transformer T_1 ; thus, the drive input and ultimately the collector current of transistor Q_1 are decreased.

In the circuit arrangement shown in Fig. 148, the base is driven hard compared to the expected peak collector current (forced beta of ten, for example). If the storage time of the transistor used is much longer than one-tenth of the total period of oscillation T , the transistors begin to have an appreciable effect on the frequency of operation. In Fig. 148, the storage time could conceivably be quite long because there is no turn-off bias (the drive voltage only decreases to zero) for Q_1 until the collector current of Q_1 begins to decrease.

Two methods of overcoming this problem by decreasing the storage time are shown in Fig. 149. In Fig. 149(a) a capacitor is placed in parallel with each base resistor R_b . When V_s is positive, the capacitor charges with the polarity shown. When V_s decreases to zero, this capacitor provides turn-off current for the transistor. In Fig. 149(b), a feedback winding from the output transformer is placed in series with each base. The base-to-emitter voltage V_{BE} is then expressed as follows:

$$V_{BE} = V_s - V_{fb} - V_T$$

If V_s decreases to zero and the collector current does not begin to decrease, then the base-to-emitter voltage is expressed simply by

$$V_{BE} = V_{fb} - V_T$$

A turn-off bias is thus provided to decrease the collector current.

The energy stored in the output transformer by its magnetizing current is sufficient to assure a smooth changeover from one transistor to the other. The release of this stored energy allows the inverter-circuit switching to be accomplished without any possibility of a

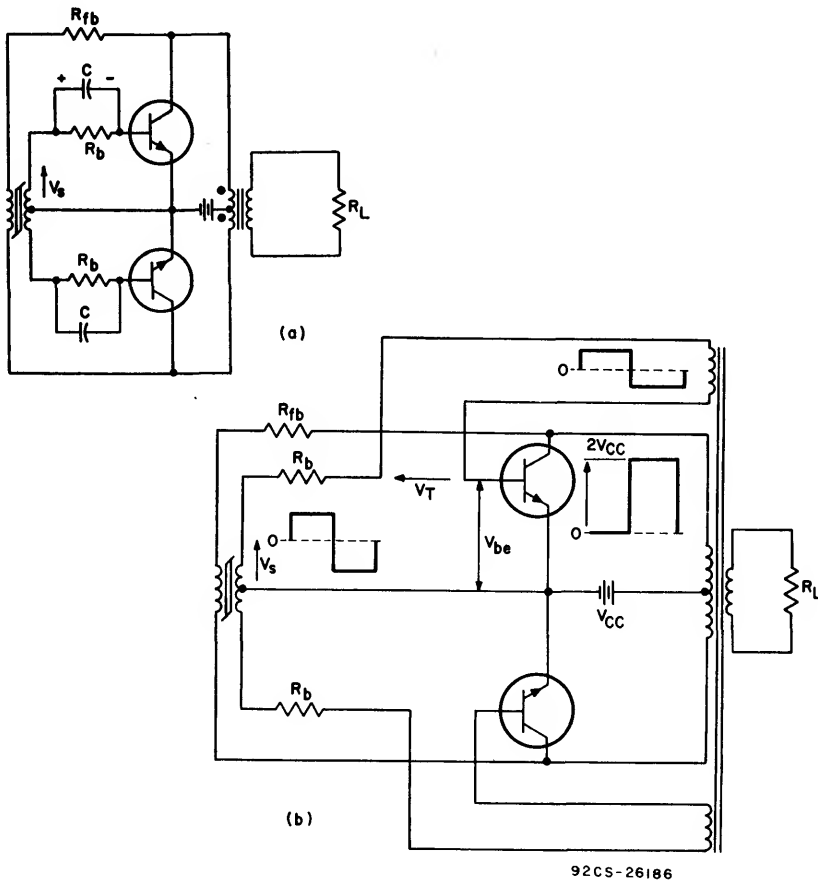


Fig. 149 - Two-transistor, two-transformer push-pull switching inverters in which transistor-storage times are reduced: (a) Capacitor in parallel with each base resistor assures sharp turn-off of associated transistor; (b) Feedback winding from output transformer in series with base of each transistor assures sharp cutoff characteristics.

"hang-up" in the crossover region during the short period when neither transistor is conducting.

The operation of the high-speed converter is relatively insensitive to small system variations that may cause slight overloading of the circuit. Under such conditions, the base power decreases; however, this loss is so small that it does not noticeably affect circuit performance. At the same time, the amount of energy stored in the output transformer also increases. Although this increase results in a greater

transient dissipation, the inverter switching is still effected smoothly.

A practical design of the high-speed converter should include some means of initially biasing the transistors into conduction to assure that the circuit will always start. Such starting circuits, as described later, can be added readily to the converter, and are much more reliable than one which depends on circuit imbalance to shock the converter into oscillation.

Four-Transistor Bridge Inverters

Fig. 150 shows a four-transistor, single-transformer bridge configuration that is often used in inverter or converter applications. In this type of circuit, the primary winding of the output transformer is simpler and the breakdown-voltage requirements of the transistors are reduced to one-half those of the transistors in the push-pull converter shown in Fig. 145.

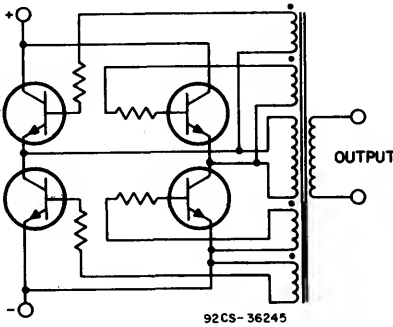


Fig. 150 - Basic circuit configuration of a four-transistor, single-transformer bridge inverter.

The separate saturable-transformer technique may also be applied in the design of a bridge converter, as shown in Fig. 151.

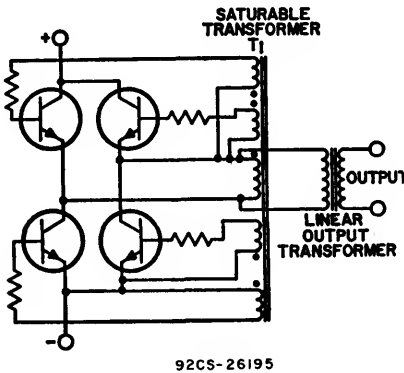


Fig. 151 - Basic configuration of a four-transistor bridge inverter that uses a saturable output transformer.

Three-phase bridge inverters for induction motors are usually used to convert dc, 60-Hz, or 400-Hz input to a much higher frequency, possibly as high as 10 kHz. Increasing frequency reduces the motor size and increases the horsepower-to-weight ratio, desirable features in military, aviation, and portable

industrial power-tool markets. Fig. 152 shows a typical three-phase bridge circuit with base driving signals and transformer primary currents.

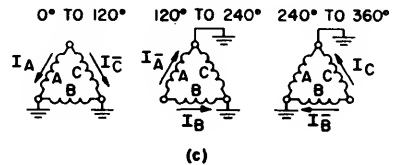
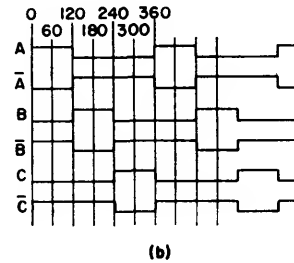
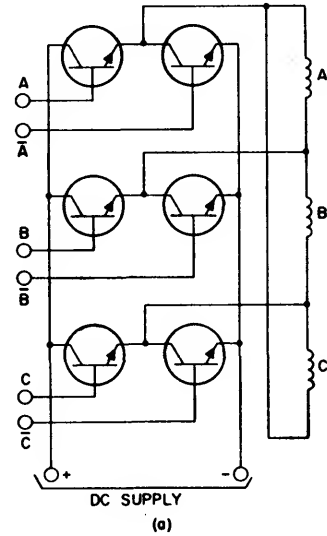


Fig. 152 - Three-phase bridge inverter: (a) circuit configuration; (b) base driving signals; (c) transformer primary current switching.

DESIGN OF OFF-THE-LINE INVERTER AND CONVERTER CIRCUITS

Power transistors have been used successfully in the past to generate and control large amounts of ac or dc power at low frequencies such as 60 and 400 cycles. At these low frequencies, however, most power sources are

bulky because large amounts of magnetic materials are required in transformers and inductors, particularly if kilowatts of power output are required.

The current trend in power inverter/converter designs is to use higher-frequency switching techniques and direct operation from the available utility lines (i.e., 110/220 V). The use of higher operating frequencies reduces not only the magnetic materials required but also the size of the filter capacitors. Direct off-line operation and the use of power transistors with high voltage breakdowns and peak-current-handling capabilities, combined with high-frequency switching techniques, have resulted in a new generation of power sources which are substantially smaller and have good efficiency and reliability.

General Design Considerations

The designer of a power inverter/converter usually must satisfy certain specification requirements, such as ac or dc power output, ac or dc input voltage, output frequency and waveform (inverter), load characteristics (including starting load, phase angle, duty cycle, and desired regulation), efficiency, maximum size and weight, minimum and maximum operating temperature (or other environmental requirements), and cost effectiveness.

The circuit designer's first task is to select a switching transistor capable of performing the intended function most economically and efficiently. Information supplied by manufacturers is usually very general, and the circuit engineer has the problem of relating this information to his particular design requirements. His selection of the switching transistor may be further complicated by a limited knowledge of the relative merits of transistors as switching devices. The designer may be inclined to select devices which are compatible with his experience, although not necessarily cost-effective. Selection of the proper switching device can be simplified if the relative merits of transistor switching capabilities are better understood.

Selection of the Switching Device

The selection of a switching transistor depends primarily on the power output level required. Table VIII lists the characteristics of the 2N6678 SwitchMax power transistor.

A switching device for off-line, high-frequency, switch-mode inverter circuits must possess the following characteristics:

- (a) High-voltage breakdown capability to withstand the maximum peak inverse voltage and transient voltages encountered.

Table VIII - Device Characteristics

| Characteristic | Transistor 2N6678 |
|---------------------------|--|
| Max. Voltage | $V_{CE0}=400\text{ V}$ |
| Peak Current | $I_C=15\text{ A}$ |
| Switching Characteristics | $t_r=0.6\text{ }\mu\text{s}$ $t_f=0.5\text{ }\mu\text{s}$ |
| Forward Voltage Drop | $V_{CE(sat)}=1\text{ V}$ @ $I_C=15\text{ A}$ |

- (b) High peak current capability to support the output load current demand.
- (c) Fast switching speed characteristics (i.e., sufficiently low turn-on and turn-off times) to minimize transient switching power dissipation.

Transistors are available which possess all of these unique features. The RCA-2N6678 transistor is a representative device for high-frequency power-switching applications.

Fig. 153 shows that the RCA-2N6678 can provide peak collector currents of 15 amperes with current gain of 8 up to approximately 22 kHz. The peak current of the transistor is limited by both gain and dissipation at high frequencies. Because the maximum V_{CE0} of the RCA-2N6678 is 400 volts, the transistor is limited to 110-V, off-line application in both single-ended (flyback) and push-pull circuits.

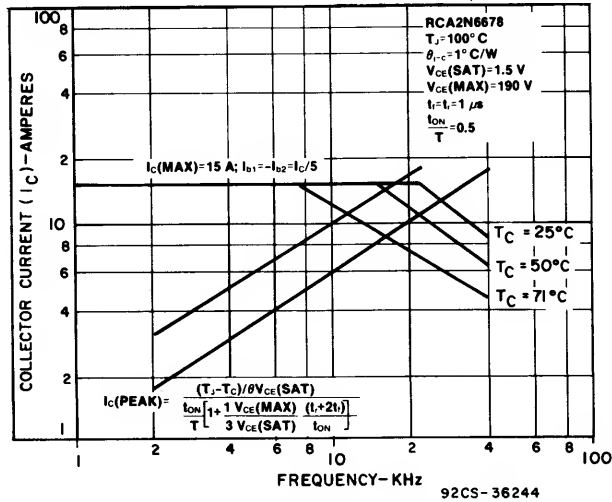


Fig. 153 - I_C as a function of frequency in the push-pull arrangement.

230-WATT, 40-KHZ, OFF-LINE FORWARD CONVERTER

The performance of the 2N6673 SwitchMax power transistor is demonstrated in the following 230-watt, 15-volt, 15-ampere off-

line converter operating at 40 kHz from a 120-volt, 60-cycle line; a block diagram of the circuit is shown in Fig. 154. The 2N6673 is designed, characterized, and tested for the parameters critical to this type of converter

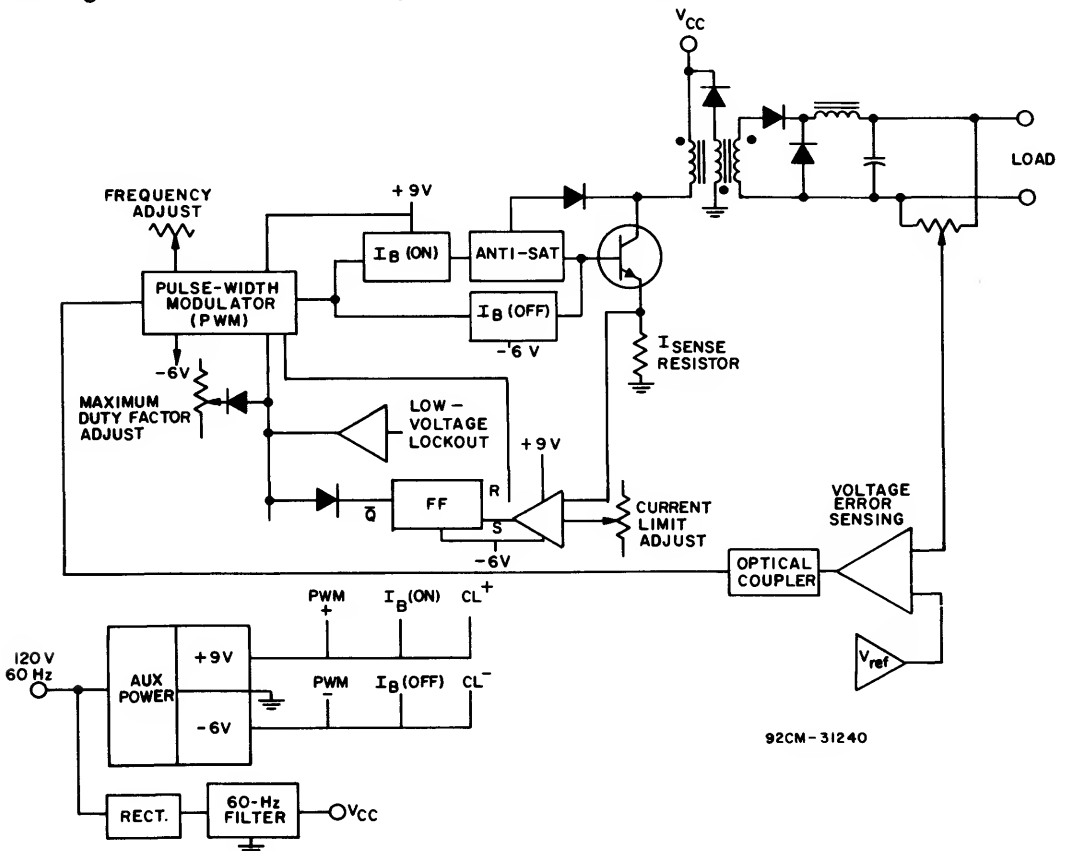


Fig. 154 - Block diagram of 230-watt single-ended converter.

design which is capable of providing 230 watts output, 15.5 amperes at 15 volts, from a low line of 100 volts rms to a high line of 135 volts. At high line, the power-switching device dissipates only 17 watts (4 watts saturation plus 13 watts switching). Table IX shows the performance to be expected from this converter. The primary purpose of this circuit is to demonstrate switching-device/circuit-format compatibility and capability and not to propose the design of a converter complete to commercial standards.

Table IX - Converter Performance

Regulation

Regulation is 0.2% from no load at $V_{\text{high line}}=135 \text{ V(rms)}$ to 230-watt load at $V_{\text{low line}}=100 \text{ V(rms)}$.

Overall Efficiency

Overall efficiency, including blower and auxiliary power is 70% at low line (100 V(rms)) to 67.24% at high line (135 V(rms)).

Efficiency of Converter System Alone

Efficiency of converter system alone is 78% or
 234 watts out
 299 watts in

Ripple

40-kHz ripple is 20 mV or better, Fig. 7(b), 60/120-Hz ripple is unmeasurable at 50 mV/division, Fig. 7(d).

HF Switching Noise

HF switching noise is approximately 1.2 volts peak-to-peak, the exact value is obscured by rfi received on load-box leads and shielding problems in the measurement.

Transient Response

Transient response at no load to full load: $V_{\text{drp}}=2 \text{ volts maximum}$; 90% recovery in 5 milliseconds or less.

The advantages of the forward converter design are its electrical simplicity and parts economy. These advantages are manifest by:

1. The simple power transformer.
2. The single power-switching device required.
3. Single-ended operation which, with the tertiary demagnetizing winding, avoids the core saturation problems caused by the unmatched switching characteristics

or winding dissymmetries that occur in some push-pull configurations.

4. The faster response to step changes in load made possible by the availability of higher than normal switching frequencies.

The following considerations must be observed to assure reliable forward-converter operation; these considerations are given below in the form of comparisons with a push-pull type of converter.

1. The transformer core must have 1.5 to 2 times the cross section of a push-pull core because of the unsymmetrical flux operation.
2. Because of the reduced duty factor allowed for the forward converter (0.5 maximum), the output choke must be correspondingly large or the switching frequency must be increased.
3. The power-switching devices and high-frequency rectifiers must be able to handle up to twice the peak current that devices in a push-pull design of the same power would be required to handle.
4. Because of the transformer and choke considerations mentioned above, it is desirable to increase the operating frequency of the forward converter beyond that which would be used with a push-pull converter. This increase mandates proportionately increased switching losses in the power switch, thus requiring faster switches or larger heat sinks and/or more sophisticated drive techniques. The SwitchMax transistor has demonstrated its special amenability to the higher temperatures and enhanced base-drive characteristics required for successful performance in forward converter systems.

The design of the subject converter proceeded from the operational switching ratings of the 2N6673 transistor:

1. $V_{\text{CE(sat)}}=2 \text{ V max.}$
 $V_{\text{BE(sat)}}=1.6 \text{ V max.}$
 $@ I_{\text{C}}=5 \text{ A}/I_{\text{B}}=1 \text{ A}$
 $T_{\text{J}}=125^{\circ} \text{ C}$
2. $t_{\text{a}}=4 \mu\text{s max.}$
 $t_{\text{c}}=0.8 \mu\text{s max.}$
 $@ I_{\text{C}}=5 \text{ A}, I_{\text{B1}}=I_{\text{B2}}=1 \text{ A}$
 $V_{\text{clamp}}=450 \text{ V}$
 $\text{Load}=25 \Omega + 170 \mu\text{H}$
 $T_{\text{J}}=125^{\circ} \text{ C}$
3. $V_{\text{CEX(clamped)}}=450 \text{ V}$

Within the constraints of the forward converter configuration, an available conversion power of 234 watts was determined based on the application of these ratings in the following relationship:

$$\text{Maximum Conversion Power} = V_{CC}(\text{low line}) \times I_{C(\text{max})} \times D(\text{max}) \times \text{Efficiency}$$

where $V_{CC}=130$ V, $I_{C(\text{max})}=5$ A, $D(\text{max})=\text{Maximum Duty Factor}=0.4$, and $\text{Efficiency}=90\%$.

$D(\text{max})$ was chosen as 0.4 rather than 0.5 to allow for a $2.5 \mu\text{s}$ dead-space guardband at 40 kHz. The 15-volt output voltage permits use of the breadboarded circuit as a utility bench supply so that experience with the circuit can be gained.

The turn-off time losses in a switching circuit are approximated by the following relationships:

1. For the resistive load case:

$$P_F(R) = \frac{t_r \times I_{C(\text{peak})} \times V_{CE(\text{peak})} \times f}{6}$$

2. For the clamped inductive load case:

$$P_F(I) = t_c \times I_{C(\text{peak})} \times V_{CE(\text{peak})} \times f \times 0.4$$

Assuming an operating frequency f of 40 kHz and a worst-case junction temperature of 125°C , calculations based on data-sheet values of t_r , t_c and a high line V_{CC} of 200 volts yields a $P_F(R)$ of 12 watts and a $P_F(I)$ of 29 watts. If a reasonable value of system thermal resistance, junction-to-air, of 3.3°C/W is also assumed, the maximum allowable ambient temperature $t(\text{amb.})$, for the resistive condition is $T(\text{amb.}) = T_J(\text{max}) - P_F(R) \cdot R_{JCSA} = 125 - 12 \times 3.3 = 85.4^\circ\text{C}$. For the inductive case the same initial expression would yield $125 - 29 \times 3.3$ for a $T(\text{amb.})$ allowable of 29.3°C .

Of course, the high line V_{CC} and full load will not exist for more than a few seconds, and the steady-state $P_F(I)$ at high line will be closer to 26 watts, allowing a maximum ambient temperature of 39°C .

Now that the forward converter design has been shown to be thermally practical from the device standpoint, storage time must be considered. As indicated previously the t_c condition represents a worst-case data-bulletin limit obtained with a forced gain of 5 ($I_C=5$ A, $I_{B1}=I_{B2}=1$ A). Furthermore, this condition implies a worst-case t_c (storage time) of 4 microseconds at 125°C . At $f=40$

kHz, the total allowable on time (t_p) is only 12.5 microseconds, so that 4 microseconds of t_c would be intolerable. Therefore, either a proportional drive or an antisaturation clamp technique must be used to reduce the storage time. The design under discussion employs an antisaturation drive; a technique that reduces t_c to about 1 microsecond, a tolerable value. An added benefit of this choice of antisaturation drive is an improved fall time, both t_r and t_c being improved by a factor of 1.5 to 2. Reinforcement for the antisaturation drive decision comes with the recognition that t_c is at its lengthiest for light loads at low line voltage, and that base drive proportioning in some form is essential to the existence of a manageable storage time.

Circuitry

The schematic diagram of the power output circuit is shown in Fig. 155; discussion begins with the output terminals.

As previously stated, the terminal voltage is 15 volts. The energy-storage/filter system is conventional, except that the filter choke value of approximately 120 microhenries is greater than one might consider adequate for this sort of circuit. It must be recognized that in a half-wave circuit the maximum duty factor, D , must not exceed 0.5. The secondary voltage, V_s , must, therefore, be 2.2 to 4 times the output voltage, whereas, in a full-wave circuit, V_s would be 1.1 to approximately 2.2 times the output voltage.

During the on time, DT , the current, I_C , in the energy-storage choke will consist of two parts, the pedestal current, I_p , and the ramping current, i_R , as shown in Fig. 156. During the on time, DT , this current is supplied from the rectifier and appears to the power switch as:

$$(I_p + i_R) \times \frac{N_s}{N_p} = i_C \text{ (collector current)}$$

if primary magnetizing currents and losses are neglected. i_R can be found from the basic

$$\text{relationship } E = L \frac{di}{dt}; E = (V_s - V_o), di = i_R \text{ and } dt = DT \text{ where } D = \frac{V_o}{V_s}$$

The power output of the circuit and its efficiency will be largely dependent on the value of the ramp current, i_R . Referred to the primary side of the transformer, the peak ramp current should be less than 1 ampere at

Using a minimum load current of 0.5 amperes and a DT of 0.25 (corresponding to a high line voltage), a value for L of approximately 140 microhenries is determined. Therefore, a choke with an $L(\min)$ of 140 microhenries at an I_{DC} of 1 ampere or an $L(\min)$ of 80 microhenries at an I_{DC} of 15 amperes is required.

The output capacitor value was not optimized; the key to capacitor choice is low equivalent series impedance rather than absolute capacitance. The rectifiers in Fig. 155 are 1N3910 fast-recovery DO-5 stud units.

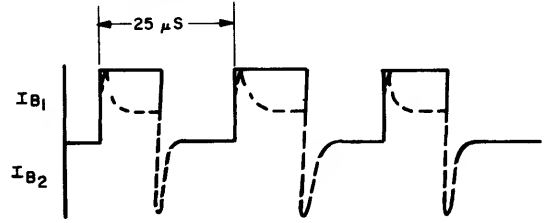
The secondary of the transformer was strap wound. While not necessary for the current level indicated above, the strap provided a neat, flat foundation on which to position the bifilar primary and tertiary windings so that the best coupling and lowest possible leakage inductance could be realized.

Leakage inductance, L_l with secondary and tertiary shorted, was measured at 16 microhenries. The energy stored in L_l at the end of each on period cannot be commutated to the secondary. It must, therefore, be dissipated as heat either in the transistor (where it becomes reverse-bias second-breakdown energy, $E_{S/b}$)

or in an auxiliary circuit called a "snubber".

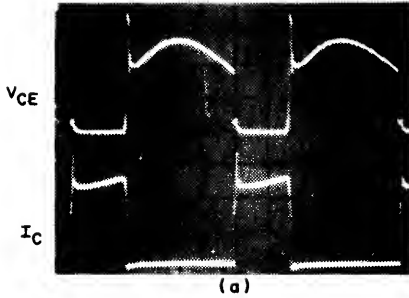
The snubber in this circuit consists of a 0.002 microfarad capacitor and a 50-ohm 5-watt resistor connected across the 2N6673 switch. This circuit will hold the worst-case collector spike voltage to less than 450 volts and the turn-on current spikes to less than 6 amperes.

The base drive arrangements of the forward-converter circuit are intended to provide 1 ampere of available I_{B1} drive by way of the

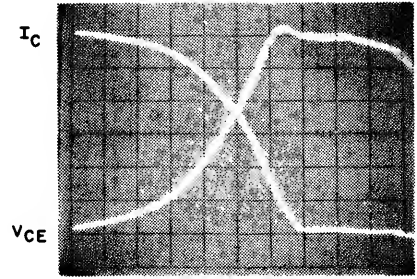


92CS-31243

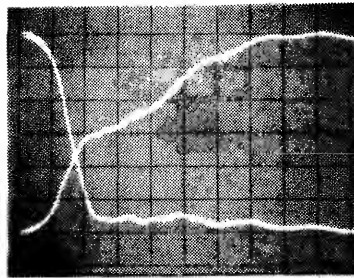
Fig. 157 - Base drive current applied to antisaturation network (solid line) and actual I_{B1} and I_{B2} in the 2N6673 base (dashed line).



(a)



(b)



(c)

92CS-31237

Fig. 158 - Turn-off switching behavior:

(a) Collector-voltage, collector-current waveform at $I_{Load}=15.5$ A, $V_{Load}=15$ V $V_{line}=120$ V (rms) $V_{CE}=100$ V/div., $I_C=2$ A/div. t (horizontal scale)=5 μ s/div.

(b) Fall time of power-switching transistor at $I_{Load}=15.5$ A, $V_{Load}=15$ V $V_{line}=120$ V (rms) $V_{CE}=360$ V, $I_C=5$ A t (horizontal scale)=50 ns/div.

(c) Fall time of power-switching transistor at $I_{Load}=3$ A, $V_{Load}=15$ V $V_{line}=120$ V (rms) $V_{CE}=210$ V, $I_C=3$ A peak t (horizontal scale)=50 ns/div.

2N6702, a high-speed, 7-ampere, medium-voltage switch. The combination of the D2201 fast-recovery clamp diode and the 1N5393 level-shift diodes cause the 2N6673 transistor to operate approximately 2 volts out of saturation, which greatly reduces the storage time by shunting the excess base current into the collector circuit as shown in Fig. 157. The device is turned off by a -6-volt V_{BB2} , further assuring minimal switching-loss heat generation. Turn-off switch behavior is shown in Fig. 158.

The designs of the +9-volt and -6-volt auxiliary supplies are straightforward and need no explanation.

Oscillator and Pulse-Width Modulator

The schematic diagram of the oscillator and pulse-width modulator circuit is shown in Fig. 159. The foundation of the control system is an oscillator/pulse-width-modulator integrated circuit. The oscillator-logic/comparator system powered by the +9 and -6-volt auxiliary supplies operates conventionally. The current-

limiter and shut-down facilities provided on the chip are not used. The error amplifier operating only as a voltage follower is driven from the collector of the 2N6702 photocoupler, which provides the phase inversion and dc isolation from load-to-line.

Voltage Sensing—The CA723 integrated circuit voltage regulator shown in Fig. 159 provides four functions of the voltage error-sensing system:

1. Reference-voltage supply for error amplifier
2. Error amplification (non-inverting)
3. LED drive to photocoupler
4. LED current limiting (with the addition of one zener)

The output stage of the CA723 is arranged as a current limiter to prevent over powering of the LED in the photocoupler.

Because the power converter operates from a 15-volt supply, the voltage reference, error amplifier, and photocoupler can be self-powered from the 15-volt output bus. With a

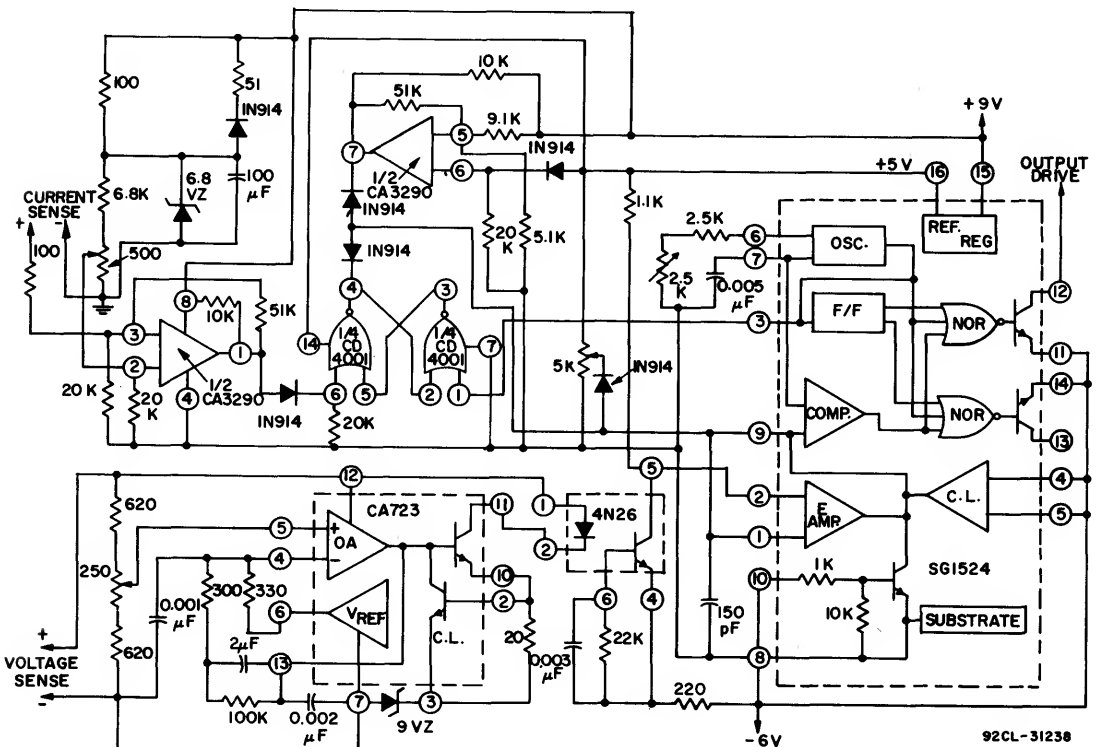


Fig. 159 - Schematic diagram of oscillator and pulse-width modulator circuit.

lower-voltage supply, the necessary operating voltage can be obtained with the aid of an extra rectifier-capacitor combination, directly from the secondary of the high-frequency transformer.

Auxiliary Functions—In addition to the following seven basic voltage-regulating functions:

1. Reference-Voltage Source
2. Error Amplifier
3. Photocoupler Isolator
4. Voltage Follower
5. Ramp Generator
6. Comparator
7. Logic Output

the power converter also provides the following:

8. Minimum Duty Factor Control to assure complete discharge of snubber network.
9. Maximum Duty Factor Control
10. "Soft-Start" and Low Line-Voltage Lockout
11. Pulse-by-Pulse Current Limiting

Functions 8 through 11 are discussed in more detail below.

Minimum Duty Factor—The minimum duty factor, $D(\min)$ is established by the emitter resistor in the 4N26 photocoupler; this resistor clamps the minimum voltage to the pulse-width modulator. For the snubber to operate effectively, the time at each operating point (switch on or switch off) must be sufficiently long so that the capacitor reaches equilibrium. Therefore, a minimum on time, DT , must be established for each cycle of at least t_{rise} plus five times the snubber RC product. In the circuit being considered, $RC = 50 \times 0.002 \times 10^{-6} = 0.1 \mu s$. Hence, a 1-microsecond minimum on time is adequate. The emitter resistor selected, 220 ohms, yields a minimum DT of approximately 2.5 microseconds, which provides ample margin.

Maximum Duty Factor—The maximum duty factor control must limit $D(\max)$ to less than 0.5, allowing for delays and storage in the remainder of the system, to assure that the transformer is demagnetized during the off time.

The maximum duty factor is set by adjusting the tap on a 5-kilohm potentiometer so that the maximum voltage that can appear at the comparator rail (terminal 9 on the pulse-width modulator) is limited. In the circuit being discussed, the potentiometer is set for a maximum on-pulse width of 10 microseconds

at no load with sensing disconnected for 40-kHz operation.

"Soft-Start" and Low Line-Voltage Lockout—Safe operation of pulse-width modulator supplies requires that the drive circuits and main load power be sequenced on and off in the proper order as the power supply, connected across the power mains, is turned on or off. If this condition is not complied with, severe stresses will be placed on the switching transistor, and device failure may result. An effective way to provide proper sequencing is to use a "soft start" (defined in statement 2, below), and a low-voltage lockout circuit. The objectives of the lockout circuit are to:

1. Apply drive to the power devices only after:
 - a. The oscillator is running at the proper frequency, 40 kHz.
 - b. Voltages for the base drive system are at full operating values.
 - c. The initial line-surge phase of the 60-Hz rectifier filter is complete.
2. Apply base drive in a "soft-start" fashion; i.e., start with minimum pulse width, but full base current, then slowly increase the pulse width to its full controlled value of 10 microseconds.
3. In the event of low line voltage, shut off the base drive pulse before deterioration of the base drive current occurs. Low base current causes partial switching of the power device and operation outside the safe operating area.
4. Upon restoration of proper line voltage, restore the supply to operation in the soft-start mode.

Pulse-by-Pulse Current Limiting—Pulse-by-pulse current limiting in the primary rather than dc-load side-current limiting was chosen as the limiting technique in the forward converter circuit for several reasons.

1. Current surges into the output capacitors at start-up are eliminated.
2. There is no problem with load-to-line isolation.
3. Damage control is simplified. Shorted rectifiers, shorted transformer or choke turns, transformer saturation, and excess load conditions can be sensed. The circuit can operate in an impaired condition without producing additional damage, thus simplifying service procedures.

A 0.03-ohm resistor is in series with the emitter of the 2N6673. The emitter-current

sensing voltage produced is applied to terminal 3, the non-inverting input of the second half of the CA3290 dual comparator. An adjustable reference voltage is applied to terminal 2. When the voltage at terminal 3 exceeds the reference on terminal 2, the output at terminal 1 goes high and triggers the CD4001 flip-flop which, in turn, crowbars the comparator rail (terminal 9) of the pulse-width modulator IC, and the drive pulse is terminated. At the start of the next half cycle, the flip-flop is reset by the clock pulse from terminal 3 of the pulse-width-modulator IC.

Note that the snap action of the comparator is assured by the positive feedback obtained through the 51-kilohm resistor connected between terminals 1 and 3 of the CA3290. This feedback eliminates any ambiguities in sensing.

Summary

This converter could be redesigned to handle 400 watts or more by using a second output unit (driver, output device and transformer) operating from the now unused phase of the SG1524 pulse-width modulator, or by substituting a 2N6675 in the output, making slight changes in the base drive resistance and using a larger output rectifier.

Again, as previously stated, this does not describe a finished commercial item. Rather it serves as a demonstration of switching-device/circuit-format capability. Only the full-time power-supply designer can envision all of the environments and contingencies that will be the ultimate determinants of the design of a finished product.

340-WATT, 20-KHZ FLYBACK CONVERTER

The power-switching capability of the RCA-2N6676 SwitchMax power transistor is demonstrated in the following high-power flyback converter. The circuit provides 340 watts of output power at 20 kHz when operated from a 110-volt ac power line. The resultant overall efficiency was determined to range from 82 to 86 percent for inputs of 150 to 190 volts dc to the converter stage.

Converter Circuit Description

The converter circuit, shown in Fig. 160 in block diagram form, is powered by a direct input from a 110-volt ac power line; this input is rectified by a full-wave bridge to provide a dc output. This dc source, which is filtered by a capacitor, serves as the power supply for the RCA-2N6676 power switch. The circuit also contains a driver stage which provides sufficient gain to allow interfacing between suitable low-power pulse-width-controlled modulator logic circuitry and the input of the high-level transistor switch. The reverse-bias ($-I_{b2}$) current amplifier provides reverse-bias current essential for rapid turn-off of the power switch. Overvoltage and overcurrent protection circuitry is also provided. The driver stage, reverse-bias amplifier, and protection circuit are discussed in this section together with the flyback output stage. The pulse-width control function, indicated by dashed lines in Fig. 160, is not discussed; adequate material is available to show the implementation of necessary logic-function designs.

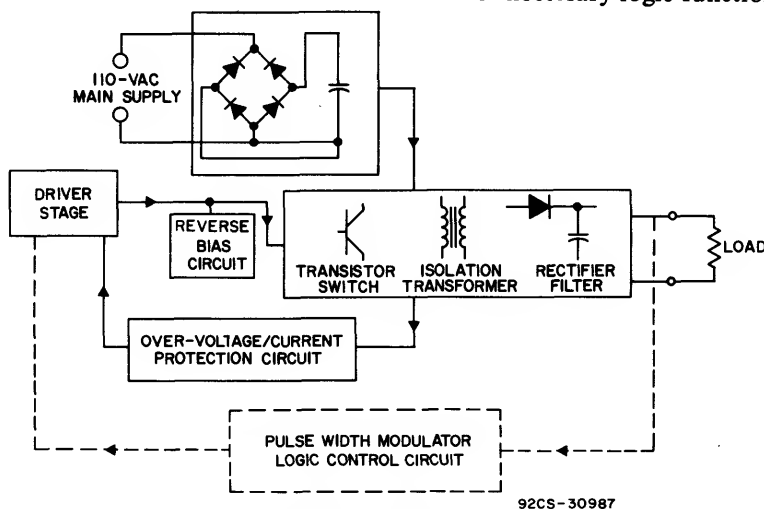


Fig. 160 - Block diagram of the converter circuit.

Output Stage

The flyback-type converter is generally not considered a high-power generator for three main reasons:

- 1. It requires approximately twice the peak current of a square-wave type.
- 2. It requires a larger output transformer as a result of the large magnitude of the dc current flowing and the need for a large air gap to avoid core saturation.
- 3. It requires, at low output voltage (5 to 12 volts), very large and expensive capacitors to obtain good ripple-voltage reduction.

However, the flyback converter does have several attractive features which make it worthy of consideration for applications requiring a high-power output:

- 1. Simplicity and low cost.
- 2. Provision for isolation of the secondary load from the main-line input voltage.
- 3. Suitability for multiple output supplies.
- 4. Suitability for medium-to-high levels of secondary voltages.

Fig. 161(a) shows a typical basic flyback-converter circuit that uses a single transistor as the switching device. The transistor is driven with a positive rectangular input pulse of controllable width and constant period. In this circuit, when the base control or drive pulse turns the transistor on, a current (I_p) builds up in the primary winding (which serves as a choke) of transformer T_1 , as shown in Fig. 161(b). The secondary winding of the transformer is phased so that diode D_1 blocks the flow of secondary current at this time. The primary or collector current I_p rises linearly, provided the winding series resistance is low, to a final value determined by the primary winding inductance, L_p , the supply voltage, V_{cc} , and the turn-on duration, t_{on} , of the transistor. The transistor is considered to be inductively loaded. Energy is stored in the primary winding during the on time of the transistor; the maximum amount of energy stored must be sufficient to support the secondary load requirements. This energy is released into the secondary side after the transistor is turned off; the secondary current flows through diode D_1 into filter capacitor C_o and the load R_o .

In the practical flyback circuit shown in Fig. 162, the output circuit employs an RCA-2N6676 power transistor (Q_4) as the power switch. The 110-volt ac power-line voltage is rectified and applied to the collector of the

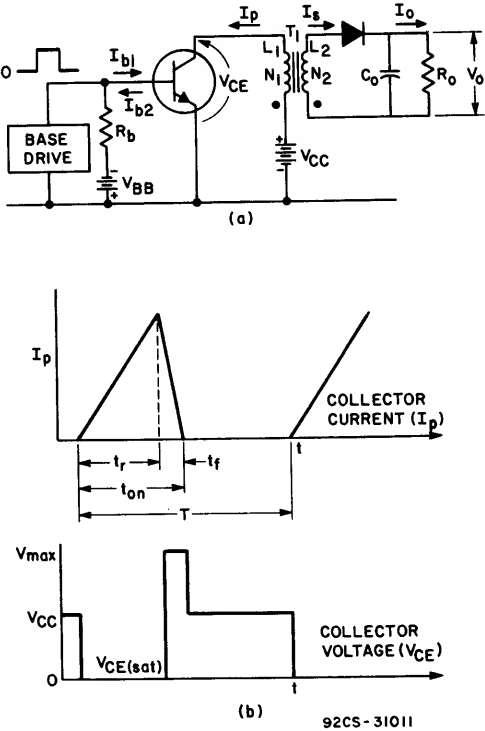
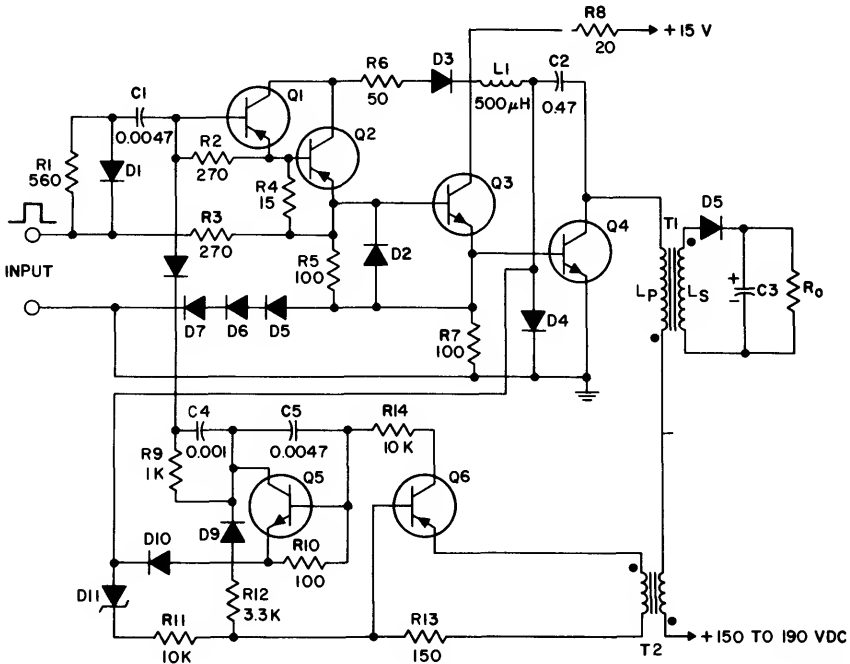


Fig. 161 - Basic flyback converter circuit and primary circuit waveforms.

power transistor through the primary winding of transformer T_1 . The primary inductance L_p of the transformer is determined by the maximum allowable peak collector current, $I_{c(pk)}$, the minimum dc input voltage (low ac line voltage), and the maximum width of the turn-on pulse at low line voltage. Generally the secondary load requirements together with the rectifier and transformer losses dictate the final value of the peak collector current. The peak collector current in the design shown was determined by the following conditions:

| | |
|--|-------------------|
| Operating Junction Temperature (T_j) | 100° C |
| Operating Case Temperature (T_c) | 50° C |
| $V_{ce(sat)}$ at $T_j=100^\circ\text{C}$ | 2 Volts |
| Operating Frequency (f) | 20 kHz |
| Duty Cycle | 50% |
| Inductive Turn-Off Time (t_c) | 0.8 μs |
| Maximum Collector Voltage, $V_{ce(sus)}$ | 450 V |
| Thermal Resistance, θ_{jc} | 1° C/W |



92CL-30996

Q1, Q6 = 2N5416; D1 = IN914
 Q2 = 2N6213; D2, D3, D4 = A280
 Q3 = 2N3878 OR 2N5038; D5, D6, D7 = IN1206
 Q4 = 2N6676 D8
 Q5 = 2N3439 D9 } = IN4937
 D10
 D11 = 400 V ZENER

T₁ = CORE: SIEMENS E CORE SET (N27)
 AIR GAP: 0.04 INCH
 PRIMARY: 29 TURNS, 30/36 LITZ
 SECONDARY: 10 TURNS, 30/36 LITZ
 (SANDWICHED LAYERS 1 PRI./2 SEC./1 PRI.)

T₂ = CORE FORM: 3/8 INCH OD, LENGTH 1.5 INCHES
 PRIMARY: L_P = 2 μH, WIRE SIZE No. 20
 SECONDARY: L_S = 2 μH WIRE SIZE No. 20

Fig. 162 - Practical flyback converter circuit.

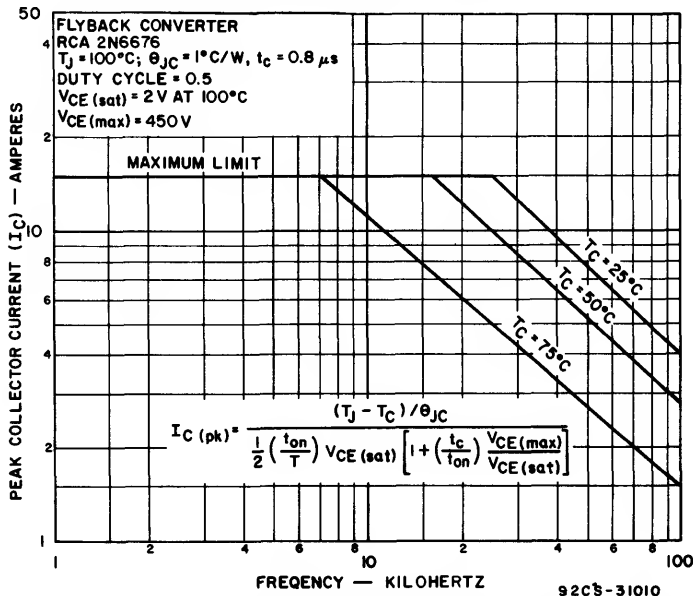


Fig. 163 - Peak collector current of the RCA-2N6676 as a function of frequency for three different case temperatures.

Fig. 163 shows a plot of the peak collector current of the RCA-2N6676 as a function of frequency for three different case temperatures. At a case temperature of 50°C, the peak collector current must be limited to 12 amperes. The flyback converter shown in Fig. 162 was designed to operate with a 20-kHz pulse-width modulated input drive signal and to provide a dc output of 48 volts with more than 300 watts of continuous output power.

An equally important part of the flyback converter is the output transformer, T_1 . The switching converter works by cyclically storing energy in the primary winding, L_p , and then dumping this stored energy into the load, which is connected to the secondary side of the transformer. The design of the output transformer is important not only because it affects the amount of output power and efficiency of the converter, but also because it determines the operating frequency range.

Switching Characteristics

The turn-on time of the RCA-2N6676 transistor for a given peak collector current is a function of the duration of the base turn-on drive current. Although the turn-off time is related to the amplitude of the negative base-current drive, particularly with regard to storage-time reduction, the actual turn-off time in the flyback circuit is determined by the characteristics of the 2N6676 transistor and the output transformer. However, the application of sufficient reverse base current minimizes the effects of the transistor turn-off time on the overall turn-off characteristics of the circuit. Fig. 164 shows the base current

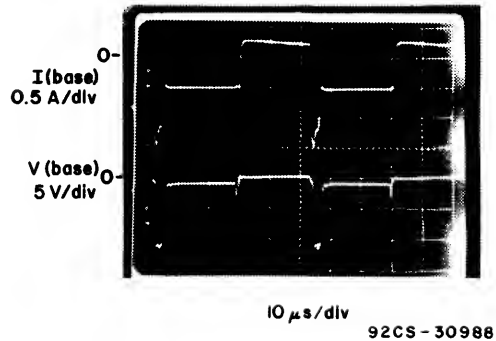


Fig. 164 - Base characteristics for the RCA-2N6676 at $V_{cc}=+150 V_{dc}$, $t=50 \mu s$, $t_{on}(\text{collector})=25 \mu s$.

and voltage waveforms during maximum output-load conditions. The base-current turn-on pulse has a peak value of 0.75 amperes. A peak reverse base current of 1 ampere is obtained with a negative base-to-emitter voltage of 12 volts.

The base-to-emitter junction can be operated into the avalanche region during the reverse-bias condition. The result is an enhancement in turn-off time with no immediate observable degradation in junction characteristics. This result is attributed to the low level of reverse-bias energy present during the reverse base current conduction time, (approximately 1.5 microseconds); the reverse-bias energy in the base-to-emitter junction is approximately 18 microjoules.

Performance

Typical collector current and voltage waveforms for the 2N6676 transistor are shown in Fig. 165(a); transformer secondary current and voltage waveforms at maximum output

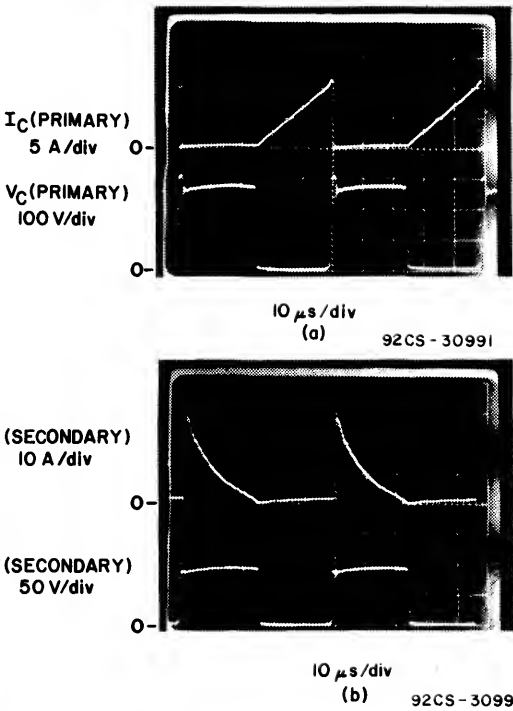


Fig. 165 - (a) Collector current and voltage (primary) for the RCA-2N6676 and (b) transformer secondary current and voltage at $V_{cc}=150 V_{dc}$, $t=50 \mu s$, $t_{on}=25 \mu s$, $V_o=48 V_{dc}$, $I_o=7.2 A$.

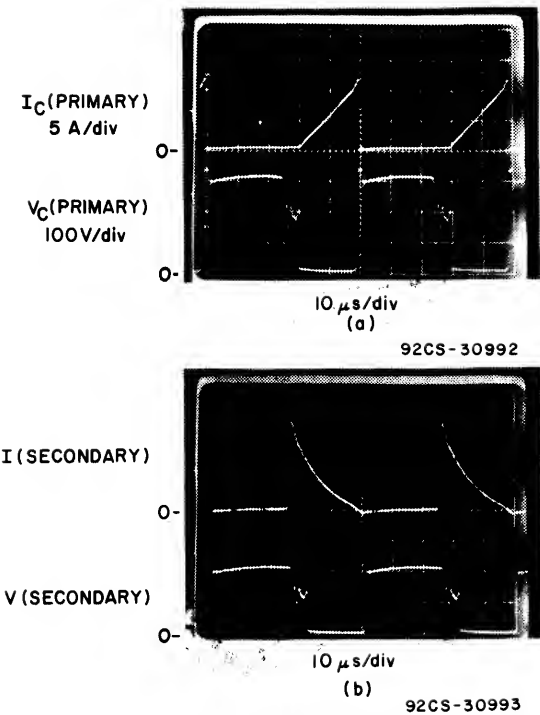


Fig. 166 - (a) Collector current and voltage for the RCA-2N6676, and (b) transformer secondary current and voltage at $V_{CC}=190$ V_{dc}, $t=50 \mu\text{s}$, $t_{on}=19 \mu\text{s}$, $V_o=48$ V_{dc}, $I_o=7.2$ A.

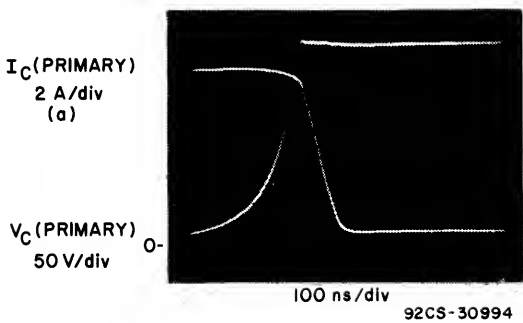


Fig. 167 - Turn-off characteristics for the RCA-2N6676 at $V_{CC}=190$ V_{dc}, $t=50 \mu\text{s}$, $t_{on}=19 \mu\text{s}$, $V_o=48$ V_{dc}, $I_o=7.2$ A.

power are shown in Fig. 165(b). The maximum output power of 345 watts was measured with a dc input of 150 volts and a turn-on pulse width of 25 microseconds at a frequency of 20 kHz.

Fig. 166 shows the performance of the flyback circuit at high line voltage, a V_{CC} of 190 volts. In order to limit the peak collector current to 10.8 amperes, the turn-on pulse width was reduced to 19 microseconds. The peak secondary current and voltage waveforms shown in Fig. 166 are identical to those shown in Fig. 165, indicating that this flyback converter design provides constant output power.

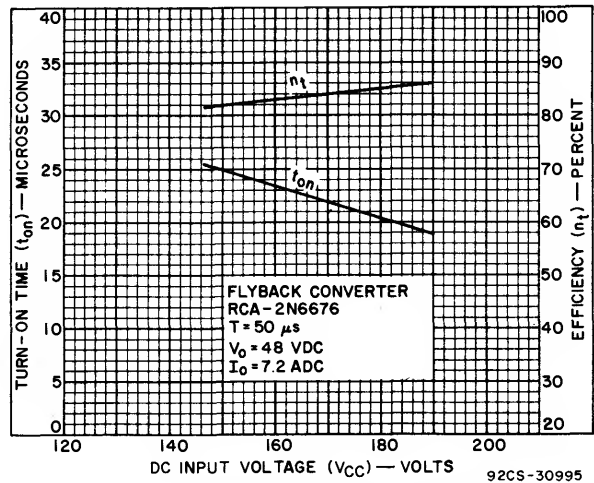


Fig. 168 - Overall efficiency of the RCA-2N6676 flyback converter stage (upper curve); efficiency with reduction of turn-on pulse width and increasing line voltage (lower curve).

Fig. 167 shows the turn-off characteristics of the 2N6676 transistor output stage at high line voltage, 190 volts, and reduced turn-on pulse width. The turn-off time interval, approximately 400 nanoseconds, was also reduced, indicating a reduction in turn-off dissipation in the transistor. The upper curve in Fig. 168 shows the overall efficiency of the RCA-2N6676 flyback converter stage; the efficiency ranges from 82 to 85.5 percent. The reduction of the turn-on pulse width with increasing line voltage results in high operating efficiency, as shown in the lower curve of Fig. 168.

Driver Stage

The driver stage of the converter, Q3, shown in Fig. 162, utilizes an RCA-2N5038 or 2N3878 transistor in an emitter-follower circuit configuration. The driver stage is operated from a separate 15-volt dc supply which is obtained from a line to a low-voltage transformer. The driver stage provides sufficient current gain to allow interfacing between suitable low-power pulse-width-controlled modulator logic circuitry and the input of the high-level transistor power switch. The driver stage serves as an impedance matching transformer as well as a current amplifier. In order to provide 750 milliamperes of base drive to the output power switch, the driver stage requires approximately 30 milliamperes of input base current.

Reverse-Bias Amplifier

The reverse-bias current, $-I_{b2}$, for power switch Q4 is provided by a current amplifier consisting of transistors Q1 (RCA-2N5416) and Q2 (RCA-2N6213). Because the reverse-bias circuit is somewhat uncommon, its operation is discussed in detail. The source of energy used to turn off power switch Q4 is stored in capacitor C2. During collector-current turn-off, the voltage developed across capacitor C2 is equal to the clamped flyback voltage across Q4; this voltage is limited to 400 volts. The voltage at the diode (D4) end of C2 becomes a negative value equal to the peak inverse or flyback voltage when the output transistor Q4 turns on. This negative voltage cannot be used directly as a source for $-I_{b2}$ since the peak flyback voltage (which is converted to zero volts at the D4 end of C2) occurs as I_c just starts to fall. To be effective, this negative voltage must be present during

the entire I_c fall time (as it would be in a purely resistive circuit). Inductor L1 is used in series with R6, C2, and the $-I_{b2}$ switching transistors Q1 and Q2 to maintain the required negative potential.

The reverse-bias current switch Q1, Q2 is turned on by the charge on C1 at the end of the input, or oscillator, pulse, at which time the voltage at C2 is -400 volts. The functions of L1 are:

1. To reduce the source voltage at R6 during conduction of $-I_{b2}$, thereby reducing dissipation in R6.
2. To reduce the influence of the flyback voltage, which would tend to nullify $-I_{b2}$ at this time since the voltage at C2 is zero.
3. To provide a ramping negative voltage across R6, which, in turn, creates an increasing $-I_{b2}$ during the fall time of the collector current of Q4 (a condition that tends to eliminate tailing). The end result is an output device, Q4, that experiences minimum dissipation because of a fast turn-off time.

As an added benefit of this circuit, capacitor C2 provides snubbing action. This benefit occurs because the charge that is dissipated by the reverse-bias current circuit must be replaced by the sustaining voltage, $V_{CE(sus)}$, of the output device, Q4. The reverse-bias current drain represents the resistance part of the RC network connected across the collector and emitter of output transistor Q4. The network acts as an inhibitor, at about 400 volts, on the operating range of the inverter.

Protection Circuitry

The protection circuit for the converter consists of transistors Q5 and Q6 and operates under the following conditions: short circuit, open circuit, 50-percent duty cycle exceeded, and high line voltage. Open-circuit and high line voltage conditions are detected simply by monitoring the flyback peak voltage across the output transistor, since both of these conditions manifest themselves as an excessive voltage across the device, a voltage that would ultimately destroy the device. The clamping action of C2 is not a rigid clamping action and, as a result, the peak V_{CEX} varies somewhat with line voltage and loading conditions. The maximum safe V_{CEX} was chosen as 400 volts.

The selection of R6 and L1 determines both the value of $-I_{b2}$ and the voltage level at which C2 effectively clamps. When the V_{CEX} of the

output device exceeds 400 volts, as it would during high line-voltage or open-circuit conditions, Q_6 turns on by conduction of the 400-volt zener diode D_{11} . Since the voltage at the diode end of C_2 becomes negative when Q_4 turns on, the level being determined by the peak positive voltage across the output transistor, Fig. 165, the zener diode will fire the protection circuit on the next conduction cycle after the peak voltage exceeds 400 volts. Even during a sudden open-circuit condition, this voltage cannot change instantaneously (because of the presence of C_2) and will take several cycles to rise above 400 volts. When Q_6 turns on, the base of Q_5 is effectively tied to the line voltage through R_{14} , while its emitter is at -400 volts. This arrangement provides about 40 milliamperes of base drive to Q_5 , and turns it on. Part of the collector current of Q_5 is fed back to Q_6 . This current maintains both Q_5 and Q_6 in a latched-on condition until the line voltage is switched off.

Short circuit and over-50-percent duty-cycle conditions are detected by inserting a small air-core transformer, T_2 , in series with the primary winding of the output transformer. Observation of the primary current waveform, Fig. 165(a), shows that, under normal conditions, the collector current of Q_4 ramps up gradually from a zero current level. Under conditions of over 50-percent duty cycle, abnormally high current demands, or a short circuit, the waveform changes. All of the above conditions cause the same change in varying degrees, that is, a step up from the zero current level before the ramp starts. This step occurs, because, in all of the above conditions, the secondary current continues to flow even after the start of the next cycle.

The connection of the current-sensing transformer to Q_5 provides for a starting pulse to the Q_5, Q_6 switch whenever there is an appreciable step in current in the positive direction. There is always a very large step in the negative direction as a result of the fall time of the collector current in the output transistor, Q_4 . This negative step is bypassed around Q_6 by D_9 .

A 450-WATT, 40-KHZ, 240-VAC TO 5-VDC, FORWARD CONVERTER

The principles and virtues of the forward-converter circuit are well known, and this type of circuit has been advocated for some time. Until recently, however, a main drawback to

its use in high-power and high-frequency power supplies has been the lack of high-voltage power transistors with fast enough rise and fall times. Development of RCA's SwitchMax transistor family makes possible the design of a single forward converter of 450 watts output that can operate from nominal mains of 240 volts ac and a 40-kHz switching frequency.

A block diagram of such a converter is shown in Fig. 169.

Performance Considerations

Some of the advantages and disadvantages of the forward-converter circuit are:

Advantages:

1. Superficially a simple circuit.
2. No transformer balance problem.
3. Problem of unequal storage time (t_s) eliminated.
4. "Switch-through" problem avoided.

Disadvantages:

1. Transistor repetitive peak voltages may exceed 750 volts at high line, limiting choice of devices having suitable switching speeds.
2. Short duty factor (<.5) mandates a higher value energy-storage choke than that needed for a push-pull circuit.
3. Transformer requires a bifilar tertiary winding for commutation of magnetizing energy.
4. Primary leakage inductance of the transformer cannot be commutated so must be snubbed.
5. Because a single forward converter is a half-wave system, the peak current on the transistor is twice what it would be in a full-wave circuit of similar power.
6. Total duty factor (D) of power switch must not exceed 50%.

Fundamental to all switching supplies is the requirement of load-to-line isolation. The method by which this isolation is accomplished affects the subsequent design of the base drive system and whether it will be transformer or direct coupled.

The low saturation resistance of the type 2N6751 ($V_{CE(sat)}$ typically less than 0.5 V at $I_C=5$ A, $I_B=1$ A) permits the effective use of the Baker (antisaturation) clamp technique to reduce the storage time of the power switch. A two-diode-drop level shift is sufficient to put the transistor into the active region, thus reducing the worst-case, high-temperature

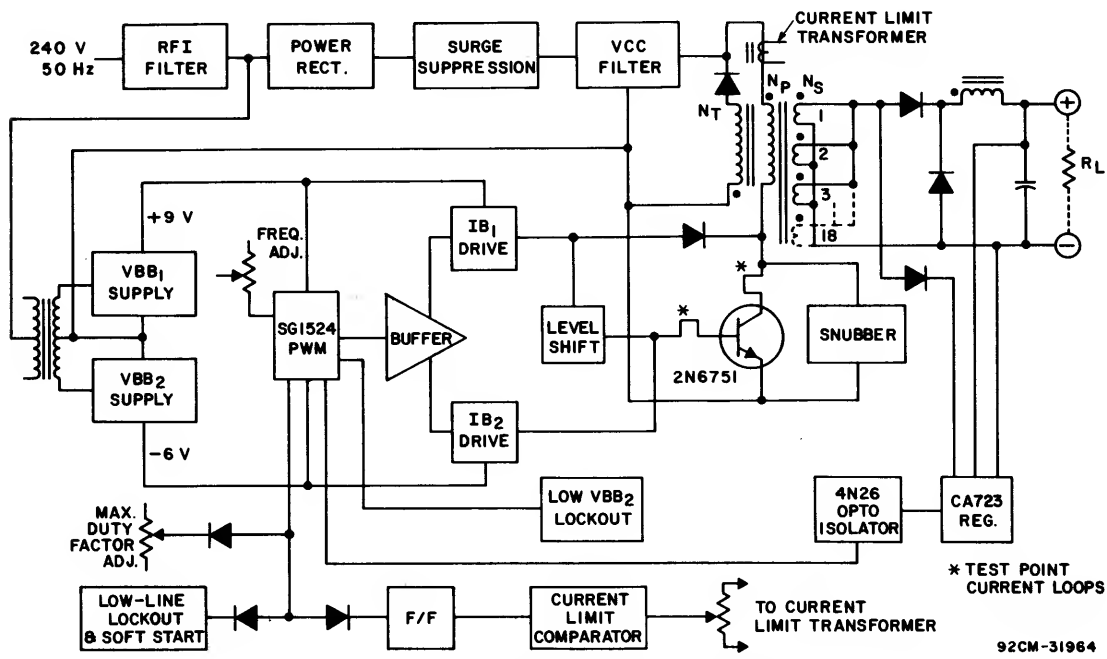


Fig. 169 - Block diagram of the converter.

storage time to less than 1.5 microseconds and lowering the fall time to 50 to 70% of its saturated switching-speed value.

Dead Time

Since the forward converter is a single-ended design, the simultaneous conduction problem that can occur with push-pull, half-bridge or bridge circuit formats does not exist. However, the total duty factor must not exceed 50%. Violation of this constraint will result in eventual transformer saturation and system failure. The need for the provision of a brief and controlled storage time becomes apparent. This storage time, together with a setting of the maximum duty factor control on the pulse-width modulator for D=0.4, provides a worst-case on time, including a 1.5-microsecond t_s , of about 11.5 microseconds with a 1-microsecond safety margin.

Transformer Limitations

One of the limitations of the forward converter is the portion of the on time (DT) consumed by the current rise time in the switching transistor and dominated by the referred leakage inductance of the transformer secondary. This limitation restricts the energy per cycle that can be transferred to the load side of the system at low line. The inductance

of concern is that measured across the primary with the secondary shorted and the tertiary winding open (L_o). The power transfer is the product of the energy per cycle (W_c) times frequency (f).

$$W_c = \int_0^{DT} V_{CC} i_c dt$$

where:

$$D = \text{duty factor, } T = \frac{1}{f}$$

$$i_c = I_{c(max)} \left(1 - e^{-\frac{t}{\tau}} \right)$$

$$\tau = \frac{L_o}{R_L} = \frac{\text{secondary leakage inductance referred to primary at } V_{CC}(\text{low line})}{I_{c(max)}}.$$

Combining the above yields:

$$P_{transfer} = f \times V_{CC}(\text{min})$$

$$\times I_{c(max)} \int_0^{DT} \left(1 - e^{-\frac{R_L t}{L_o}} \right) dt$$

If $DT > 3\tau$ (which it must be for efficient operation) the equation integrates to $P_{transfer} = 1/T \times V_{CC}(\text{min}) \times I_{c(max)}$

$$\times \left(DT - \frac{L_o}{R_L} \right).$$

Inserting into the simplified equation the values of $V_{CC}(\text{low line})=240$ volts

$$I_C(\text{max})=5 \text{ A}$$

$$D \times T=11.5 \mu\text{s}$$

$$R_L=V_C/I_C=48 \text{ ohms}$$

$$L_o \text{ typical}=40 \mu\text{H}$$

The value of P_{transfer} would be:

$$P_{\text{transfer}}=1/25 \times 240 \times 5 \times (11.5-40/48)=512 \text{ watts}$$

The value of L_o in the final transformer design was 16 microhenries. Reevaluating the equation with this value yields $P_{\text{transfer}}=536$ watts, a substantial improvement. The reader can anticipate the effect on power transfer of increasing the operating frequency to 80 kHz, for example.

Snubbing and Turn-Off Dissipation

To restrain voltage overshoots on the power switching device at turn-off, it is necessary to add capacitance between the collector and emitter to absorb the energy of the uncommutated leakage inductance of the primary (L_{p1}).

Current Limiting

To protect the power switching transistor from the load faults that may occur at the output of a power supply, collector current limiting is essential. To be effective, the delay time through the entire current control loop must be minimal and the base drive must keep its integrity to pulse widths narrower than those necessary for normal voltage regulation.

Antisaturation clamping relieves the worst part of the forward-loop delay problem by holding the power-device storage time (t_s) to less than 1.5 microseconds.

Overcurrent may be sensed by using a current-sensing toroid on the primary lead of the power transformer. This technique has several benefits:

1. The toroid is so located that it senses only the referred secondary currents and ignores the excess base-current contribution.
2. The comparator circuit is isolated from the high voltages and high currents that may occur with a power-switching failure.

As previously mentioned, the forward-converter circuit places very high repetitive peak voltages (in excess of 700 volts) on the switching transistor, clamp diode, snubber, capacitor, and transformer windings. Should power requirements be such as to require the paralleling of forward-converter circuits, a

half-bridge circuit might be more economical and produce lower stresses with a wider choice of transistors.

900-WATT, OFF-THE-LINE, HALF-BRIDGE CONVERTER

The performance of two RCA-2N6678 'SwitchMax' high-speed power transistors (15 A, 450 V (V_{CEX})) is demonstrated in the following 900-watt, half-bridge converter.

The circuit switches at a 20-kilohertz rate and with minimal alterations can operate from either 120 or 240 volts. It was built using conventional circuitry but in a non-compact modular format so that it would be easily accessible for instrumentation connections and component or design alteration. The power switches used are the RCA-2N6678 'SwitchMax' 15-ampere [$I_{CE}(\text{sat})$], 450-volt (V_{CEX}) high-speed transistors.

Because the purpose of this effort was not to develop an optimum design but to permit experimentation with and analysis of high-speed transistor switching operation, a 10-volt/100-ampere output capability was selected rather than the more common 5-volt/200-ampere range. This choice permitted the use of simple magnetic components and fast-recovery rectifiers, rather than Schottky devices, without the hazard of rectifier damage in the event of lost regulation. It also permitted easier dummy-load manipulation.

The half-bridge circuit was chosen because of the following advantages:

1. Requires a simple transformer primary having a single winding.
2. System leakage inductance is commutable, allowing minimum snubber design and lower dissipation.
3. Adaptable to either 120- or 240-volt operation.
4. Permits easy maintenance of B-H symmetry in transformer core without exotic circuits or excessive air gaps.
5. Modulation and drive circuits are easily protected from the consequences of a power stage failure.
6. Needs only two 2N6678 'SwitchMax' transistors for almost a kilowatt of output.

The disadvantages encountered with the selection of the half-bridge circuit include:

1. Difficulties in making voltage versus current measurements because the primary section has no identifiable ground plane.
2. Difficulty in providing solid turn-off drive

- power at short duty factors.
3. Tendency to cross-switch at high power levels because of large displacement currents in the device mica-heat sink region and sharp $L \, di/dt$ voltages.
- These disadvantages, however, were found to be manageable.

System Configuration

A block diagram of a half-bridge converter is shown in Fig. 170. The system is made up of three major building blocks:

- I. **Power Block.** This block encompasses the 60-Hz power rectifiers, filters, power switching devices, commutating diodes and snubbers, 20-kilohertz 8-to-1 step-down transformer, rectifier, and filter elements.
- II. **Oscillator-Modulator Block.** This block comprises the oscillator for the pulse-width modulator, modulator IC, soft-start, low-line lock-out comparator, pulse-by-pulse current limiter, and the predriver IC's.
- III. **Base Driver Block.** This block provides on and off drive to the power switches.

System Performance

The over-all performance of the 900-watt half-bridge rectifier system is given in Table X. The line and load regulation figures though

Table X - Performance of 900-Watt Converter System

| |
|--|
| Output Voltage (nominal)— $V_o=10$ volts |
| Output Current (nominal)— $I_o=90$ amperes |
| Line Regulation at $V_o=10$ V, $I_o=50$ A, $V_{LINE}=120$ rms: -0.7% at $V_{LINE}=105$ V rms +0.5% at $V_{LINE}=135$ V rms |
| Load Regulation at $V_o=10$ V, $I_o=50$ A, $V_{LINE}=110$ V rms: +1% at 10 A to -0.6% at 80 A Current limit at 90 A |
| Hum (see Fig. 171) at 120 Hz=100 mV peak to peak |
| Ripple (See Fig. 172) at 20 kHz=50 mV peak to peak |
| RF Noise (see Fig. 172) at 5 MHz=0.5 V peak to peak |
| Efficiency=69 to 73% (conventional watt-meter readings) |

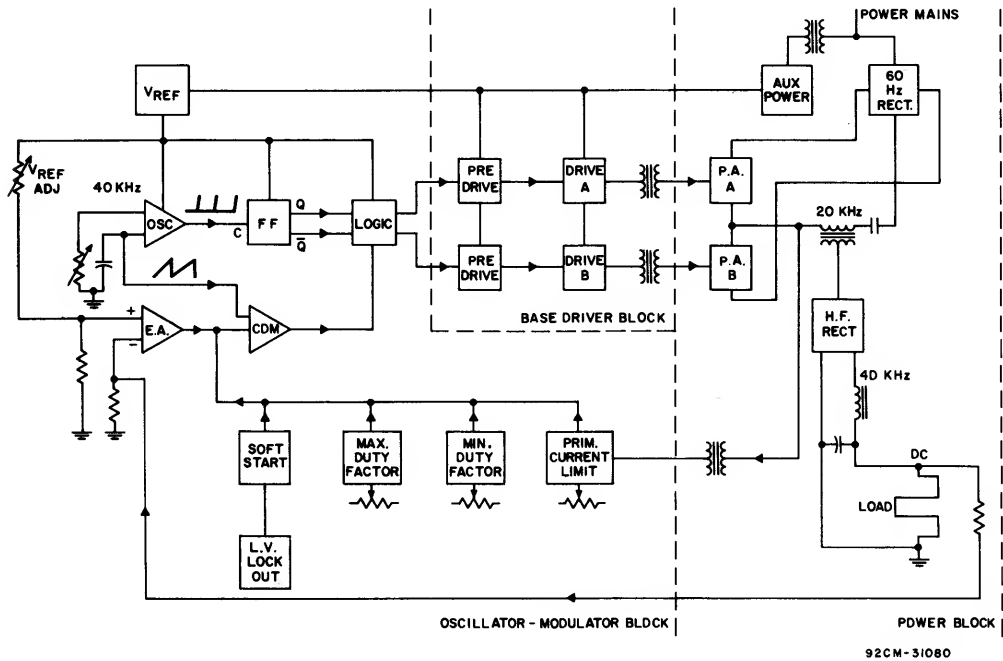


Fig. 170 - Block diagram of half-bridge driven converter. Note the three major sections: Power Block, Oscillator-Modulator Block, and Base Driver Block.

satisfactory are not outstanding and could be improved by a higher dc open-loop gain. Such improvement, however, is not likely in the present configuration.

The hum performance, less than 100 millivolts on a 10-volt output, is respectable (see Fig. 171) and is comparable to the accepted industry standard of 50 millivolts on a 5-volt output. Some additional design effort on the error amplifier and a less conservative roll-off characteristic could bring about a two to one improvement.



Fig. 171 - Hum performance of 900-watt converter system.

As shown in Fig. 172, the ripple at 20 kilohertz is also low, less than 50 millivolts peak to peak on a 10-volt output. High-frequency ripple is almost entirely dependent on the quality of the final filter capacitor (C13 in Fig. 173).

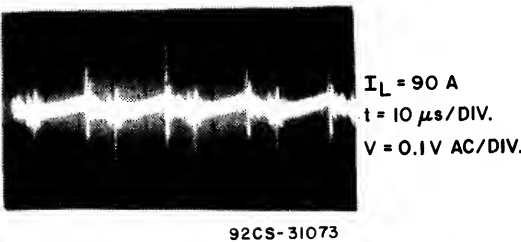


Fig. 172 - Ripple performance of 900-watt converter system. Note rf noise during rectifier transitions.

The elimination of rf noise presents a major problem. The noise, see Fig. 172, is caused by the transition of the high-current rectifiers and is extremely difficult to filter or shield. The appearance of this noise in a magnified oscilloscope display is that of several different high-frequency damped oscillations excited by the same voltage or current shock. This problem is further complicated by the confusion of grounding systems between the isotransformer, and associated instrumentation, as well as the radio-frequency inter-

ference radiating from the long leads of the breadboard system.

The efficiency of the supply, depending on load and based on conventional wattmeter readings, is 69 to 73 per cent. A 100-watt discrepancy, however, was noted between the wattmeter measurements and the total of the subsystem calculated losses. A summary of the calculated losses at the 900-watt level with 120-volt line is given in Table XI. The total power loss is 251 watts and the calculated efficiency, therefore, is a more reasonable 78 per cent. Determination of true efficiency would require the use of a 300-volt dc supply in place of the 60-Hz mains, rectifier, and ac wattmeter.

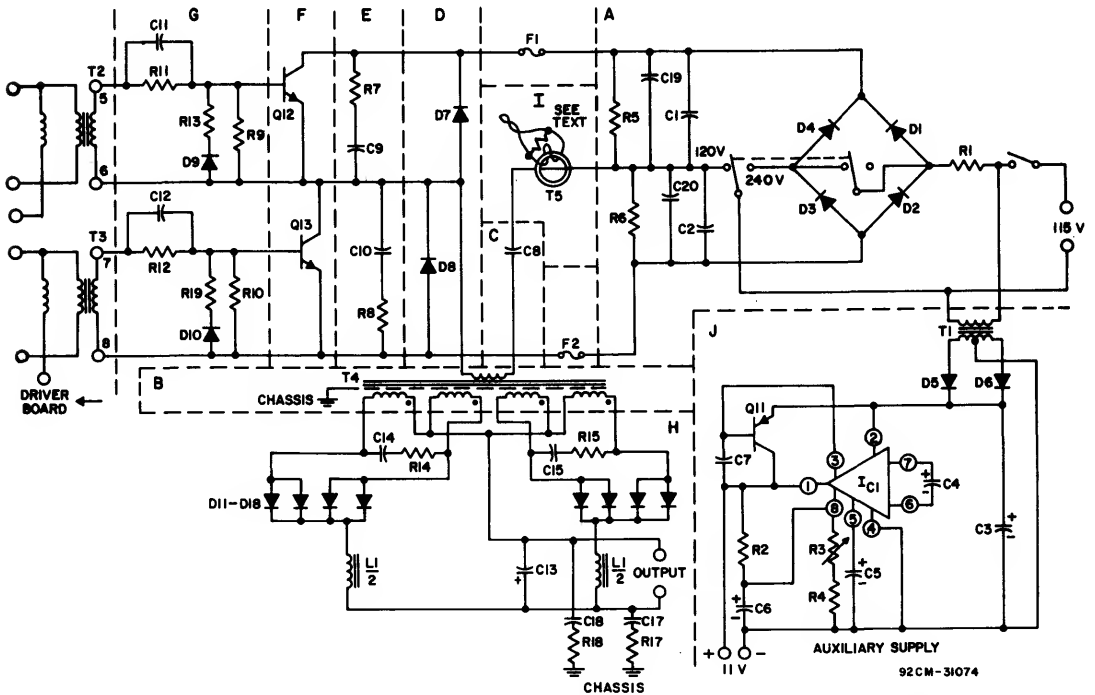
Table XI - Power Losses Calculated by Subsystem

| Subsystem | Power Loss (W) |
|---|----------------|
| Auxiliary Supply Pass Regulator | 20 |
| Base Driver System | 25 |
| Power Switches | 50 |
| Output Rectifier | 100 |
| High-Frequency Transformer | 10 |
| 60-Hz Rectifier | 10 |
| Snubbers | 10 |
| Output Chokes | 6 |
| 60-Hz Bleeder Resistors | 20 |
| Total | 251 |
| Calculated efficiency=251/(251+900)=78% | |

Power Block Operation Analysis

The schematic diagram and parts list for the power-block portion of the 900-watt half-wave bridge converter are given in Fig. 173. For discussion purposes, this block is divided into ten sections:

- A. 60-Hz Rectifier and Filter
 - B. High-Frequency Power Transformer
 - C. Coupling Capacitor
 - D. Commutating Diodes
 - E. Snubber Network
 - F. Power Switches
 - G. Base-Input Networks
 - H. Output Rectifiers and LC Filter
 - I. Current-Sense Transformer
 - J. Auxiliary Power Supply
- A. **60-Hz Rectifier and Filter.** This section, which could also operate on 50 Hz, is conventional. It provides the option of switch-



- C1,C2** =4500 pF, 250 V, electrolytic
C3 =1100 μ F, 25 V, electrolytic
C4 =100 pF, ceramic
C5 =2 μ F, 25 V, electrolytic
C6 =10 μ F, 25 V, electrolytic
C7 =0.05 μ F, 100 V, ceramic or paper
C8 =4 capacitors in parallel, each 2 μ F, 200 V, paper
C9,C10 =3 capacitors in parallel, each 0.001 pF, 600 V, Mylar or metal film
C11,C12 =0.68 μ F, 200 V, Mylar or metal film
C13 =6 capacitors in parallel, each 1600 μ F, 50 V, low ESR electrolytics (Sangamo 301JP162 U050B or equivalent)
C14,C15 =0.01 μ F, 1 kV, ceramic
C17,C18 =0.005 μ F, 1 kV, ceramic
C19,C20 =0.5 μ F, 600 V, paper or Mylar

- D1,D2**
D3,D4 =20 A/300 V, DO5 rectifier, 1N1195A or equivalent
D5,D6 =6 A/50 V, DO4 rectifier, 1N1341B or equivalent
D7,D8 =18 A/600 V, fast-recovery rectifier, D2412M or equivalent
D9,D10 =1 A, fast-recovery diode, 1N4933 or equivalent
D11 through D18 =fast-recovery diode, 1N3910 or equivalent
F1,F2 =8 A/250 V fuse

- IC1** =CA3085, voltage rectifier
L1 =9 μ H, 2 18- μ H inductors in parallel
Q11 =2N6649, p-n-p Darlington, TO-3
Q12,Q13 =2N6678, power transistor
R1 =2.5 ohms (cold); 0.045 ohms (hot) Rodan surge guard SG-7
R2 =0.12 ohms, 2 W
R3 =10 kilohms, potentiometer
R4 =820 ohms, 1/2 W
R5,R8 =3500 ohms, 10 W, wire wound
R7,R8 =50 ohms, 12 W, made up of 6 300-ohm 2-W resistors in parallel
R9,R10 =4 ohms, 3 W, made up of 3 12-ohm 1-W resistors in parallel
R11,R12 =1.5 ohms, 10 W, non-inductive
R13,R19 =10 ohms, 2 W
R14,R15 =10 ohms, 1 W
R16 =1 ohm, 1/2 W
R17,R18 =20 ohms, 1/2 W
T1 =115 V, 28 V, 2 A, center tapped (Signal Transformer 241-7-28 or equivalent)
T4 =Cores — pair IR8113 "E", Indiana Secondaries — 4 each 3-1/2 turns of 0.020" x 0.75" copper strap Primary — wound on secondaries, 28 turns 6 strands of #21 enameled wire =1000 turns #32 wire on a pair of linear ferrite E cores about 3/8" x 3/8"; cross section non-critical. See text.
T5

Fig. 173 - Schematic diagram and parts list for Power Block portion of 900-watt converter.

ing from a bridge for 230-volt operation to a doubler for 115-volt operation. The capacitors and rectifiers are oversize to provide the extended range of operating conditions desired for this study. Minimal surge limiting is provided by a surge-limiting resistor having a negative temperature coefficient. A commercial power supply would require a sturdier arrangement plus an RFI filter.

B. High-Frequency Power Transformer. The high-frequency power transformer T4 uses a pair of Indiana General IR8113 E cores. The secondaries have four windings, each $3\frac{1}{2}$ turns of copper strap 0.75 inch wide by 0.020 inch thick. The $3\frac{1}{2}$ turns allow the common point for all windings to terminate on the same side of the bobbin for ease of connection to the negative bus. The primary is 28 turns of 6 strands of No. 21 enameled wire twisted two turns per inch and wound on top of the secondary. Three-mil Mylar drafting film provides the interlayer insulation. Each secondary winding has a $0.01\text{-}\mu\text{F}/10\text{-ohm}$ damper network across it at the rectifiers to reduce self-resonance ringing. A five-mil insulated copper-foil Faraday shield between the primary and secondary windings is grounded to the output common and chassis to reduce coupling between windings. The double secondary made of 0.75-inch strap was required by the core dimension to provide the copper cross section needed to keep I^2R losses below nine watts.

C. Coupling Capacitor. The power transformer coupling capacitor C8 is designed to preserve the B-H symmetry in the half-bridge circuit. However closely components are matched to preserve drive symmetry to the switching transistors, differences in heat sinking, the switching temperature coefficient, transient load changes, or unsymmetrical rectification can cause offset of the transformer-core B-H curve. As a result, the transformer may draw abnormal current on one half of its cycle and, in turn, charge the coupling capacitor to a higher voltage than normal. When the cycle reverses, the higher capacitor voltage adds to the $V_{CC}/2$ being applied to the other switch, thus providing extra voltage across the transformer winding in such a direction as to recenter the B-H characteristic.

Selection of the proper value for this capacitor requires some analysis. The lower limit of the capacitor value can be determined by recognizing a series resonant circuit formed

by the capacitor and the referred value of the filter choke $L = (N_P/N_S)^2 L_F$. The resonant frequency must be less than half of the switching frequency and for charging to be linear it should be less than one fourth of it. The circuit of Fig. 173 uses a filter inductance of 9 microhenries (two 18 microhenry chokes in parallel) and a switching frequency of 20 kilohertz. Allowing for a high dc current and temperature, the effective value of the inductance is estimated as 6 microhenries. With this value for L_F and a resonant frequency of 5 kilohertz, a value for the coupling capacitor C can be determined as follows:

$$f = \frac{1}{2\pi \sqrt{LC}} \quad L = (N_P/N_S)^2 L_F$$

$$C = \frac{1}{4\pi^2 f^2 (N_P/N_S)^2 L_F}$$

$$C = \frac{1}{4\pi^2 \times 25 \times 10^6 \times 8^2 \times 6 \times 10^{-8}}$$

$$= 2.6 \mu\text{F}$$

This value of $2.6 \mu\text{F}$ is a reasonable one.

The charging voltages on the coupling capacitor should be considered next. With an average current of 10 amperes for 20 microseconds, the capacitor would charge to a value given by:

$$V = \frac{I}{C} \times dt$$

$$V = \frac{10 \times 20 \times 10^{-6}}{2.6 \times 10^{-6}}$$

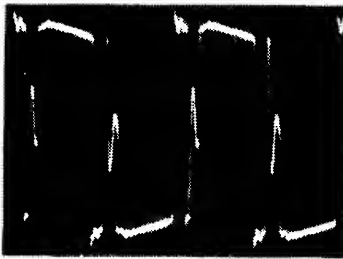
$$= 77 \text{ volts}$$

This value of 77 volts is excessive and would interfere with regulation at low line voltages. A more reasonable value would be 30 volts or 10 per cent of the nominal V_{CC} (20 per cent of $V_{CC}/2$). With this value for V

$$C = I \frac{dt}{dv} = \frac{10 \times 20 \times 10^{-6}}{30}$$

$$= 6.67 \mu\text{F}$$

Based on this calculation, a value of $8 \mu\text{F}$ was selected for the coupling capacitor C8. Although a voltage rating of 50 volts would be adequate theoretically, 200-volt units were used for safety purposes. To minimize heating, four $2\text{-}\mu\text{F}$ 200-volt paper capacitors in parallel were used. The effect of this capacitor is illustrated in Fig. 174, which shows the droop



92CS-31071

Fig. 174 - Waveform of transformer primary voltage. Note tilt in waveform caused by compensating effect of coupling capacitor.

in transformer voltage at high ampere-second products.

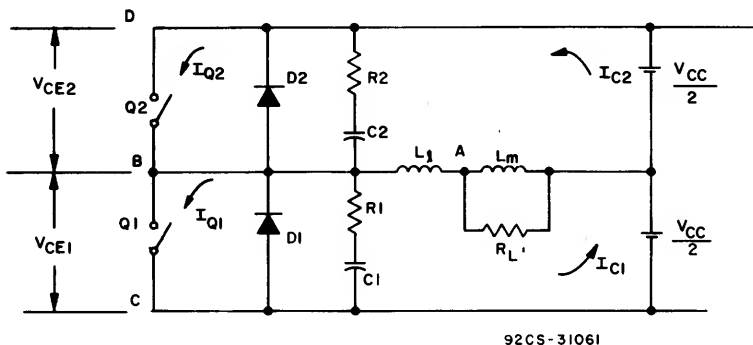
D. Commutating Diodes. The commutating diodes (D7 and D8) are standard, fast-recovery, 12-ampere, 450-volt rectifiers D2412M connected as close as possible to their companion transistor switches (Q12 and Q13). In a half-bridge circuit, the commutating diodes do more than steer leakage inductance energy back to the main supply. In the event of a sudden off-load, or a backfeed, the drastic increase in transformer flux can drive the collector of the conducting transistor negative with respect to its emitter, forcing the device into "inverse conduction". The commutating diode then bypasses the switch until the collector again goes positive, thus preventing a high-stress situation.

E. Snubber Network. The snubber network limits the $L_1 di/dt$ voltage excursion produced by the interruption of the current flow in the transformer and absorbs the energy in the leakage inductance. In contrast, the commutating diode does not absorb the inductive

energy, but transfers it back to the main power source. A feature of the half-bridge circuit is that most of the leakage and wiring inductance can be commutated. This feature allows the use of smaller, lower-dissipation snubbers than would be needed for forward or push-pull inverters of comparable power. Instead of absorbing the entire $L_1 I_p^2/2$ energy, the snubber needs only enough capacitance to hold the V_{CE} down to its limit value until the turn-on delay of the commutating diode is overcome. This turn-on delay is in the order of 50 to 100 nanoseconds depending on the diodes and wiring. The interplay between snubbers and commutating diodes can be clarified by a study of the simplified circuit of Fig. 175 and the corresponding waveforms in Fig. 176.

For additional information on Snubber Network Systems Design, refer to RCA Application Note AN-6743 "A 900-Watt Off-the-Line Half-Bridge Converter."

F. Power Switching. The power switching devices, 2N6678, are from the RCA "Switch-Max" power transistor family. They have been specially designed for high inductive-switching-locus capability (clamped $E_{s/b}$) up to 450 volts at 15 amperes and with a load inductance of 50 microhenries. They also provide excellent switching-speed performance at high temperature as well as at room ambient. All devices in this family are tested for these parameters at both 100°C and at 25°C. The circuit designer, therefore, can safely use these transistors to the full extent of their capabilities with assurance that no critical limit will be exceeded. As a result, maximum efficiency and cost effectiveness can be achieved in switching-circuit designs.



92CS-31061

Fig. 175 - Simplified diagram of snubber network system.

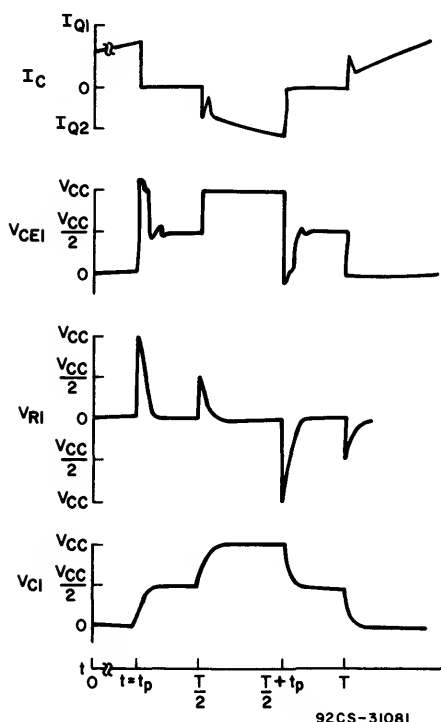


Fig. 176 - Waveforms in snubber network.

G. Base-Input Network. The base-input network conforms to standard practice with a 1.5-ohm current-limiting resistor and 0.68- μ F speed-up capacitor to sharpen the base-current rise time and enhance the I_{B2} , V_{BB2} turn-off drive. A 4-ohm resistor is connected from base to emitter of each switching device to minimize the cross-switching problem previously mentioned.

H. Output-Rectifiers and LC Filter. The output rectifiers (D11-D18) are conventional 1N3910 fast-recovery types wired and mounted on heat sinks with their companion chokes. The chokes use Indiana General SR15002-1-245 pregapped E cores wound with 9 turns each of 0.75-by-0.020-inch copper strap giving a nominal inductance of 20 microhenries per choke. The strap ends were left long to facilitate low-ohmic connections to the rectifiers and filter capacitors. The double filter chokes were used because the standard pregapped cores available were rated at only 50 amperes at the inductance selected. The chokes were designed for a minimum load current of 10 amperes.

The filter capacitor bank C13 consisted of

six Sangamo 1600-pF/50-V tubular single-ended electrolytics (Cat.#301JP162U050B). This capacitor bank effectively keeps the 20-kilohertz ripple to less than 50 millivolts at all loads from 10 to 90 amperes. Calculations show that a capacitance of only 8000 μ F is needed for good ripple control but a total of 9600 μ F was used to be conservative. For stability tests, an additional 30,000 μ F of capacitance was added to approximate worst-case loading.

I. Current-Sensing Transformer. The current-sensing transformer is placed on the primary side of the power transformer so that it will be responsive to core saturation as well as provide fast response to load faults. The secondary of the current-sensing transformer (T5) is 1000 turns of No. 32 wire on a pair of ferrite E cores having a $\frac{3}{8}$ " by $\frac{3}{8}$ " center leg. The primary is one turn of the wire to the power transformer wrapped over the secondary. Terminated with 1100 ohms, T5 produces a faithful waveshape of about 1 volt/ampere.

J. Auxiliary Power Supply. This supply powers the pulse-width modulator and base drive circuits. It is a basic transformer, rectifier, series-pass regulator system. The only critical component is the high-quality transformer (T1) needed for the line-voltage range over which the inverter must work, 95 to 135 volts RMS. Economy transformers tend to overheat at high line conditions and cause regulation problems at low line.

Oscillator-Modulator Block Operation Analysis

The circuit diagram of the complete Oscillator-Modulator Block is given in Fig. 177. This block uses the pulse-width modulator integrated circuit type 1524 combining on one chip a reference voltage source, a clock oscillator and ramp generator, a toggling flip-flop, separate A and B output buffers, an error operational amplifier, and a comparator. The shut-down clamp and the current-limit shut-down portions are not used in this application. Additional components provide the following functions.

1. Maximum Duty Factor Control—prevents common-mode conduction.
2. Minimum Duty Factor Control—prevents double pulsing in case of a sudden off-load, line surge, or back feed, and assures proper snubbing action.

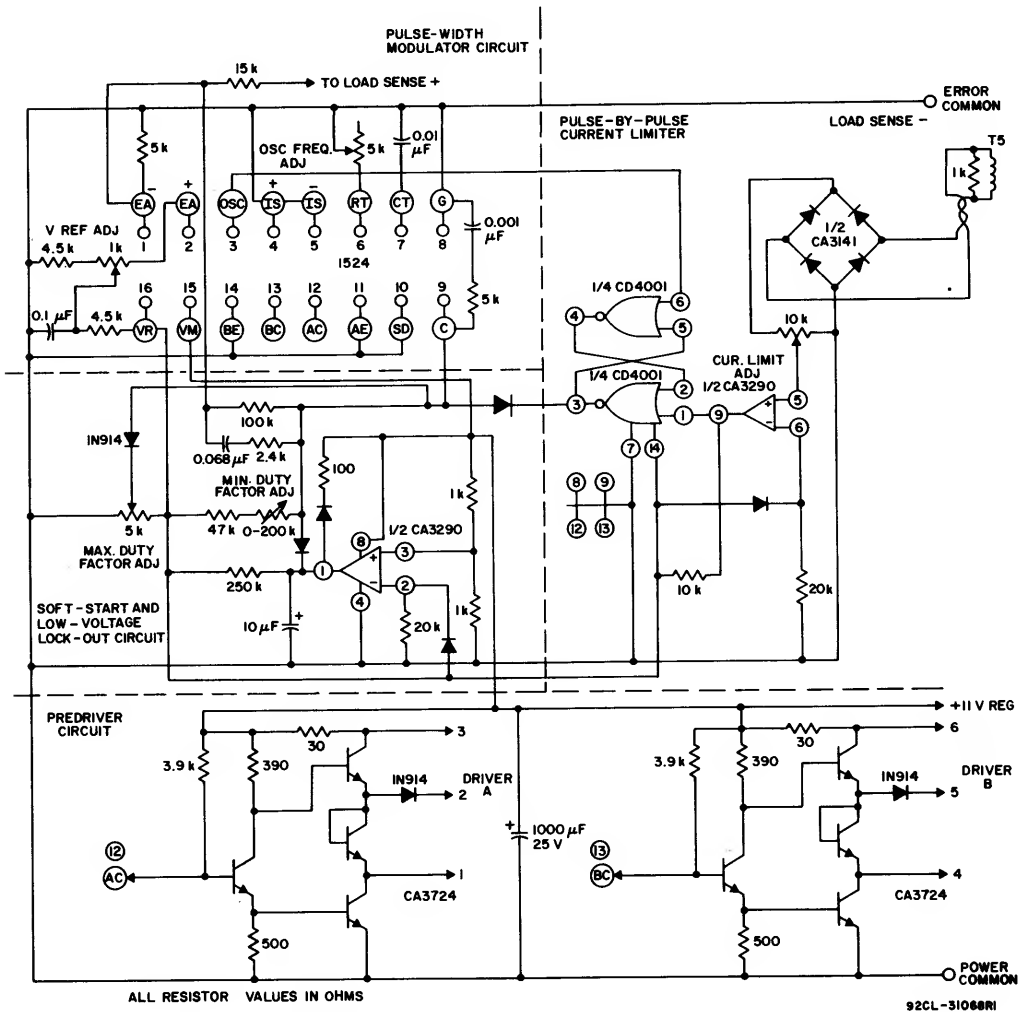


Fig. 177 - Schematic diagram of Oscillator-Modulator Block.

3. Soft Start—with a fast reset, limits surge currents.
4. Low-Line Lock-Out—truncates the duty factor whenever the power line voltage drops below 100 volts RMS and shuts down the supply entirely at 85 volts.
5. Pulse-by-Pulse Current Limiter—terminates the drive pulse in the event of overload or core saturation.

Pulse-Width Modulator Circuit. The operation of the pulse-width modulator circuit is conventional except for the following:

1. Because the current-limiting and shut-down facilities are not used, terminals 4, 5, and 10 are tied to common pin 8.
2. To maintain a minimum duty factor, a positive current is forced into the error

amplifier-comparator control rail from the voltage reference source through the 47-kilohm and 200-kilohm adjustable resistor. This current prevents the high-impedance error amplifier from driving the control rail all the way to zero and provides a minimum 2.5-microsecond width for the adjustable pulse to assure that if there is a sudden off-load, back feed, or power-line surge, the switching devices continue to alternate their switching action until the output voltage regulates downward, thus preventing the problem called "double pulsing."

Soft-Start and Low-Voltage-Lock-Out Circuit. For the safe operation of the pulse-width modulator supply-voltage circuits, the

drive circuits and the main power load must be sequenced on and off in the proper order as the power supply is turned on or off across the power mains. If not, severe stresses are placed on the switching transistors and can lead to device failure.

An effective way to provide these capabilities is to use a "soft-start" circuit having a fast reset and a low-voltage lockout provision. "Soft start" refers to the application of the base drive pulse to the switching transistors. It starts with a minimum pulse width but with full current and then slowly increases pulse width to its full controlled value. Such a circuit is shown in Fig. 178. This circuit

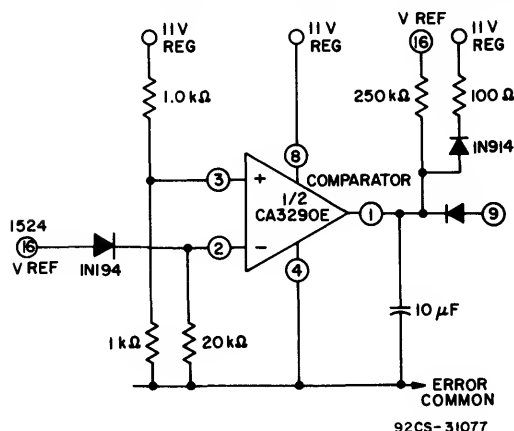


Fig. 178 - Soft-start low-voltage lock-out circuit.

assures that base-drive power is applied to the power switches only after the auxiliary power is up to its full regulated value (in this case 11 volts) and then, in a soft-start fashion, it minimizes start-up current surges. Conversely when power is removed from the system, either accidentally, deliberately, or because of brown-out conditions, the low-voltage lock-out truncates the duty factor over the range of 100 to 75 volts without lowering the base-drive current. Upon recovery of the main voltage, the soft-start circuit again takes control.

The soft-start low-voltage lock-out circuit operates as follows.

1. Upon application of power, the voltage at the 11-volt auxiliary regulator output increases and applies power to the 1524 pulse-width modulator circuit, producing a reference voltage of 5.2 volts at its pin 16. (See Fig. 177). This reference voltage

is applied through a 1N914 coupling diode to the negative input, pin 2, of the CA3290 comparator and through a 250-kilohm resistor to the 10-microfarad soft-start capacitor. This capacitor is held low, thus holding the control bus, pin 9 of the 1524, low also.

2. The regulator auxiliary supply voltage connects through a voltage divider to the positive input, pin 3, of the CA3290 comparator.
3. When the voltage on comparator pin 3 exceeds that on pin 2, the output, pin 1, goes high and the 10-microfarad capacitor charges through the 250-kilohm resistor and allows the voltage on pin 9 of the 1524, to rise to that value called for by the error amplifier or the maximum duty factor control.
4. If the auxiliary voltage falls below its limit, the comparator goes low, draining the 10-microfarad capacitor and pulling down the control bus voltage, truncating the duty factor pulse, and finally shutting off the drive voltage. This circuit also has the effect of "degaussing" the power transformer during system turn-off.
5. When the equipment is switched off under normal conditions, the 100-ohm resistor and the diode quickly discharge the capacitor to reset it for the next turn-on.

Pulse-by-Pulse Current Limiter

The major hazards in the life of a power converter are core saturation and overload, both of which are heralded by excessive collector currents. Because the user cannot be expected to count every ampere of load on the output terminals, a current sensor placed in the primary side of the power transformer can recognize core saturation as well as provide fast response to load faults. Fig. 179 gives the schematic for the current-sensing technique used in this converter. The current-sensing transformer (T_5) was described as part of the Power Block. Its output waveform is shown in Fig. 180.

Base-Driver Block Operation Analysis

The Base-Driver Block provides the on and off drive to the power switches. It gets its input from the Oscillator-Modulator Block. A schematic of the drive system is given in Fig. 181. The pre-driver portion of the oscillator-modulator block is a conventional circuit and is also included in Fig. 181.

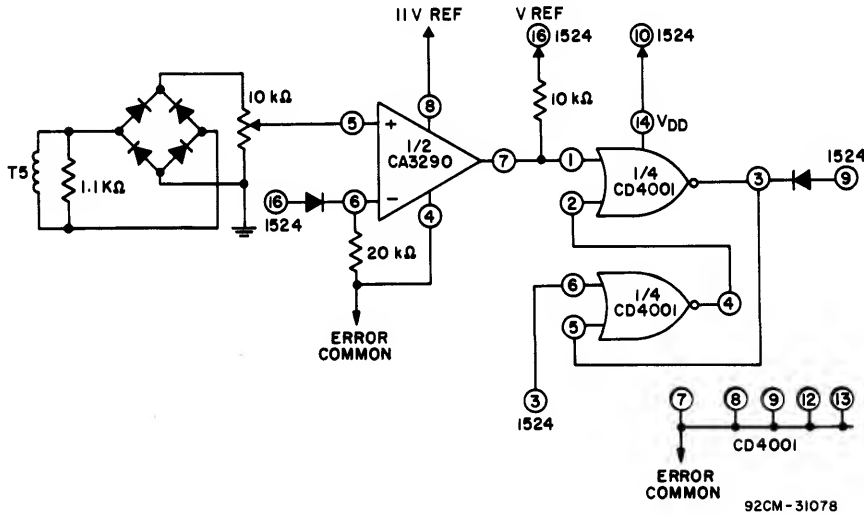


Fig. 179 - Pulse-by-pulse current-limiter circuit.



Fig. 180 - Waveform of current-sense transformer output voltage.

PERFORMANCE CONSIDERATIONS

Feedback Loop

Rigorous design requires that open-loop gain and phase-shift calculations be made to ascertain that the open-loop gain is reduced to unity (0 dB) before the 360-degree total phase shift is reached. The total open-loop gain is made up of five increments, as shown in Fig. 182. These increments are:

- G_S = gain of the sensing circuit
 G_A = gain of the error amplifier
 G_P = gain of the pulse-width modulator
 and the power switch combination
 G_T = gain of the high-frequency power
 transformer
 G_F = gain of the filter network

The summing of $G_S + G_A + G_P + G_T + G_F$ and their related phase shifts shows the system to be stable but not optimized for best hum suppression.

The mechanics of phase-gain calculations

and the techniques of equipment measurements are well-documented in the current literature. Experience with this converter and similar projects indicates that the best reasonable calculations give only crude estimates and actual measurements of operating gain and the phase relations are essential for optimal design.

Power Losses in Power-Switching Transistors

The most essential element of power loss is the power dissipation during the fall time of the driver pulse. This dissipation ranges from $(V_{CE(max)} \times I_C \times t_f \times F)/6$ for the pure resistive and oversnubbed case to $V_{CE(max)} \times I_C(max) \times t_c \times f \times 0.4$ for the clamped inductive case. These dissipations span almost a three-to-one range. In operating equipment, both equations and anything in between are correct at one time or another. The reason is that if a simple RC snubber network is made from calculations based on the previously discussed criteria, it will be made for the highest collector current for which the equipment is designed. For lower currents, consequently, the equipment is oversnubbed. In other words, a voltage-current locus that is inductive at 13 or 15 amperes will be resistive at 3 to 4 amperes, if snubbing is properly in place. This transition from capacitive-to-resistive-to-inductive turn-off locus with change in output load is shown in Fig. 183.

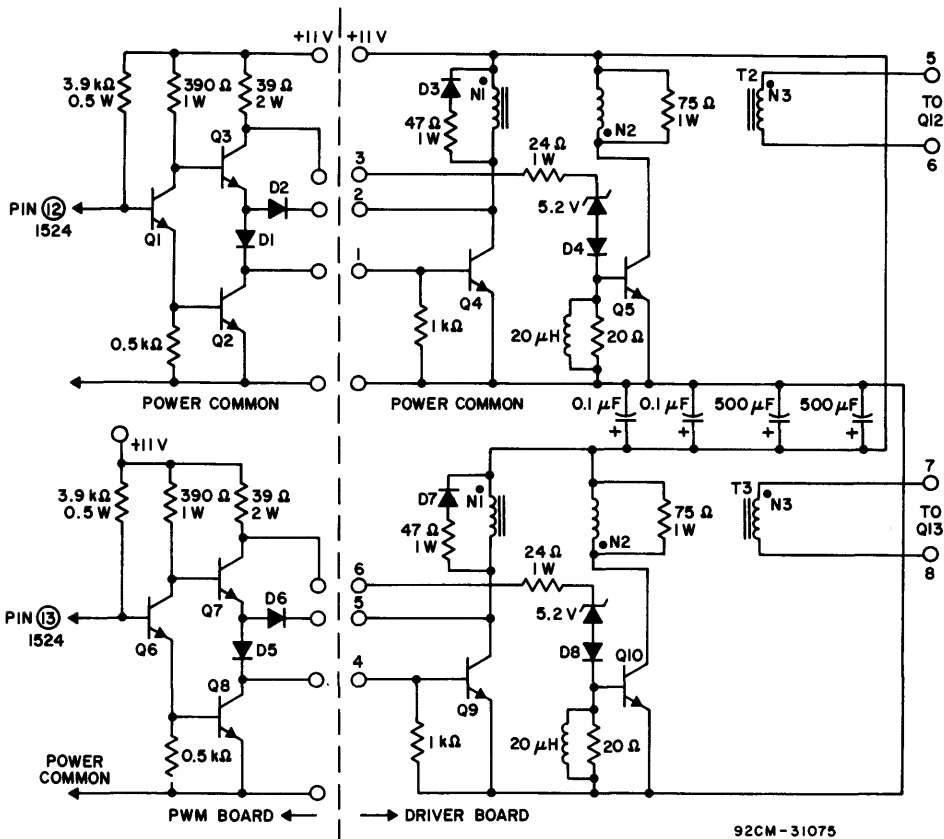
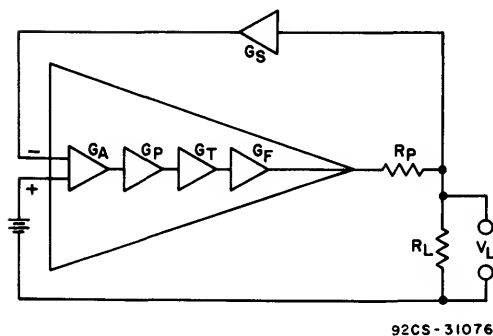


Fig. 181 - Schematic of Base-Driver Block. Includes predriver stage on pulse-width-modulator of Oscillator-Modulator Block.



$$V_L = A(V_R - V_L G_s) - I_L R_P$$
$$= A V_R - A V_L G_s - I_L R_P$$

$$A = \frac{I_L R_P}{V_R}$$
$$\frac{V_L}{V_R} = \frac{A}{1 + A G_s}$$

where A = Vector system forward gain

$$= G_A + G_P + G_T + G_F$$

G_s = Vector gain of feedback network

R_P = Parasitic resistance of rectifier's wiring

V_R = Reference voltage

Fig. 182 - Feedback components in converter.

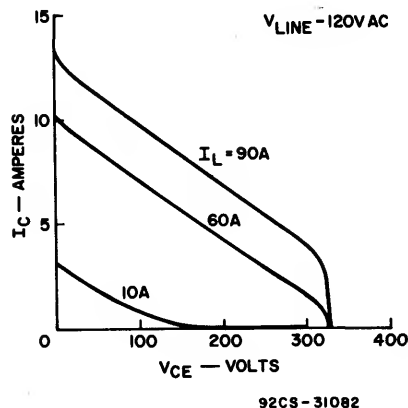


Fig. 183 - Collector current-voltage switching locus with change in output load.

Thermal Considerations

Because the converter was not intended as a commercial design the heatsinking is far from optimum. On each power transistor, a standard $1.8^\circ C$ per watt heatsink is used to which its companion commutating diode is also mounted. At full load they reach a case temperature of about 60 to $70^\circ C$. The base-drive transistors are each mounted on small heatsinks of about three square inches on their circuit card. The eight output rectifiers are mounted on two $1.8^\circ C$ per watt heatsinks (four on each) which get quite warm in operation. No forced ventilation is used.

The snubber network resistors reach about $70^\circ C$ in operation. This dissipation burden, however, can be better distributed by partial snubbing at the transformer instead of doing the entire job at the transistor terminals. The heatsinking of the snubber networks was improved by soldering the leads of the six parallel 2-watt resistors to punched 10-mil copper straps connected at their tops to the cathode of their respective commutating diodes.

The auxiliary-supply pass transistor and rectifier diodes mount on a fifth $1.8^\circ C$ per watt heat sink and are only comfortably warm.

Overload and Short-Circuit Protection

Overload and short-circuit protection are provided by the combined functions of soft start, low-line lock-out, pulse-by-pulse current limiting, and the capacitor-coupled transformer. With the system described, no failures were experienced as the result of turn-on at

full load, stepped-load charge, load pull, shorted filter chokes, or turn-off with full load. A direct short was not tried.

1-KW, 20-KHZ, OFF-LINE DRIVEN CONVERTER

Driven converters offer certain advantages over free-running converter systems which depend on the magnetic properties of a transformer to control switching. The main advantages are: 1) stable operating frequency independent of load (the degree of stability is dependent on the clock circuit chosen); 2) a simplified transformer design because feedback windings are not required; and 3), lower cost of the ferrite material employed (the cost of linear ferrite cores is often less than half that of square-loop cores of comparable size). One major disadvantage of this converter-circuit approach, however, is a tendency for common-mode conduction. Common-mode conduction refers to a mode of circuit operation during which both devices of a push-pull pair conduct simultaneously. During this period, the net flux density within the transformer core is virtually nulled out, presenting, for all practical purposes, short-circuit load conditions to the transistors. Although the high currents which prevail during this mode tend to turn off the transistor which has completed its normal conduction period, the opposite device starting its on period experiences high voltage and high current at the same time. This could lead to second breakdown. Therefore, considerable care must be taken when designing the drive circuitry to prevent or at least minimize common-mode conduction during light- or no-load conditions.

The inverter employed for this application uses a small high-frequency output transformer to isolate the load from the ac line and from the system ground of the converter itself. Because of the high operating frequency of the inverter, low ripple dc can be obtained by using low-valued capacitor-filter components. To achieve the same low level of ripple, a linear power supply would require the use of a regulator circuit and a series pass transistor (or transistors) with high energy-handling capability.

Since the transistors in an inverter are operated in the switching mode, their required energy-handling capability is considerably less than those employed in a linear power supply of comparable power output.

The following paragraphs describe a 1-kilowatt driven converter that operates from a 117-volt ac line. The converter is designed to provide a dc output of 100 volts and deliver 1 kilowatt of continuous output power to the load with an overall system efficiency exceeding 85 percent. This performance is achieved through the use of type 40854 transistors selected from the 2N6250 power-transistor family.

The following discussion is limited to a review of the design and construction of the converter circuit only. In a complete system, overload sensing and some form of latching circuit must be added to protect the transistors and other vital components from an overload or short circuit at the output terminals.

CIRCUIT DESCRIPTION

The converter consists of four major sections as illustrated by the block diagram shown in Fig. 184. A complete schematic diagram of the converter circuit is shown in Fig. 185. All circuits are operated from a single high-voltage source and are stable over ac line-voltage variations between 105 and 130 volts. The oscillator, buffer, and driver circuits easily fit on a single 4½-inch by 5½-inch

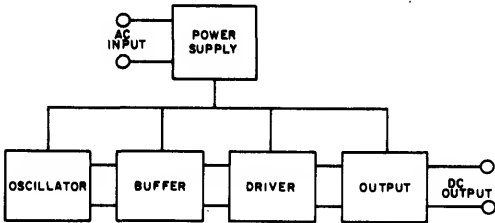
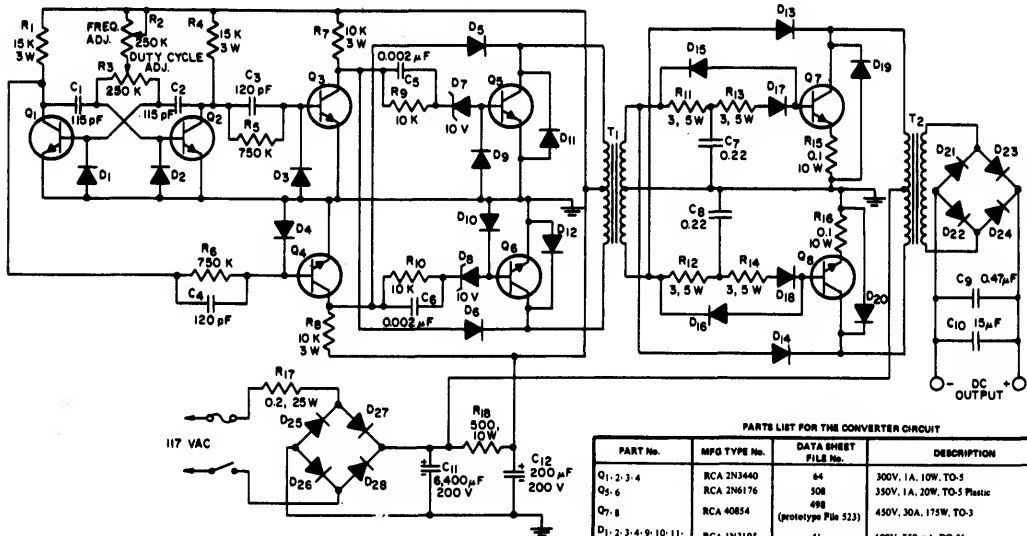


Fig. 184 - The four major converter sections.

circuit board. Additional filtering of the supply voltage for these stages keeps the ripple voltage below 500 millivolts during normal load conditions. Because all circuitry operates from a high dc potential, and because the speed-up capacitors employed in the base drive circuits for wave shaping charge up to this potential, diodes must be connected from base to ground of every transistor (with the exception of output transistors Q₇ and Q₈) to clamp the bases and prevent base-emitter junction breakdown during each transistor's respective off period. The effect of the clamping diode can be seen in the bottom waveform of Fig. 186.



| PARTS LIST FOR THE CONVERTER CIRCUIT | | | |
|--------------------------------------|--------------|---------------------|--|
| PART No. | MFG TYPE No. | DATA SHEET FILE No. | DESCRIPTION |
| Q1-2-3-4 | RCA 2N3440 | 64 | 300V, 1A, 10W, TO-5 |
| Q5-6 | RCA 2N6176 | 508 | 350V, 1A, 20W, TO-5 Plastic |
| Q7-8 | RCA 40854 | 498 | 450V, 30A, 175W, TO-3 |
| (prototype File 523) | | | |
| D1-2-3-4-9-10-11-12-19-20 | RCA 1N3195 | 41 | 600V, 750 mA, DO-26 |
| D5-6-13-14-15-16 | RCA TA7894 | * | 600V, 1A, DO-26, fast recovery rectifier |
| D7-8 | TRW 1N4740 | * | 10V, 1W, zener diode |
| D17-18 | RCA TA7900 | * | 600V, 3A, modified DO-4, fast recovery rectifier |
| D21-22-23-24 | RCA TA7985 | * | 300V, 40A, DO-5, fast recovery rectifier |
| D25-26-27-28 | RCA 1N1195A | 6 | 300V, 20A, DO-5 |

* - Supplemental data sheet

Fig. 185 - Complete schematic diagram of the converter circuit.

TOP: COLLECTOR
VOLTAGE OF Q₁ (V-50V/DIV,
H-10 μ s/DIV), BOTTOM: BASE
VOLTAGE OF Q₄ (V-1V/DIV,
H-10 μ s/DIV)



Fig. 186 - The effect of the clamping diodes and the wave shaping resulting from the presence of the buffer stage.

Oscillator

The clock signal is provided by a simple two-transistor (Q₁ and Q₂) multivibrator. The desired frequency of 20 kHz is stable to within ± 2 -percent drift with dc supply voltage varying between 125 and 175 volts. Trimmer resistors R₂ and R₃ are used to adjust the oscillator frequency and duty cycle. Resistor R₃ is included to eliminate the need for matching circuit components.

Buffer

A buffer stage (Q₃, Q₄) between the oscillator and driver circuits provides the isolation required by the oscillator for stable operation independent of the load. The wave shaping resulting from this stage is evident in the waveforms shown in Fig. 186. The top waveform is the collector voltage of Q₁ (or Q₂). The bottom waveform is the voltage present at the base of the respective drive transistor Q₅ (or Q₆).

Driver

Common-mode conduction in the push-pull driver stage is minimized by delaying the base drive to transistors Q₅ and Q₆. The desired delay is obtained through the use of cross-coupling diodes D₅ and D₆. These diodes prevent the base drive from reaching the non-conducting driver while the other is still in the conducting state. The base drive is held back until the V_{CE} of the conducting driver, during its transition to the off state, exceeds the breakdown voltage of the zener diode (D₇ or D₈) connected to the base of the non-conducting driver. This technique provides a delay that varies proportionately with the storage time of the devices in the sockets, and thus eliminates the need for matching transistors.

Output

The severity of common-mode conduction in the output stage is several orders of magnitude greater than that encountered in the driver stage if no steps are taken to delay the base drive. During the time when common-mode conduction occurs, the current flowing through each device is limited only by the transistor's gain and the impedance of the collector-emitter circuit. As these currents and their conduction times increase, the possibility of the occurrence of secondary breakdown also increases. Even if the safe-operating-area of the transistors is not exceeded, the resulting high volt-ampere pulses can substantially increase the power dissipation and affect the overall efficiency of the system.

The waveforms shown in Fig. 187 illustrate

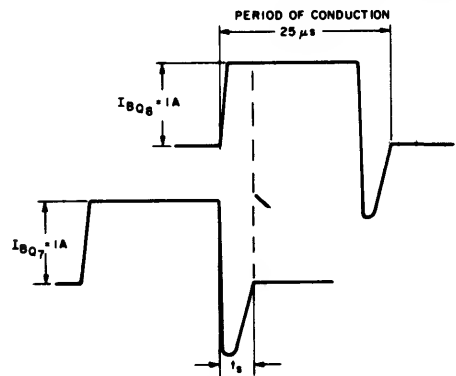


Fig. 187 - Form of base current to output transistors Q₇ and Q₈ without delay circuit.

what the base current to output transistors Q₇ and Q₈ would look like if no delay circuit were employed. If this drawing represented the actual operating condition of the output stage, common-mode conduction would occur during the storage time interval t_s . The amount of storage time is dependent on how hard the transistor is driven into saturation. Fig. 188 shows the reverse base-current waveform of one of the output devices under different load conditions with constant forward base drive. Comparison of the two waveforms shows almost a two to one increase in storage time when the converter is switched from a normal load state (1 kilowatt output) to an unloaded state.

A number of methods for obtaining the proper variable delay are available to the designer. The circuit approach shown in Fig.

REVERSE BASE
CURRENT WAVEFORM OF Q7
TOP: WITH 1KW LOAD
BOTTOM: WITH NO LOAD
V-1 AMP/DIV
H-0.5 μ S/DIV

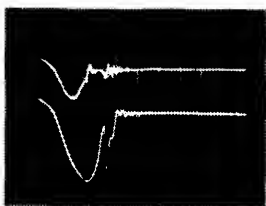


Fig. 188 - The reverse base-current waveform of one of the output devices under different load conditions with constant forward base drive.

185 has been chosen because it is economical; it requires a minimum of parts. The same design philosophy used in the driver stage has been applied to the output stage. Cross-coupling diodes D₁₃ and D₁₄ are used to shunt drive current through the conducting transistor during the needed delay period. When the conducting transistor turns off, its collector-to-emitter voltage rises to twice the supply voltage. As soon as this voltage increases beyond the base threshold voltage, the conducting shunt diode becomes back biased, turns off, and permits current flow to the base of the non-conducting output transistor. The base threshold voltage is determined by the series base diodes (D₁₇, D₁₈), the transistor base-emitter diode, and the voltage dropped across the emitter resistor (R₁₅, R₁₆). The end result is a base current pulse whose width varies according to the delay dictated by the load and the switching characteristics of the output transistors being used. For any given load and supply voltage, higher peak collector currents are required to maintain a constant average current if the forward drive portion of the base pulse width becomes narrower.

Therefore, it is highly desirable to keep the needed delay to a minimum. Diodes D₁₅ and D₁₆ minimize delay by providing a low-impedance base return to ground during the reverse-bias portion of each cycle. This low-impedance return reduces transistor-switching storage time.

Although the emitter resistors account for only a small part of the base threshold voltage (voltage drop results from collector-to-emitter leakage current), the degeneration they provide contributes to the reliability of the output stage by suppressing transient current spikes and enhancing the thermal stability of the device.

Transformer Design Considerations

A description of the transformers employed in the converter is given in Table XII. Because of the high operating frequency, ferrite was chosen as the core material for both transformers to minimize core losses. Each transformer is designed for non-saturated operation at core temperatures up to 100°C and supply voltages as high as 185 volts. The primaries of both transformers are bifilar wound to assure symmetrical coupling to the secondaries. The number of primary turns was determined through the use of the following formula:

$$N_p = \frac{2 V_{cc} \times 10^8}{4 f A_c B}$$

where V_{cc} is dc supply voltage, f is frequency, A_c is core cross-sectional area, and B is flux density.

Utilization of No. 12 wire (based on 800 to 1000 cir. mils/amp. rms) for the output transformer was found to be impractical. Not only was it extremely difficult to wind, but several layers were required to obtain the

Table XII - Ferrite Transformer Description

| Transformer | Primary | Secondary | Remarks |
|----------------|---|--|---|
| T ₁ | 300 turns C.T. bifilar AWG No. 30 | 10 turns C.T. bifilar AWG No. 22 | Ferroxcube pot core, No. 36/22, 3B7 |
| T ₂ | 60 turns C.T. bifilar AWG No. 18 | 20 turns bifilar AWG No. 16 | Allen Bradley C core, (4 pieces) No. U2625C133A, WO-3, paralleled sets of primary and secondary windings |

needed number of turns called for in the design. The parasitic winding capacitance and leakage inductance resulting from this poor physical design caused severe ringing and large voltage turn-off spikes at the collectors of Q₇ and Q₈. The ringing and voltage spikes were reduced considerably by paralleling duplicate pairs of the primary and the secondary windings from each set of C cores. This arrangement permitted the use of smaller-gauge wire to reduce the total number of layers and to get the windings closer to the core for better coupling. As a result, the transformer efficiency was improved, and a corresponding decrease in its operating temperature was obtained.

Performance Characteristics

The output performance characteristics of the converter are shown in Fig. 189. Fig.

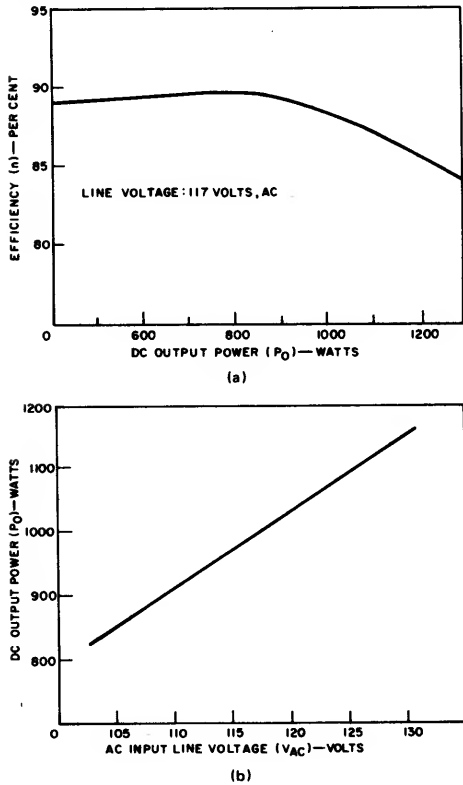


Fig. 189 - Output performance characteristics of the converter: (a) efficiency as a function of dc output power at the nominal ac line voltage; (b) dc output power as a function of the ac input line voltage.

189(a) shows the converter efficiency versus dc output power at the nominal ac line voltage. Fig. 189(b) shows the dc output power as a function of the ac input line voltage. The efficiency is computed by the use of the following formula:

$$\eta = \frac{\text{DC output power}}{\text{AC input power}} \times 100\% \text{ eff.}$$

The losses in efficiency are primarily attributed to power consumption within the semiconductor components. The bulk of this dissipation is due to switching and saturation voltage losses. Since saturated switching techniques are employed, the dominant dissipation factor results from the switching losses. To optimize efficiency, the designer should therefore select devices that offer the best switching characteristics without sacrificing so much safe-operating-area capability that the system becomes unreliable. Because this trade-off exists, the care that should be exercised in device selection cannot be over-emphasized.

Fig. 190 shows typical output collector

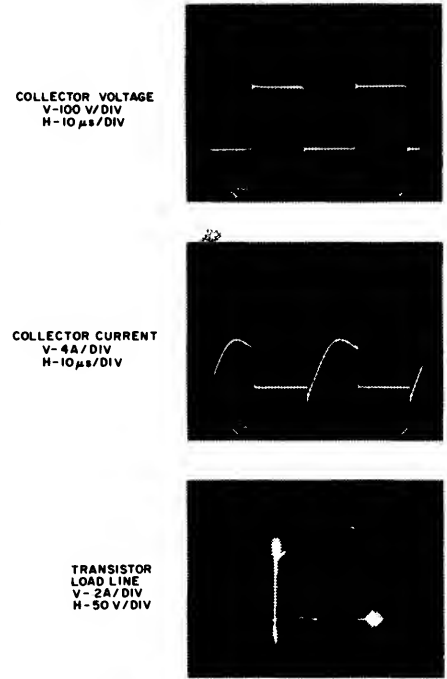


Fig. 190 - Typical output collector voltage, collector current, and load-line waveforms for a 1-kilowatt load at the nominal ac line voltage.

voltage, collector current, and load-line waveforms for a 1-kilowatt load at the nominal ac line voltage. By using these waveforms together with the published safe-operating-area curves and temperature-derating curves found in the transistor data sheet, the designer can determine if the transistor will operate safely and reliably in the circuit.

The bottom waveform in Fig. 191 shows a magnified view of the intensified portion of the fall-time region of the collector-voltage waveform shown in Fig. 190. The inflection seen in Fig. 191 results when simultaneous conduction of both halves of the output-diode bridge reflects an instantaneous short back to the primary side of T_2 and causes a momentary collapse of the collector voltage. This condition occurs during the diode reverse-recovery time and persists until all stored charge is depleted from the junction and the diode ceases conduction. The condition becomes readily apparent in a comparison of the two waveforms in Fig. 191 where the top waveform is the output diode current of one half of the bridge.

TOP: CURRENT
THROUGH DIODE Q21
(V-4 AMP/DIV, H-0.5 μ s/DIV)
BOTTOM: COLLECTOR VOLTAGE
OF Q8 (V-100V/DIV, H-0.5 μ s/DIV)



Fig. 191 - Waveforms showing current through diode D21 and collector voltage of Q8.

Efficiency/Cost Considerations

Some improvement in converter efficiency can be obtained by using two diodes instead of four for full-wave rectification of the output. This change can be readily accomplished by doubling the present number of secondary turns on T_2 and including a center tap for the ground return point. The elimination of a diode drop in the system described previously would represent a saving of 10 to 15 watts of power dissipation when the converter is delivering 1000 watts into a 10-ohm load. Since the forward diode voltage increases with current, the power dissipated by the rectifiers increases as the load-current demand increases. Although the number of secondary turns is doubled, dissipation within the transformer remains essentially unchanged because each

half of the secondary conducts for only 50 percent of the time. The size constraints imposed on a system may make it impossible for a designer to use this approach even though it could offer increased reliability and, possibly, lower system cost. Implementation of this change in the present design would require the use of a larger core and a redesign of the transformer.

Another point to be considered when attempting to optimize efficiency is wire lead length. Because the residual inductance of the leads has an adverse effect on transistor switching speeds, lead lengths should be kept as short as possible. The turn-on times of transistors Q_7 and Q_8 were improved by approximately 0.3 microsecond when the converter breadboard circuit was reassembled into the final form.

2-KILOWATT STEPPED SINE-WAVE INVERTER

The following pages describe the use of the 2N5578 power transistor in a 2-kilowatt, 60-Hz, 117-volt, stepped sine-wave inverter. Additional information is provided to permit conversion of the inverter to 50-Hz, 220-volt operation.

General Circuit Description and Operation

The inverter is frequency regulated, has a peak and average power capability equivalent to a 117-volt rms sine wave, operates from a 24-to-28-volt dc power source, and yields a maximum efficiency of 87 percent. The 2N5578 employed in the inverter is a high-current transistor that is ideally suited to switch up to 60 amperes in a common-emitter inverter configuration. In the following application 3.5 kilowatts of peak power are converted from a 24-to-28-volt dc bus at a frequency of 180 Hz.

The classical method for obtaining a 60-Hz, 117-volt power source from a dc bus is to use a single 60-Hz square-wave inverter. The disadvantages of this method are the large size and considerable weight of the resultant system and the fact that the waveform factor of a square wave does not have the same peak-to-rms voltage ratio as that of a conventional sine wave, a condition required for proper operation of various equipment and appliances. All of these disadvantages are overcome with the stepped approach.

The basic operation of the inverter can be described with the aid of the simplified circuit schematic diagram shown in Fig. 192. Power is taken from a dc supply and inverted into an ac-power square wave by a high-power transistor inverter employing six 2N5578 power transistors. The inverter operates at a frequency of 180 Hz while the output is stepped into a 60-Hz signal. The secondary winding of the inverter transformer is composed of two series-connected windings with different turns ratios, and two SCR's (silicon controlled rectifiers) attached in a bidirectional conduction configuration to the ends of each winding. The other side of each SCR is connected in common with one side of the load, R_L , while

the opposite side of R_L is returned to the off-center tap of the secondary winding. With the inverter in operation, the switching of the SCR's causes a stepped sine wave with the peak-to-average power ratio of a 117-volt ac rms sine wave to appear across R_L . Waveform A of Fig. 192 exists across the secondary winding while waveform B is present across R_L .

Circuit Description

As shown in the block diagram of Fig. 193, the inverter comprises six functions:

- 1. Low-Power Voltage Regulator: Provides a constant voltage of 10 volts to the low-power circuits for supply voltage variations from 24 to 28 volts dc.

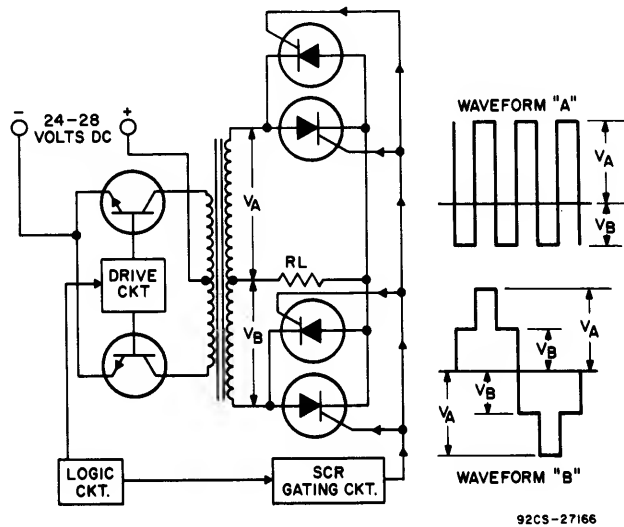


Fig. 192 - Basic circuit schematic diagram.

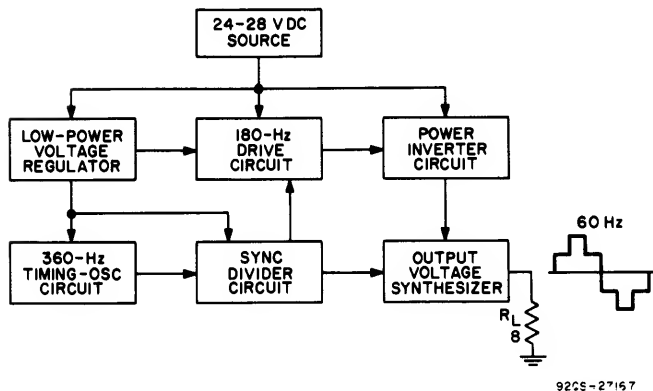


Fig. 193 - Block diagram of a 3.9-kilo-watt-peak, 60-Hz, synthesized sine-wave inverter.

2. 360-Hz Timing Oscillator: Determines the timing reference for the sync divider and drive circuits.
3. Sync Divider: Divides the 360-Hz time-reference signal by two and six to create a 180-Hz drive signal and a 60-Hz SCR gating signal and synchronizes the 60-Hz SCR gating signal with the 180-Hz drive signal.
4. 180-Hz Driver: Amplifies the drive current so that it will be capable of meeting the drive requirements of the power-inverter stage.
5. Power Inverter: Delivers a maximum of 150 amperes into a pair of bifilar-wound primary windings alternately at a rate of 180-Hz. This circuit is composed of a 2-kilowatt power transformer and six 2N5578 power transistors.
6. Output-Voltage Synthesizer: Amplifies the SCR gating signals and drives the SCR's at a 60-Hz rate to simulate the average

power and peak voltage of a 117-volt sine wave.

Detailed Circuit Operation

A detailed schematic diagram of the inverter is shown in Fig. 194. When power is applied to the circuit, the low-power regulator section starts to regulate its output to 10 volts. As the voltage builds up, the 360-Hz reference oscillator begins to generate timing pulses that are fed into the CMOS CD4017AE integrated-circuit ring counter. Seven outputs of the CD4017AE are utilized: six for a dividing function and one for reset. Eight diodes are used in the divider circuit to create two frequencies: 180 Hz and 60 Hz. This type of circuit is employed because of its simplicity and its ability to assure synchronization of the 180-Hz inverter drive signal with the 60-Hz SCR gating signals. Synchronization plays an important part in the voltage synthesizer

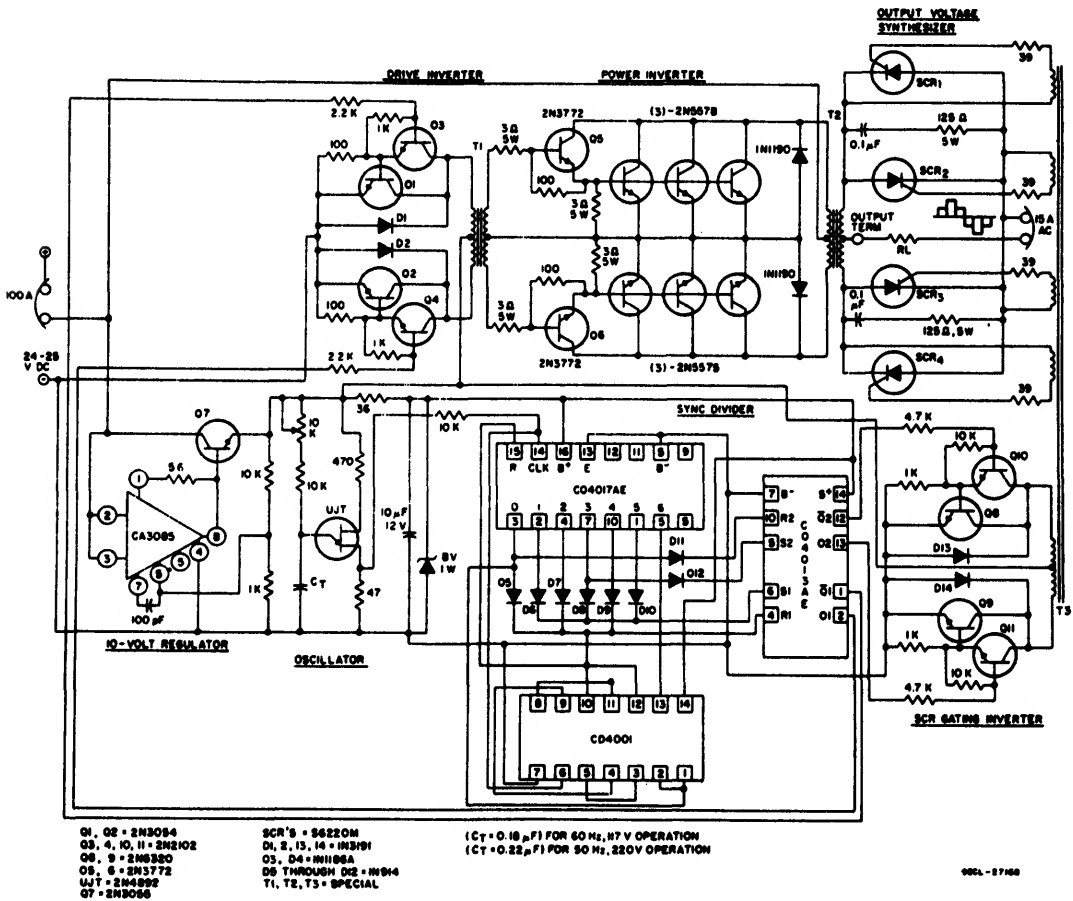


Fig. 194 - 2-kilowatt, stepped sine-wave inverter.

circuit in the simulation of the sine wave voltage across the load.

The 180-Hz and 60-Hz signals are fed into the CMOS CD4013AE dual-data flip-flop. The dual-data flip-flop provides two 60-Hz square-wave signals which are 180 degrees out of phase and which drive the push-pull SCR gating inverter. The other output of the dual-data flip-flop also has two 180-Hz square-wave signals which are 180° out of phase and drive the push-pull inverter drive circuit. The inverter drive circuit supplies 1.5 amperes of base drive to the 2N3772 power transistors in the power inverter.

Each 2N3772 transistor drives three matched 2N5578's in parallel. The 2N5578's operate the inverter output transformer T_2 in push-pull at 180 Hz. As the transformer is switched, the primary current can reach 150 amperes, depending on the load demand. One secondary winding of the transformer is connected to the other in series, as shown in Fig. 194. One winding produces 164 volts while the other produces 84 volts, as shown in Fig. 195.

Fig. 195 illustrates the voltage phase relationship between the primary and secondary windings of the inverter power transformer T_2

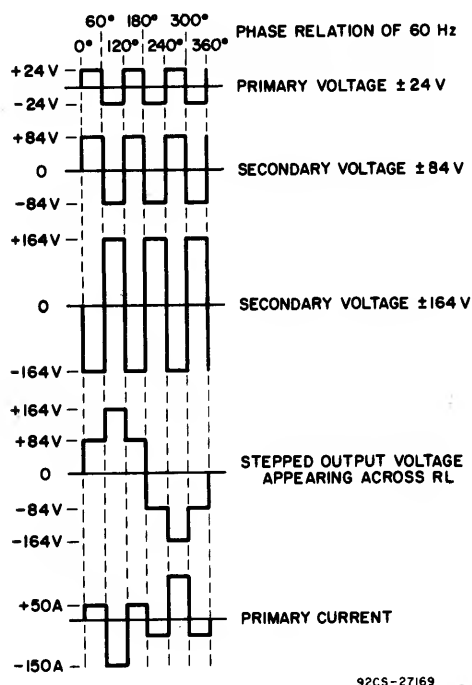


Fig. 195 - Synchronized voltage waveforms of T_2 and stepped output.

and shows the phasing between the secondary voltages and the 60-Hz synthesized sine-wave output voltage.

The voltage synthesizing circuit is a bi-directional full-wave-rectifier bridge circuit in which the SCR's are triggered alternately at 60 Hz to produce a positive or negative voltage swing across the load, R_L . The positive side of the stepped sine wave is produced when SCR's 2 and 3 are triggered together; the negative side is produced when SCR's 1 and 4 are triggered, see Fig. 194.

Circuit Design Considerations

The design of a high-power inverter of the type under discussion is based upon the voltage and power capabilities of the dc source. The 2N5578 was selected on the basis of its high-current switching capability. Careful attention must be given to the published maximum electrical characteristics for each power-transistor type: the maximum allowable case temperature, $V_{CE(sat)}$, H_{FE} , I_C , and V_{BE} . In addition, the minimum load resistance allowed must be determined so that the maximum power limitations of the transistors are not exceeded.

The following procedure is used to determine the required secondary voltage levels for the power transformer. These voltage levels are calculated to simulate the peak voltage and average power of a 117-volt rms sine wave in the output of the inverter circuit.

Step 1. Transistor Voltage Limit

The first step in calculating the safe limit of voltage stress for the 2N3772 and 2N5578 is to establish a typical source that is readily available, such as a battery source of 24 to 28 volts. This source is then used to subject the switching devices to a theoretical maximum of 56 volts, two times the high-line supply voltage resulting from auto transformer action. If a 50-percent margin is allowed for inductive spikes, the V_{CEX} voltage rating of 90 volts is not exceeded.

Step 2 Peak Output Voltage (maximum)

The peak-voltage value (125 volts ac) of a high-line sine wave is next calculated because that is the voltage value at which maximum power must be switched by the power transistors.

$$\text{Peak-Voltage Value} = (\text{Effective Value}) \times (1.414)$$

$$\text{or } (125) \times (1.414) = 177 \text{ volts peak}$$

Step 3. Inverter Output Power (maximum)

The maximum power that can be handled by the power inverter is now determined by multiplying the maximum collector current (I_C) of 150 amperes (50 amperes per 2N5578) by the supply voltage (V_{CC}) of 28 volts minus the switch voltage drop ($V_{CE(sat)}$) of 2 volts.

$$\text{Max. } W = I_C \text{ max.} \times [V_{CC} - V_{CE(sat)}]$$

$$\text{or } (28-2) \times 150 = 3,900 \text{ watts}$$

The power transformer is a non-saturating, driven type that has an estimated efficiency of approximately 96 percent. For practical purposes, the remainder of the calculations can be rounded out to ± 3 percent.

Step 4. Minimum Load Resistance

When the maximum power and peak voltage have been determined, the worst-case load resistance R_L can be calculated:

$$\text{Min. Load Resistance} = \frac{(\text{Max. Peak Output Voltage})^2}{(\text{Max. Inverter Output Power})}$$

$$\text{or } R_L = E^2 / P = \frac{177^2}{3900} = 8 \text{ ohms}$$

Step 5. Output Power

The average power that a 117-volt rms sine wave delivers into an 8-ohm load resistance can now be determined.

$$\text{Average Power} = \frac{(117 \text{ V rms})^2}{R_L}$$

$$\text{or } \frac{(117)^2}{8} = 1,700 \text{ watts}$$

Step 6. Peak Output Voltage (nominal)

At a nominal input voltage of 26 volts minus 2 volts for $V_{CE(sat)}$, a nominal voltage of 24 volts appears across one-half of the primary winding of the power transformer. When this voltage is present, a secondary voltage value must be available that will yield a peak-voltage value for a synthesized sine wave equivalent to that of a 117-volt rms sine wave. The calculation of the peak synthesized sine wave voltage is accomplished as described in Step 2, except that the calculation makes use of the nominal 117-volt rms value.

$$\text{Peak Voltage Value} = (\text{Effective Value}) \times (1.414)$$

$$\text{or } (117) \times (1.414) = 164 \text{ volts peak}$$

Step 7. Step Voltage

In synthesizing a 117-volt rms sine wave for peak voltage and equivalent power, a

minimum of three voltage pulses are added consecutively every 60 degrees to produce 180 degrees of a 60-Hz stepped sine wave. The values of the two voltage pulses A and C indicated in Fig. 196 are equal and, at this point in the calculations, unknown. Pulse B, which is the peak voltage for the stepped sine wave, is known, and is equal to 164 volts. The voltage values for pulses A and C can be determined since A, B and C are the same width and must be related as a square function to provide the same peak-to-average power ratio as a sine wave.

$$\text{Then } \frac{A^2}{3} + \frac{C^2}{3} + \frac{B^2}{3} = 117^2$$

$$\text{and since } A=C, \frac{2A^2 + 164^2}{3} = 117^2$$

$$A=C=84 \text{ volts}$$

Fig. 196 illustrates only the positive side of the stepped sine wave. The negative side is of equal amplitude but negative in direction.

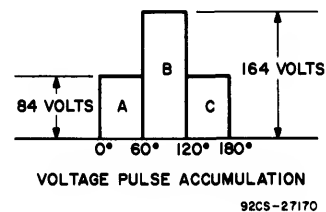


Fig. 196 - Voltage-pulse accumulation.

Step 8. Stepped Wave Power

A check on the previous calculations can be made now that the step voltage levels are known.

$$\text{Average Power} = \frac{(\text{Pulses A+C})^2}{\text{Min. } R_L} + \frac{(\text{Pulse B})^2}{\text{Min. } R_L}$$

$$\text{or } \frac{2 \times (84)^2}{8} + \frac{(164)^2}{8} = 1,700 \text{ W}$$

The information obtained in the check procedure indicates that the peak voltage and power of the sine wave synthesized in the inverter is equivalent to a 117-volt ac sine wave. However, although the peak voltage and power are equivalent, the total harmonic distortion for this type of stepped sine wave is approximately 24 percent. To obtain a sine

Table XIII - Transformer Design Data*

| 180-Hz or 150-Hz Drive Transformer (T ₁) | |
|---|--|
| Core Material | =EI 75 grain-oriented silicon steel |
| Core Size | =square stack |
| Primary | =68 turns, bifilar wound, No. 23 Ga wire @ 10 V |
| Secondary | =41 turns, bifilar wound, No. 21 Ga wire @ 6 V |
| 180-Hz Power Transformer (T ₂) | |
| Core Material | =225 grain-oriented silicon steel |
| Core Size | =2.25 inch x 4.5 inch stack |
| Primary | =5 turns, bifilar wound, .032" thick x 3" wide, Cu @ 24 V |
| No. 1 Secondary | =34 turns, No. 14 Ga wire @ 164 V |
| No. 2 Secondary | =17.5 turns, No. 10 Ga wire @ 84 V |
| 150-Hz Power Transformer (T ₂) | |
| Core Material | =EI 225 grain-oriented silicon steel |
| Core Size | =2.25 inch x 4.5 inch stack |
| Primary | =6 turns, bifilar wound, .032" thick x 3" wide, Cu @ 24 V |
| No. 1 Secondary | =78 turns, No. 14 Ga wire @ 311 V |
| No. 2 Secondary | =39 turns, No. 14 Ga wire @ 156 V |
| 60-Hz or 50-Hz SCR Gating Transformer (T ₃) | |
| Core Material | =EI 625 grain-oriented silicon steel |
| Core Size | =square stack |
| Primary | =180 turns, bifilar wound, No. 28 Ga wire @ 10 V |
| Secondary | =108 turns, 4 separate windings, No. 31 Ga wire @ 6 V each |

*This table includes transformer design data for 60-Hz/117-V and 50-Hz/220-V operation.

wave with a lower distortion content, more than three voltage pulses per polarity change must be provided.

When the two secondary voltage levels have been determined, the inverter power transformer and drive and SCR gating transformers can be designed according to standard transformer design procedures. The data needed to design the transformers used in the subject inverter is shown in Table XIII.

Two additional factors which must be considered when designing this inverter are the drive current and drive voltage needed for the Darlington-connected configuration. As illustrated in the detailed schematic diagram of Fig. 194, the three 2N5578's are driven by a 2N3772 transistor. A minimum gain of 10 was selected for the 2N3772 transistor and the 2N5578's. The total forced gain condition of the Darlington configuration is, then, 100. For 150 amperes of collector current, a base drive current of 1.5 amperes is needed. The typical worst-case V_{BE} for this Darlington configuration is approximately 3 volts. The drive transformer was designed to supply 6 volts of drive for the input. Therefore, a 2-ohm, 3-watt resistor is used in series with the base of each 2N3772 to provide base-current limiting of 1.5 amperes.

Current Sharing—Current sharing of the 2N5578's is achieved by V_{BE} matching as opposed to the less efficient emitter-ballast resistor method. The matching procedure involved the selection of three transistors with V_{BE} 's within 100 millivolts at 50 amperes. Tests indicate that this margin can spread to about 200 millivolts at a case temperature of 75°C. Since the V_{BE} will be exactly the same when the circuit is in operation, the 200-millivolt spread must be related to a collector-current spread. The data-sheet transfer characteristic of Fig. 197(a) indicates a collector-current variation of about 4 amperes. This means that a worst-case match at 150 amperes can yield collector currents of 52, 50, and 48 amperes. Therefore, the value of maximum collector current should be increased by 4 percent in the calculations for power dissipation for each device.

Power Dissipation in the 2N5578—The calculated value of power dissipation is used to determine an adequate heat-sink size for a 100°C maximum case temperature. The junction temperature, which is of main concern, is limited to 175°C for the 2N5578. If an efficiency of 85 percent is achieved at 2 kilowatts, a maximum dissipation of 50 watts per transistor could be expected. The maxi-

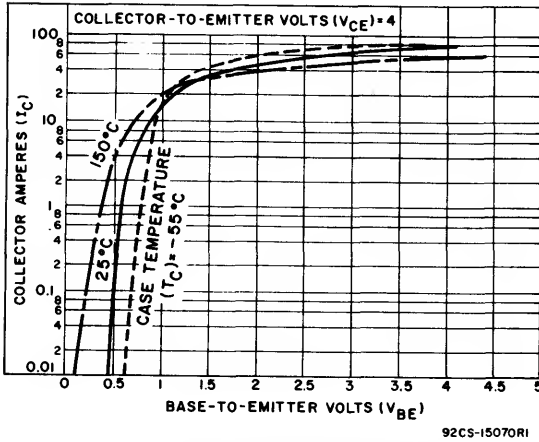


Fig. 197(a) - Typical transfer characteristics for type 2N5578.

junction temperature is then:
 $T_J = T_C + R_{\theta JC} P_d = 100 + 0.5 \times 50 = 125^\circ\text{C}$. This value is acceptable.

Actual dissipation can be calculated with the aid of the primary current waveform of Fig. 195. The dissipation of each transistor during pulses A and C is:

$$P_d = V_{CE}(\text{sat}) \times I_C = 0.45 \text{ V} \times 17 \text{ A} = 7.65 \text{ watts}$$

However, the dissipation during pulse B is much higher since the current and saturation voltage are greater:

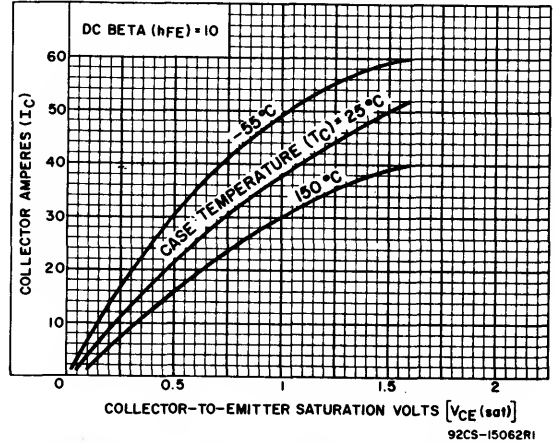


Fig. 197(b) - Typical saturation voltage characteristics for type 2N5578.

$$P_{d(\text{peak})} = 2.0 \text{ V} \times 52 \text{ A} = 104 \text{ watts.}$$

The saturation voltages are determined from the characteristic curve, which is shown in Fig. 197(b). The average power dissipation in each transistor is:

$$P_{d(\text{avg})} = \frac{1}{2} \times 7.65 + \frac{1}{6} \times (104 - 7.65) = 20 \text{ watts and}$$

$$T_{J(\text{avg})} = 100 + 0.5 \times 20 = 110^\circ\text{C}.$$

Clearly, the peak junction temperature during pulse B must be determined to assure that the 175°C temperature is not exceeded. The width of pulse B is $\frac{1}{2} \times \frac{1}{180 \text{ Hz}} = 2.8 \text{ milliseconds}$

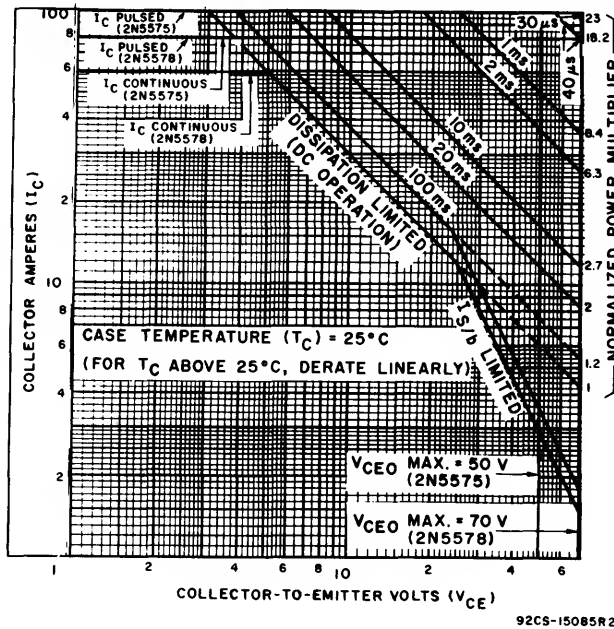


Fig. 197(c) - Collector-to-emitter voltage as a function of collector current.

and, from the maximum operating area of Fig. 197(c), the transient thermal resistance is approximately:

$$R_{\theta JC}(TR) = \frac{175-25^{\circ}\text{C}}{50\text{ A} \times 30\text{ V}} = \frac{150}{1500} = 0.1^{\circ}\text{C/watt}$$

The peak junction temperature at the end of pulse B is then:

$$\begin{aligned} T_{J(\text{peak})} &= T_{J(\text{avg})} + P_{d(\text{peak})} \times R_{\theta JC}(TR) \\ &= 110 + 104 \times 0.1 = 120.4^{\circ}\text{C} \end{aligned}$$

Since the load is primarily resistive, switching losses can be calculated in the traditional way:

$$\begin{aligned} P_{\text{sw(off)}} &= \frac{52\text{ A} \times 28\text{ V}}{6} \times 5\text{ }\mu\text{s} \times 180\text{ Hz} \\ &= 0.22\text{ W} \end{aligned}$$

It is assumed that losses for turn-on power and "shoot-through" (both sides on momentarily) are of the same magnitude; the result is a total switching loss of 1 watt.

Heat Sink

Since the total average power dissipation is now known, the minimum heat sink size can be determined from:

$$T_c = T_a + P_d \times R_{\theta HS} \text{ or } R_{\theta HS} = \frac{T_c - T_a}{P_d}$$

Assuming T_a max. = 60°C and three devices per heat sink:

$$R_{\theta HS} = \frac{100-60}{3 \times 21} = 0.64^{\circ}\text{C/watt}$$

A 0.5°C/watt heat sink was selected.

Performance

A curve of efficiency as a function of output power is shown in Fig. 198. The curve indicates that the high efficiency of a switching inverter can be realized with a simulated sine wave output. The low distortion (less than 1 percent) of a class B amplifier, which is normally used to produce a sine wave, has been sacrificed for efficiency. Ideally, a class B amplifier exhibits a peak efficiency of 78.5 percent, but this efficiency is never realized, and values of 40 to 50 percent are typical. In contrast, the stepped sine wave inverter discussed in the preceding paragraphs exceeds 75 percent efficiency above 500 watts, has an 80 percent efficiency between 650 and 2000 watts, and a peak efficiency of 87 percent at 1300 watts.

The high efficiency contributes to the low

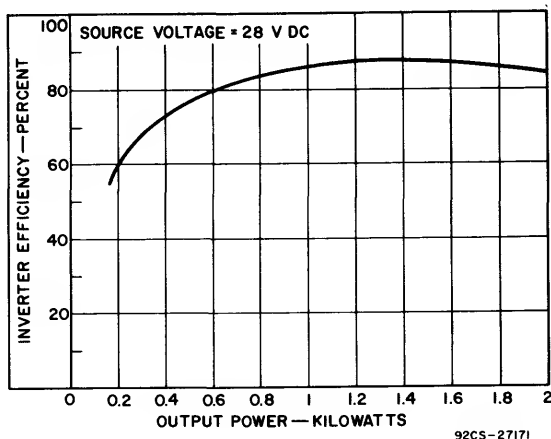


Fig. 198 - Inverter efficiency as a function of output power.

case temperature of the power transistors, approximately 60°C during operation.

Fig. 199, a regulation curve for the inverter, indicates a load regulation of about 7 percent. This value corresponds to an output resistance of 0.45 ohm up to 1500 watts output; resistance increases to 1 ohm at 2 kilowatts.

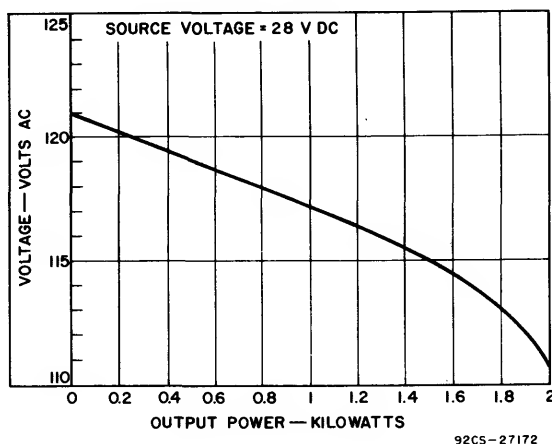


Fig. 199 - Output-voltage regulation as a function of output power.

The efficiency stated above and the power curves shown were generated with a resistive load. Tests with inductive loads indicated that phase shifts up to 60° are allowable before malfunction (common-mode conduction) occurs. Such malfunction results in circuit-breaker trip-out without noticeable damage to the supply.

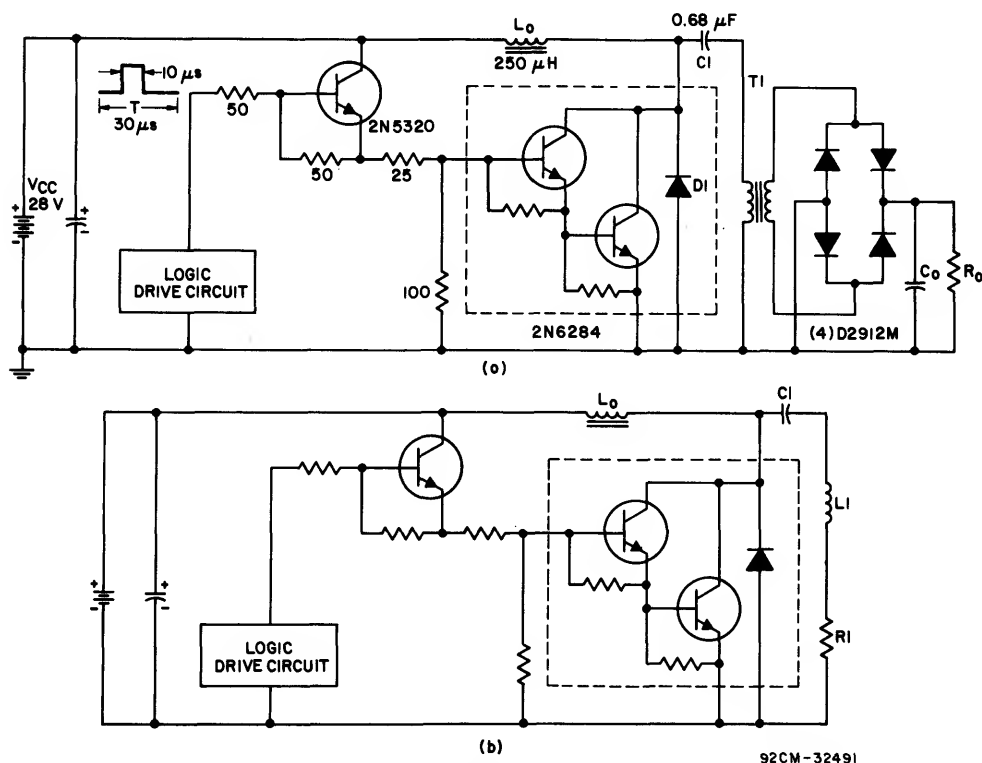


Fig. 200 - Resonant sine-wave inverter circuit.

20-AMPERE SINE-WAVE-INVERTER

Circuit Description

Single-Transistor Inverter—Fig. 200(a) shows the circuit diagram of the single Darlington-transistor sine-wave inverter. The circuit consists of a 28-volt dc power supply, a two-stage power amplifier, a charging choke (L_o) and a series-resonant load circuit, which is formed by capacitor C_1 and transformer T_1 . (Transformer and charging choke data are given on succeeding pages of this section.) The power amplifier utilizes a type 2N5320 transistor as the current source for base drive of the output transistor. The output stage utilizes the type 2N6284 (n-p-n) power Darlington transistor as the power switch; this switch is connected in shunt with the output-load circuit. The series-resonant output-load circuit is formed by capacitor C_1 , the primary leakage inductance of T_1 , and the transformed value of the secondary-load resistance. The secondary-load circuit consists of a full-wave bridge rectifier, which uses four RCA D2412M diodes, and an output filter capacitor C_o , paralleled with load resistor R_o .

Fig. 200(b) illustrates the basic form of the series-resonant circuit as viewed from the collector-emitter terminals of the 2N6284 transistor; Fig. 201 shows typical circuit waveforms. The operation of the circuit is as follows. Initially, capacitor C_1 is charged to a voltage equal to the dc input voltage, V_{cc} . The base of the type 2N5320 transistor is driven by a square-wave pulse whose width is 10 microseconds and whose repetition rate is 30 microseconds. In the type of inverter under discussion, the pulse width is maintained constant during operation; the pulse repetition rate is usually varied, however, to achieve good load regulation. Although the power-Darlington transistor has high gain, a driver stage using the 2N5320 transistor was employed to assure minimum loading on the IC logic circuitry that provides the input-drive signal.

The inverter is turned on by a 10-volt, 10-microsecond pulse, as shown in Fig. 201(b), and both the 2N5320 and 2N6284 transistors are driven into voltage saturation. During this interval, the 2N6284 transistor acts as a closed switch, essentially shorting capacitor C_1 to

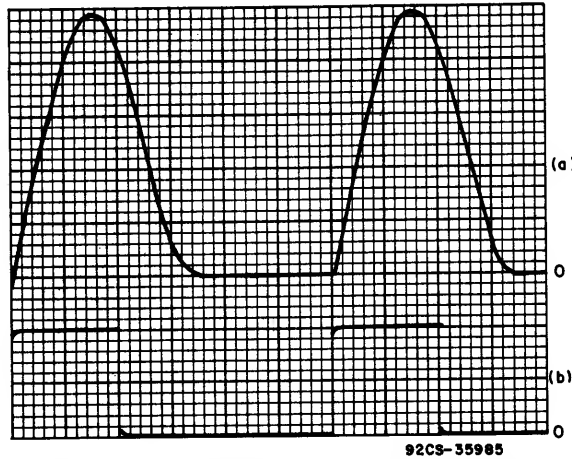


Fig. 201 - Inverter turn-on waveforms:
 (a) Collector current $I_c = 5$
 A/div.; (b) Input base drive
 voltage $V_b = 5$ V/div. ($t = 5$
 μ s/div.)

ground. Capacitor C_1 discharges its energy through inductor L_1 and resistor R_1 . The series combination of C_1 , L_1 , and R_1 forms a series resonant circuit whose natural resonant frequency is approximately 50 kHz. A sinusoidal load current ($I_c(pk)$) having a maximum amplitude of 25 amperes flows in the output circuit, as shown in Fig. 201(b). The internal diode, D_1 , of the power-Darlington transistor assures closure of the collector-emitter circuit and provides a path for any reverse-current conduction. The extent to which reverse current will flow through the diode depends upon the circuit loading and the repetition rate of the driving signal. In the implementation of the circuit of Fig. 200, the loading and repetition rate were adjusted to achieve maximum output power with good efficiency; this adjustment minimizes reverse-current flow.

Figs. 202(a) and 202(b) show the relationship between the collector current and the collector-emitter voltage of the Darlington power transistor. At the end of the 10-microsecond input-pulse interval, the drive signal is turned off for 20 microseconds. Since both the transistor and diode are then non-conducting, the combination approximates an open switch. Output capacitor C_1 is recharged by the dc input voltage, V_{cc} , through choke L_o . The resultant voltage across the transistor increases in magnitude to a peak value substantially greater than V_{cc} , as shown in Fig. 202(b). Because collector-current conduction is de-

layed until after complete collector-voltage saturation, and because the collector voltage is reapplied at the time of zero collector-current conduction, no significant transition losses occur. The main power losses occur during the on-state conduction period, and are contributed to by the associated circuit losses in the output transformer and rectifier diodes. No reverse-bias base current drive is required during turn-off.

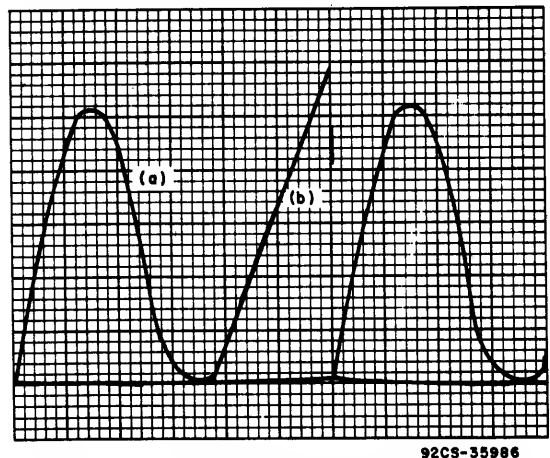


Fig. 202 - Relationship between collector current and collector-emitter voltage of Darlington power transistor: (a) Collector current $I_c = 5$ A/div.; (b) collector-to-emitter voltage $V_{CE} = 20$ V/div. ($t = 5 \mu$ s/div.)



Fig. 203 - DC output-voltage waveform
($t=5\text{ }\mu\text{s/div.}$).

Fig. 203 shows the waveform of the dc output voltage of the circuit of Fig. 200. The level of output is 48 volts across a 12-ohm load resistor for a dc output power of 192 watts. DC input power is 218.4 watts, so that circuit efficiency is 87 percent. Overall circuit per-

formance data is presented in Table XIV. Fig. 204 shows the performance of the circuit with changing load. The repetition rate may be adjusted, as shown in Fig. 204, to provide a constant output voltage of 48 volts.

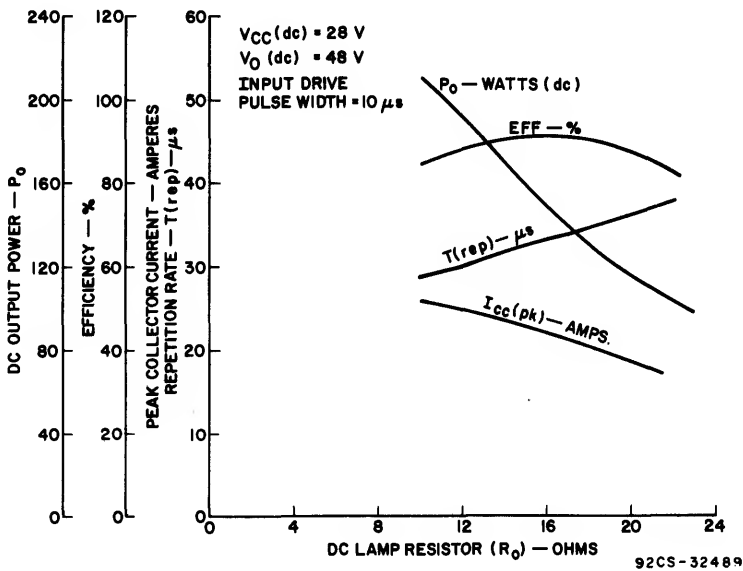


Fig. 204 - Performance of the sine-wave inverter with changing loads.

Table XIV - Typical Performance Data

| Characteristic | Value | Units |
|--|------------------------------|----------|
| DC Supply Voltage (V_s) | 28 | V |
| DC Input Current (I_{dc}) | 8 | A |
| Peak Collector Current (I_{pk}) | 25 | A |
| DC Output Voltage (V_o) | 48 | V |
| DC Output Load (R_o) | 12 | Ω |
| DC Output Power (P_o) | 192 | W |
| DC Input Power (P_s) | 218.4 | W |
| Efficiency (η_p) | 87 | % |
| Output Resonant Freq. (T_o) | 50 | kHz |
| Input Pulse Width (T_P) | 10 | μs |
| Pulse Repetition Rate T(rep.) | 30 | μs |
| Transformer and Charging-Choke Data | | |
| Transformer T_1 | | |
| Primary Inductance (L_p) | 110 μH | |
| Number Turns (N_p) | 24 T | |
| Wire Size: | 56/30 Litz (Twisted Pair) | |
| Secondary Inductance (L_s) | 375 μH | |
| Number Turns (N_s) | 43 | |
| Wire Size: | 56/30 Litz (Twisted Pair) | |
| Core: | Indiana General IR8207 | |
| Air Gap | 30 mils | |
| Note: $\frac{1}{2}$ N_p wound on separate coil form $\frac{1}{2}$ N_p wound on same form with N_s | | |
| Charging Choke | | |
| Inductance (L_o) | 250 μH | |
| Number Turns (N) | 36 T | |
| Wire Size: | 56/30 Litz (Twisted Pair) | |
| Core: | Indiana General IR8207 | |
| Air Gap: | 30 mils | |