Build a charge pump with ultralow quiescent current

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ORTABLE BATTERY-powered devices often spend most of their life in standby mode, in which the quiescent current of an internal boost converter continuously bleeds the battery. The quiescent current during standby can be larger than the actual load current. Though several inductor-based converters offer maximum quiescent current of less than 10 µA, designers usually prefer or require a regulated charge pump for cost-sensitive designs that must be intrinsically safe. Off-theshelf regulated charge pumps with output-current capabilities of at least 10 mA have typical minimum quiescent currents of 50 to 100 µA. If that level of quiescent current is unacceptable, you can reduce the overall average by adding circuitry that remotely monitors the regulated voltage and toggles the charge pump into and out of shutdown. That approach, however, may not achieve the desirable quiescent-current level of less than 10 µA. The advent of low-on-resistance analog switches and ultralow-current comparators and references makes possible a charge-pump circuit whose maximum quiescent current is approximately 7 µA (Figure 1).

Charge pumps use an ac-coupling technique to transfer energy from a transfer capacitor to a storage capacitor. The transfer capacitor first charges via analog switches to the level of $V_{\rm BATT}$, and then other analog switches transfer the

Figure 1 V_{OUT} V_{OUT} V_{OUT} V_{OUT} V_{OUT} V_{OUT} V_{BATT} V_{OUT} V_{O

This charge-pump circuit uses analog switches to achieve ultralow quiescent current.

energy to a storage capacitor tied to $V_{\rm OUT}$. The transfer capacitor then charges again, and the cycle repeats. With ideal analog switches exhibiting zero loss, the $V_{\rm OUT}$ level equals two times $V_{\rm BATT}$. As expected, however, the analog switches' finite on-resistance produces an output level that drops in proportion to the load current. The basic regulated charge pump in **Figure 1** includes an oscillator, several analog switches, a volt-

age reference, and a comparator. The comparator serves as a voltage monitor and an oscillator. When the circuit is in regulation, the comparator output is low, which closes the NC (normally closed) switches and allows C₁ to charge to V_{BATT}. When the voltage at V_{OUT} dips below the output-regulation threshold—3.3V in this case—the comparator output goes high. The NO (normally open) switches close, transferring C₁'s

design ideas

charge to C_2 . This cycle repeats until V_{OUT} regains regulation.

Resistors R, to R, provide the hysteresis necessary for oscillation. Their value, 1 M Ω , creates a notable level of hysteresis and minimizes V_{BATT} loading. As the comparator output changes state, feedback resistor R₅ creates hysteresis by moving the threshold you apply to the comparator's positive input. For the resistor values shown, reference value nominal for IC₁ (1.182V), and V_{BATT} =3V, the V_{IN} +threshold swings between approximate values of $V_{IN} + (low) = 0.39V$ and $V_{IN} + (high) =$ 1.39V. When the circuit is in regulation, V_{IN}- slightly exceeds V_{IN}+, the comparator output is low, the R₁-R₂ divider senses the voltage at V_{OUT}, and the threshold at V_{IN} + is low (0.39V). With V_{IN} + at 0.39V, you can calculate the R_1 and R, values from the equation

 V_{IN} += V_{OUT} [R_2 /(R_1 + R_2)]. The resistance of R_1 + R_2 should be greater than 1 MΩ to minimize V_{BATT} loading. If V_{OUT} = 3.3V and R_2 is 2.2 MΩ, R_1 calculates to 301 kΩ. Capacitor C_3 connects to the comparator's V_{IN} – input. Along with R_1 and R_2 , C_3 sets the oscillation frequency according to the following simplified relationships: $t_{DISCHARGE}$ = t_{LOW} = $-(R_2C_3)\ln[(V_{IN} + (LOW))/(V_{IN} + HIGH))];$ t_{CHARGE} = t_{HIGH} = $-(R_2C_3)\ln[1 - (V_{IN} + (HIGH) - V_{IN} + (LOW))/(V_{BATT} - V_{IN} + (LOW))$; and t_{OSC} = $1/t_{PERIOD}$, where $t_{DISCHARGE}$ = t_{LOW} + t_{LOW} = t_{LOW} + t_{LOW} and t_{OSC} = t_{PERIOD} , where $t_{DISCHARGE}$ = t_{LOW} + t_{LOW} = t_{LOW} + t_{LOW} and t_{OSC} = t_{PERIOD} , where $t_{DISCHARGE}$ = t_{LOW} + t_{LOW} + t_{LOW} = t_{LOW} + t_{LOW} + t_{LOW} + t_{LOW} = t_{LOW} + t_{LOW} + t

where $t_{PERIOD} = t_{LOW} + t_{HIGH}$. To maximize efficiency and reduce the effects of comparator slew rate, you should set a relatively low frequency. Choosing $C_3 = 470$ pF yields the following: $t_{LOW} = 178$ µsec, and $t_{HIGH} = 68$ µsec; thus, $f_{OSC} = 4$ kHz.

Select the values of C₁ and C₂ to achieve the desired load current and rip-

ple. For this application ($I_{LOAD} = 10 \text{ mA}$), $C_1 = 10 \text{ }\mu\text{F}$. To calculate the value of C_2 , make an approximation based on the desired ripple voltage: $C_2 = (I_{LOAD} \times t_{LOW})/V_{RIPPLE}$. With $I_{LOAD} = 10 \text{ mA}$ and $V_{RIPPLE} = 150 \text{ mV}$, $C_2 = 12 \text{ }\mu\text{F}$.

With these component values, the circuit draws a maximum quiescent current of 6.9 µA and offers a considerable improvement over off-the-shelf charge pumps. You can further lower the quiescent current by increasing the resistor values, but that effect is minimal because IC,'s maximum quiescent current of 3.8 µA dominates the total. This circuit lets you implement an ultralow-quiescent-current-regulated charge pump. Until off-the-shelf options are available, it provides an alternative for designers seeking to implement a low-cost design without the use of inductors.

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