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JFET-based dc/dc converter operates from 300-mV supply

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You use a JFET's self-biasing characteristics to build a dc/dc converter that operates from power sources such as solar cells, thermopiles, and single-stage fuel cells, all of which deliver less than 600 mV and sometimes as little as 300 mV. **Figure 1** shows the drain-to-source characteristics of an N-channel JFET under zero-bias conditions, which you can produce by connecting its gate and source together. Applying 100 mV causes a current of 10 mA to flow through the device, increasing to 30 mA at 350 mV. Exploiting the JFET's ability to conduct significant current at zero bias makes it possible to design a self-starting, low-input-voltage converter.

The circuit can supply 5V at currents as large as 2 mA—enough to serve many micropowered applications or to provide auxiliary bias for a higher power switched-mode voltage regulator. At 300-mV input, the circuit starts up at load currents of 300 µA. A load current of 2 mA requires an input of 475 mV.

In **Figure 2**, Q_1, a parallel-connected pair of Philips Semiconductor's (www.semiconductors.philips.com) BF862 JFETs, and Coiltronics' (www.coiltronics.com) Versa-Pac transformer, T_1, form an oscillator in which T_1's secondary winding provides feedback to Q_1's gate. When you first apply power, Q_1's gate rests at 0V, and drain current flows through T_1's primary winding. T_1's phase-inverted secondary winding responds by delivering a negative voltage to Q_1's gate, which turns off Q_1 and interrupts current flow through T_1's primary winding. In turn, T_1's secondary voltage collapses, and sustained oscillations begin. Although the BF862's published specifications do

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from IC_1 varies Q_1's on-time through Q_3 to close the control loop and maintain output-voltage regulation. **Figure 3** shows the ripple voltage present at the power supply's output. When the output voltage decays, comparator IC_1 switches (Trace B, middle) and allows Q_1 to oscillate. The resulting flyback events at Q_1's drain (Trace C, bottom) restore the output voltage.

Using Q_3 as a simple but effective shunt control for Q_1's gate voltage results in a 25-mA quiescent-current drain from the power source. A modification reduces the quiescent drain to 1 mA (**Figure 4**). Inserting switch Q_4 in series with T_1's secondary winding more efficiently controls Q_1's gate. Bootstrapping the voltage across T_1's secondary winding produces negative-turn-off-bias voltage for Q_4. **Figure 5** illustrates how to connect T_1's wind-

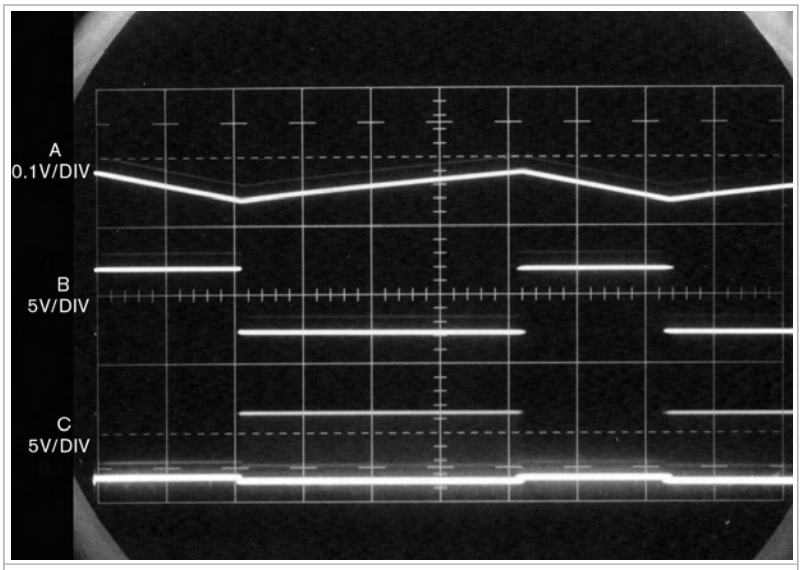
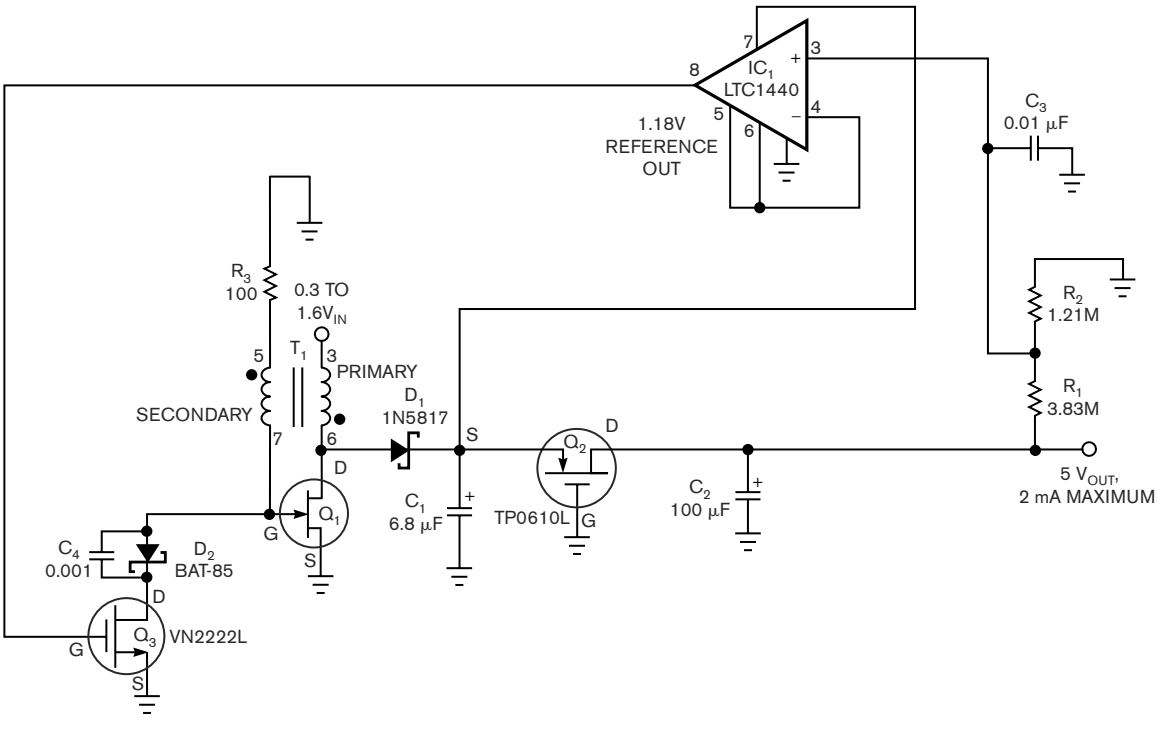


Figure 3 The dc output (Trace A), comparator IC_1's output, and the voltage at Q_1's drain (Trace C) have a horizontal-deflection factor of 5 msec.



NOTES:
1. USE ±1%-TOLERANCE METAL-FILM RESISTORS FOR R_1 AND R_2.
2. CONNECT T_1 AS SHOWN IN FIGURE 5.
3. Q_1 COMPRISES PHILIPS BF862 JFETs CONNECTED IN PARALLEL.

Figure 2 A pair of parallel-connected JFETs allows this dc/dc converter to operate from power sources that supply as little as 300 mV.

ings. When Q_4 switches off, it interrupts the current flowing in T_1's secondary winding and drives T_1's Pin 5 positive. Without diodes D_4 and D_5, the peak voltage would approach 15V and reverse-bias Q_4, an undesirable condition. Under normal operating conditions, excursions of approximately 0.8V appear at Pin 5, necessitating the use of two series-connected diodes to clamp the voltage at a safe level. Zener diode D_3 holds off bias-supply loading to aid start-up during initial power application.EDN

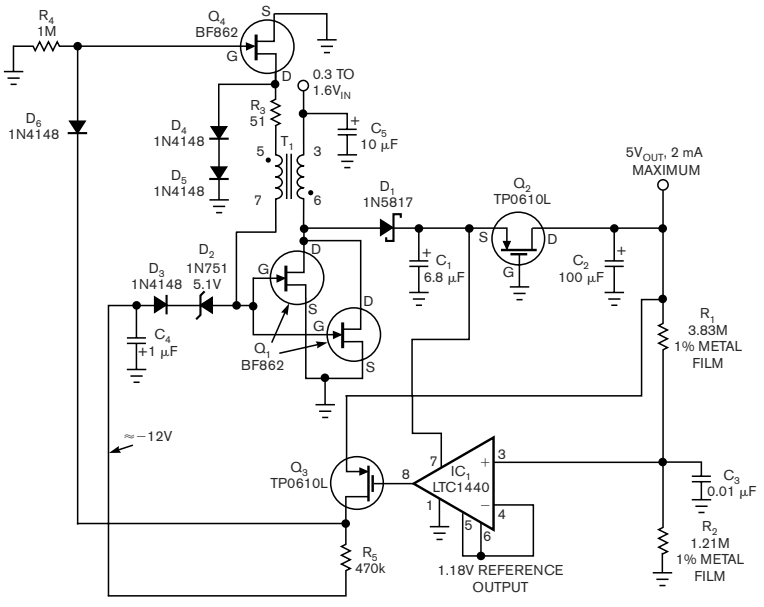


Figure 4 Adding Q_3, Q_4, and the bootstrapped negative-bias generator comprising D_2, D_3, and C_4 reduces the circuit's quiescent current from 25 mA to 1 mA.

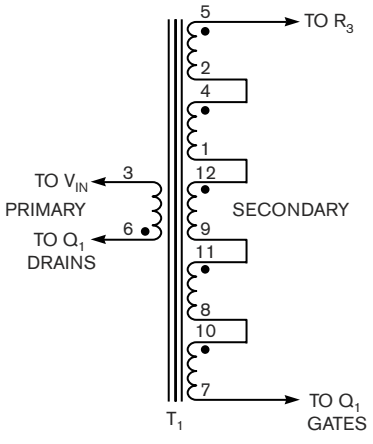


Figure 5 Comprising six independent windings that offer more than 500 configurations, Coiltronics' VP1-1400 serves as a combination feedback and flyback transformer in this application. Connect the windings as shown.

Configurable logic gates' Schmitt inputs make versatile monostables

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You can assemble a pulse-generation circuit from a simple Schmitt-input AND gate plus a resistor-capacitor timing network. However, if you need a logic function that's not a standard catalog item, you need a Schmitt-input gate or inverter and an additional logic gate. Drawing from an earlier Design Idea (**Reference 1**) and a recent design requirement for adding pulse-generation functions to a crowded pc board, I searched Fairchild Semiconductor's Web site (www.fairchildsemi.com) for small-footprint Schmitt-input logic gates and found only "old faithfuls"—familiar Schmitt-input AND gates and Schmitt buffers.

Disappointed, I investigated other logic offerings from Fairchild and stumbled across a section of the Web site that describes "configurable logic gates." Lo and behold, I suddenly realized I was looking at the solution to my problem. The NC7SZ57 and NC7SZ58 (**Reference 2**) comprise tiny, six-pin surface-mount packages that you can configure as inverters or as AND, OR, or XOR gates, all of which allow the inversion of one input. These devices feature inverted outputs, overvoltage-input tolerance, and high current drive.

Every input has hysteresis, making these devices ideal for timed pulse generation. A design that combines digital logic with analog interfaces often requires timed pulses and delays, along with pulse shorteners and stretchers. For applications in which exact pulse times are not critical, the added feature of Schmitt inputs allows the delay of one input using an RC (resistance-capacitance) timing network. When the slowly changing RC circuit's output crosses the analog-level upper- or lower-trip-point thresholds, the Schmitt feature converts the slowly rising and falling voltages to fast digital edges.

Texas Instruments (www.ti.com)