LINEAR TECHNOLOGY

Application Note 29

October 1988

Some Thoughts on DC-DC Converters

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INTRODUCTION

Many systems require that the primary source of DC power be converted to other voltages. Battery driven circuitry is an obvious candidate. The 6V or 12V cell in a laptop computer must be converted to different potentials needed for memory, disc drives, display and operating logic. In theory, AC line powered systems should not need DC-DC converters because the implied power transformer can be equipped with multiple secondaries. In practice, economics, noise requirements, supply bus distribution problems and other constraints often make DC-DC conversion preferable. A common example is logic dominated, 5V powered systems utilizing ±15V driven analog components.

The range of applications for DC-DC converters is large, with many variations. Interest in converters is commensurately quite high. Increased use of single supply powered systems, stiffening performance requirements and battery operation have increased converter usage.

Historically, efficiency and size have received heavy emphasis. In fact, these parameters can be significant, but often are of secondary importance. A possible reason behind the continued and overwhelming attention to size and efficiency in converters proves surprising. Simply put, these parameters are (within limits) *relatively easy to achieve*! Size and efficiency advantages have their place, but other system-oriented problems also need treatment. Low quiescent current, wide ranges of allowable inputs, substantial reductions in wideband output noise and cost effectiveness are important issues. One very important converter class, the 5V to ±15V type, stresses size and efficiency with little emphasis towards parameters such as output noise. This is particularly significant because wideband output noise is a frequently encountered problem with this type of converter. In the best case, the output noise mandates careful board layout and grounding schemes. In the worst case, the noise precludes analog circuitry from achieving desired performance levels (for further discussion see Appendix A , "The 5V to ±15V Converter — A Special Case"). The 5V to ±15V DC-DC conversion requirement is ubiquitous, and presents a good starting point for a study of DC-DC converters.

5V TO ±15V CONVERTER CIRCUITS

Low Noise 5V to ±15V Converter

Figure 1's design supplies a ±15V output from a 5V input. Wideband output noise measures 200 microvolts peak-to-peak, a 100× reduction over typical designs. Efficiency at 250mA output is 60%, about 5-10% lower than conventional types. The circuit achieves its low noise performance by minimizing high speed harmonic content in the power switching stage. This forces the efficiency trade-off noted, but the penalty is small compared to the benefit.

The 74C14 based 30kHz oscillator is divided into a 15kHz two phase clock by the 74C74 flip flop. The 74C02 gates and 10K-0.001μF delays condition this two phase clock

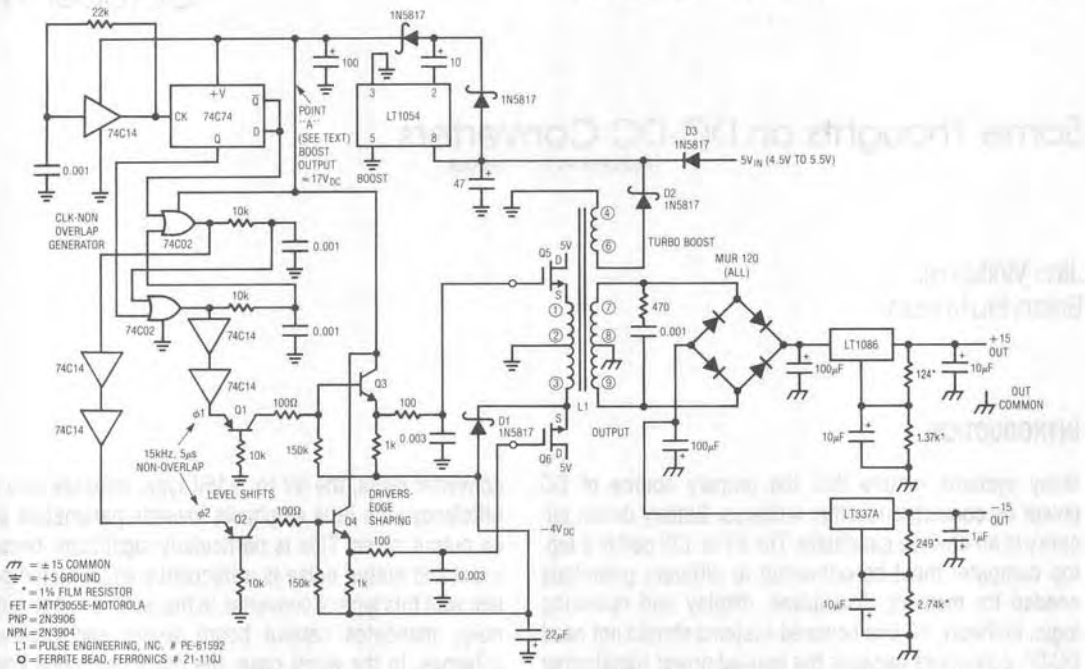


Figure 1. Low Noise 5V to ± 15V Converter

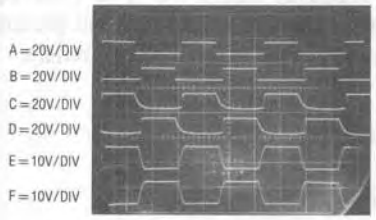


Figure 2. 5V to ± 15V Low Noise Converter Waveforms

into non-overlapping, two phase drive at the emitters of Q1 and Q2 (Figure 2, traces A and B, respectively). These transistors provide level shifting to drive emitter followers Q3-Q4. The Q3-Q4 emitters see 100Ω-0.003μF filters, slowing drive to output MOSFET's Q5-Q6. The filter's effects appear at the gates of Q5 and Q6 (traces C and D, respectively). Q5 and Q6 are source followers, instead of the conventional common source connection. This limits transformer rise time to the gate terminals filtered slew rate, resulting in well controlled waveforms at the sources of Q5 and Q6 (traces E and F, respectively). L1 sees complimentary, slew limited drive, eliminating the high speed harmonics normally associated with this type converter. L1's output is rectified, filtered and regulated to obtain the final output. The 470Ω-0.001μF damper in L1's output maintains loading during switching, aiding low noise performance. The ferrite beads in the gate leads eliminate parasitic RF oscillations associated with follower configurations.

The source follower configuration eases controlling L1's edge risetimes, but complicates gate biasing. Special provisions are required to get the MOSFET's fully turned on and off. Source follower connected Q5 and Q6 require voltage overdrive at the gates to saturate. The 5V primary supply cannot provide the specified 10V gate — channel bias required for saturation. Similarly, the gates must be pulled well below ground to turn the MOSFETs off. This is so because L1's behavior pulls the sources negative when the devices turn off. Turn-off bias is bootstrapped from the negative side of Q6's source waveform. D1 and the 22μF

capacitor produce a −4V potential for Q3 and Q4 to pull down to. Turn-on bias is generated by a two stage boost loop. The 5V supply is fed via D3 to the LT1054 switched capacitor voltage converter (switched capacitor voltage converters are discussed in Appendix B, "Switched Capacitor Voltage Converters — How They Work"). The LT1054 configuration, set up as a voltage doubler, initially provides about 9V boost to point "A" at turn-on. When the converter starts running L1 produces output ("Turbo Boost" on schematic) at windings 4-6 which is rectified by D2, raising the LT1054's input voltage. This further raises point "A" to the 17V potential noted on the schematic.

These internally generated voltages allow Q5 and Q6 to receive proper drive, minimizing losses despite their source follower connection. Figure 3, an AC coupled trace of the 15V converter output, shows 200μVp-p noise at full power (250mA output). The −15V output shows nearly identical characteristics. Switching artifacts are comparable in amplitude to the linear regulators noise. Further reduction in switching based noise is possible by slowing Q5 and Q6 risetimes. This, however, necessitates reducing clock rate and increasing non-overlap time to maintain available output power and efficiency. The arrangement shown represents a favorable compromise between output noise, available output power, and efficiency.

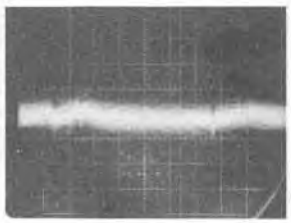


Figure 3. Output Noise of the Low Noise 5V to ±15V Converter

Ultra-Low Noise 5V to ±15V Converter

Residual switching components and regulator noise set Figure 1's performance limits. Analog circuitry operating at the very highest levels of resolution and sensitivity may require the lowest possible converter noise. Figure 4's converter uses sine wave transformer drive to reduce harmonics to negligible levels. The sine wave transformer drive combines with special output regulators to produce less than 30μV of output noise. This is almost 7× lower than the previous circuit and approaches a 1000× improvement over conventional designs. The trade off is efficiency and complexity.

A1 is set up as a 16kHz Wein bridge oscillator. The single power supply requires biasing to prevent A1's output from saturating at the ground rail. This bias is established by returning the undriven end of the Wein network to a DC potential derived from the LT1009 reference. A1's output is a pure sine wave (Figure 5, trace A) biased off ground. A1's gain must be controlled to maintain sine wave output. A2 does this by comparing A1's rectified and filtered positive output peaks with an LT1009 derived DC reference. A2's output, biasing Q1, servo controls A1's gain. The 0.22μF capacitor frequency compensates the loop, and the thermally mated diodes minimize errors due to rectifier temperature drift. These provisions fix A1's AC and DC output terms against supply and temperature changes.

A1's output is AC coupled to A3. The 2k −820Ω divider re-biases the sine wave, centering it inside A3's input common mode range even with supply shifts. A3 drives a power stage, Q2-Q5. The stages common emitter outputs and biasing permit $1V_{RMS}$ (3Vp-p) transformer drive, even at V supply = 4.5V. At full converter output loading the stage delivers 3 ampere peaks but the waveform is clean (trace B), with low distortion (trace C). The 330μF coupling capacitor strips DC and L3 sees pure AC. Feedback to A3 is taken at the Q4-Q5 collectors. The 0.1μF unit at this point suppresses local oscillations. L3's secondary RC network adds additional high frequency damping.

Without control of quiescent current the power stage will encounter thermal runaway and destroy itself. A4 measures DC output current across Q5's emitter resistor and servo controls Q6 to fix quiescent current. A divided portion of the LT1009 reference sets the servo point at A4's negative input and the 0.33μF feedback capacitor stabilizes the loop.

L3's rectified and filtered outputs are applied to regulators designed for low noise. A5 and A7 amplify the LT1021's filtered 10V output up to 15V. A6 and A8 provide the −15V output. The LT1021 and amplifiers give better noise performance than three terminal regulators. The zener-resistor network clips overvoltages due to start-up transients.

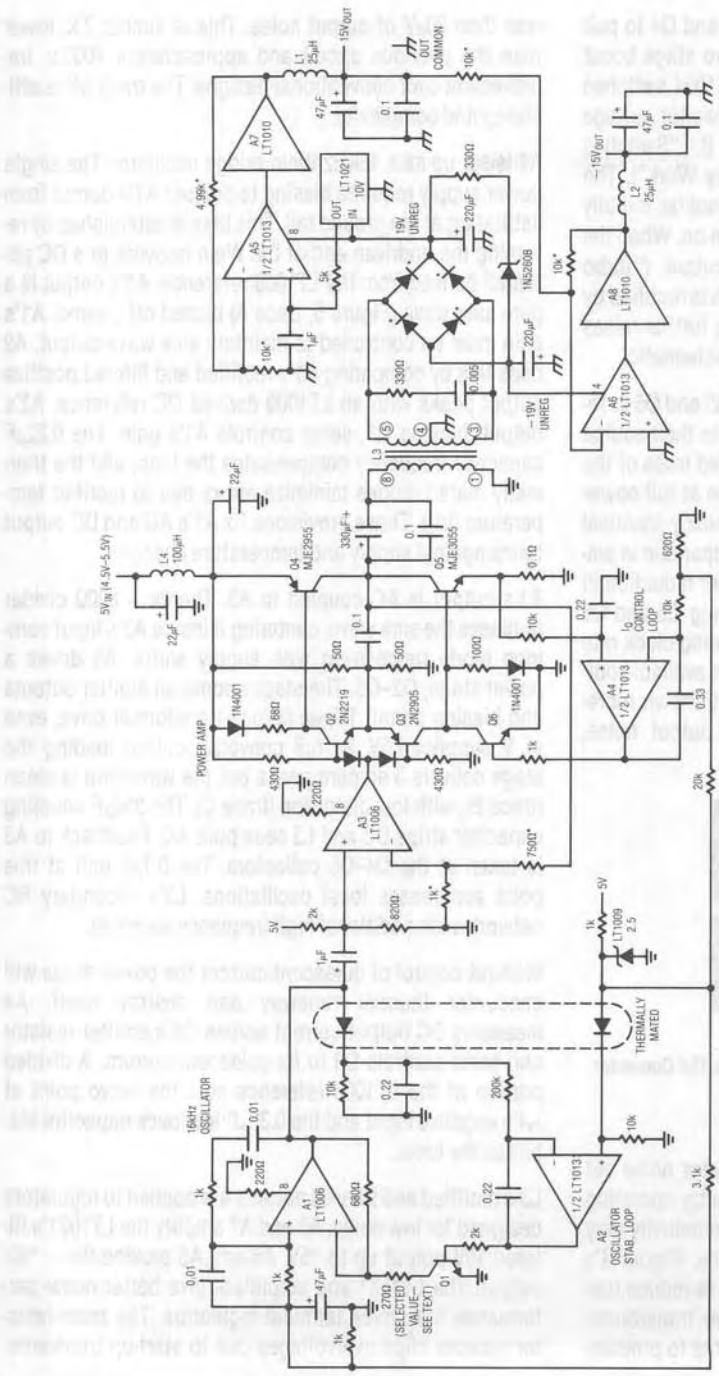


Figure 4. Ultra Low Noise Sine Wave Drive 5V to ±15V Converter

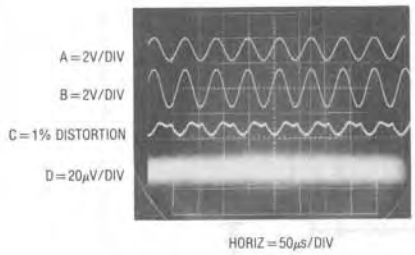


Figure 5. Waveforms for the Sine Wave Driven Converter. Note that Output Noise (Trace D) is Only 30μVp-p.

L1 and L2 combine with their respective output capacitors to aid low noise characteristics. These inductors are outside the feedback loop, but their low copper resistance does not significantly degrade regulation. Trace D, the 15V output at full load, shows less than 30μV (2ppm) of noise. The most significant trade-off in this design is efficiency. The sine wave transformer drive forces substantial power loss. At full output (75mA), efficiency is only 30%.

Before use, the circuit should be trimmed for lowest distortion (typically 1%) in the sine wave delivered to L3. This trim is made by selecting the indicated value at A1's negative input. The 270Ω value shown is nominal, with a typical variance of ±25%. The sine wave's 16kHz frequency is a compromise between the op amps available gain-bandwidth, magnetics size, audible noise, and minimization of wideband harmonics.

Single Inductor 5V to ±15V Converter

Simplicity and economy are another dimension in 5V to ±15V conversion. The transformer in these converters is usually the most expensive component. Figure 6's unusual drive scheme allows a single, two terminal inductor to replace the usual transformer at significant cost savings. Trade-offs include loss of galvanic isolation between input and output and lower power output. Additionally, the regulation technique employed causes about 50mV of clock related output ripple.

The circuit functions by periodically and alternately allowing each end of the inductor to flyback. The resultant positive and negative peaks are rectified and filtered. Regulation is obtained by controlling the number of flyback events during the respective output's flyback interval.

The leftmost logic inverter produces a 20kHz clock (trace A, Figure 7) which feeds a logic network composed of additional inverters, diodes and the 74C90 decade counter. The counter output (trace B) combines with the logic network to present alternately phased clock bursts (traces C and D) to the base resistors of Q1 and Q2. When $\phi 1$ (trace B) is unclocked it resides in its high state, biasing Q2 and Q4 on. Q4's collector effectively grounds the "bottom" of L1 (trace H). During this interval $\phi 2$ (trace A) puts clock bursts into Q1's base resistor. If the –15V output is too low servo comparator C1A's output (trace E) is high, and Q1's base can receive pulsed bias. If the converse is true the comparator will be low, and the bias gated away via Q1's base diode. When Q1 is able to bias, Q3 switches, resulting in negative going flyback events at the "top" of L1 (trace G). These events are rectified and filtered to produce the –15V output. C1A regulates by controlling the number of clock pulses that switch the Q1-Q3 pair. The LT1004 serves as a reference. Trace J, the AC coupled –15V output, shows the effect of C1A's regulating action. The output stays within a small error window set by C1A's switched control loop. As input voltage and loading conditions change C1A adjusts the number of clock pulses allowed to bias Q1-Q3, maintaining loop control.

When the $\phi 1$ and $\phi 2$ signals reverse state the operating sequence reverses. Q3's collector (trace G) is pulled high with Q2-Q4 switching controlled by C1B's servo action. Operating waveforms are similar to the previous case. Trace F is C1B's output, trace H is Q4's collector (L1's "bottom") and trace I is the AC coupled 15V output. Although the two regulating loops share the same inductor they operate independently, and asymmetrical output loading is not deleterious. The inductor sees irregularly spaced shots of current (trace K), but is unaffected by its multiplexed operation. Clamp diodes prevent reverse biasing of Q3 and Q4 during transient conditions. The circuit provides ±25mA of regulated power at 60% efficiency.

Low Quiescent Current 5V to ±15V Converter

A final area in 5V to ±15V converter design is reduction of quiescent current. Typical units pull 100-150mA of quiescent current, unacceptable in many low power systems.

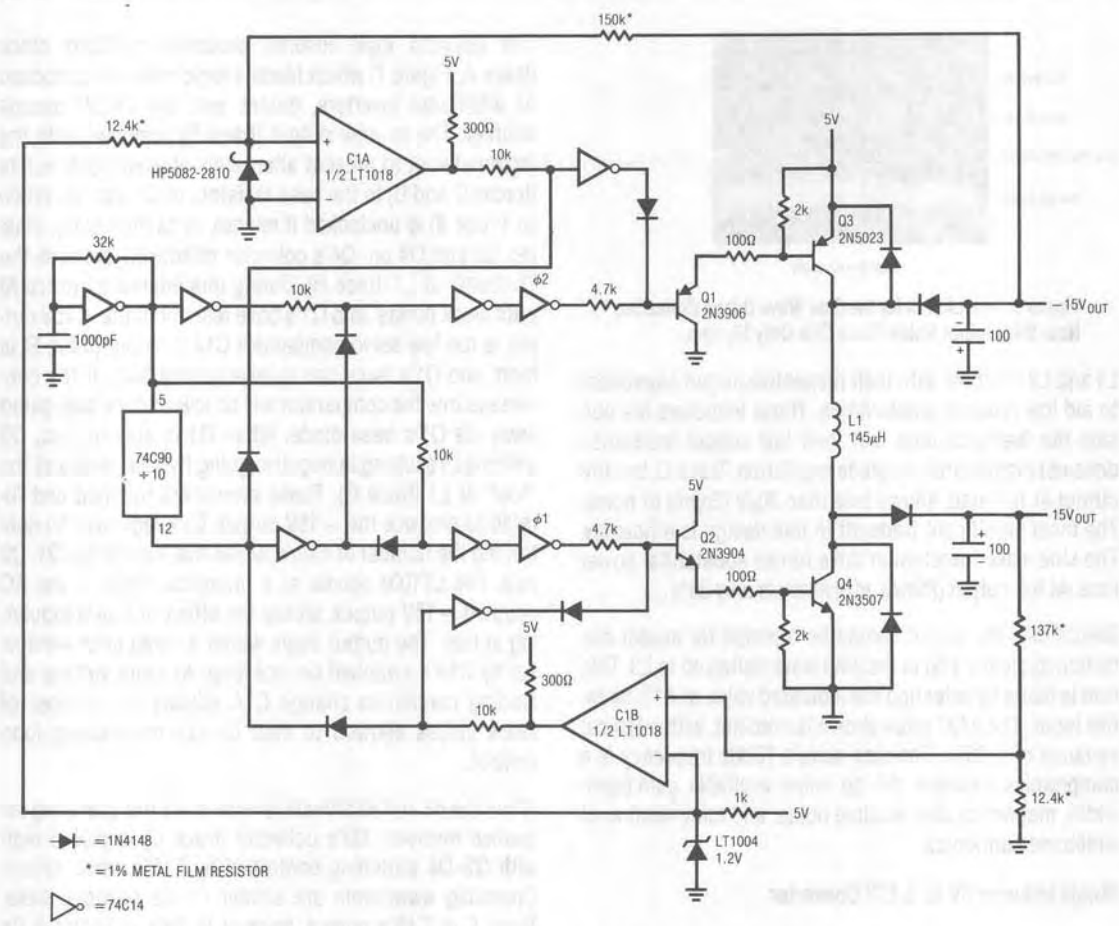


Figure 6. Single Inductor 5V to ± 15V Regulated Converter

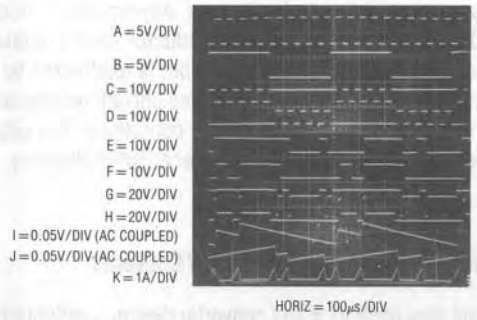


Figure 7. Waveforms for the Single Inductor, Dual-Output, Regulated Converter

Figure 8's design supplies ± 15V outputs at 100mA while consuming only 10mA quiescent current. The LT1070 switching regulator (for a complete description of this device, see Appendix C, "Physiology of the LT1070") drives L1 in flyback mode. A damper network clamps excessive flyback voltages. Flyback events at L1's secondary are half-wave rectified and filtered, producing positive and negative outputs across the 47μF capacitors. The positive 16V output is regulated by a simple loop. Comparator C1A balances a sample of the positive output with a 2.5V reference obtained from the LT1020. When the 16V output (trace A, Figure 9) is too low, C1A switches (trace B) high, turning off the 4N46 opto-isolator. Q1 goes off, and the

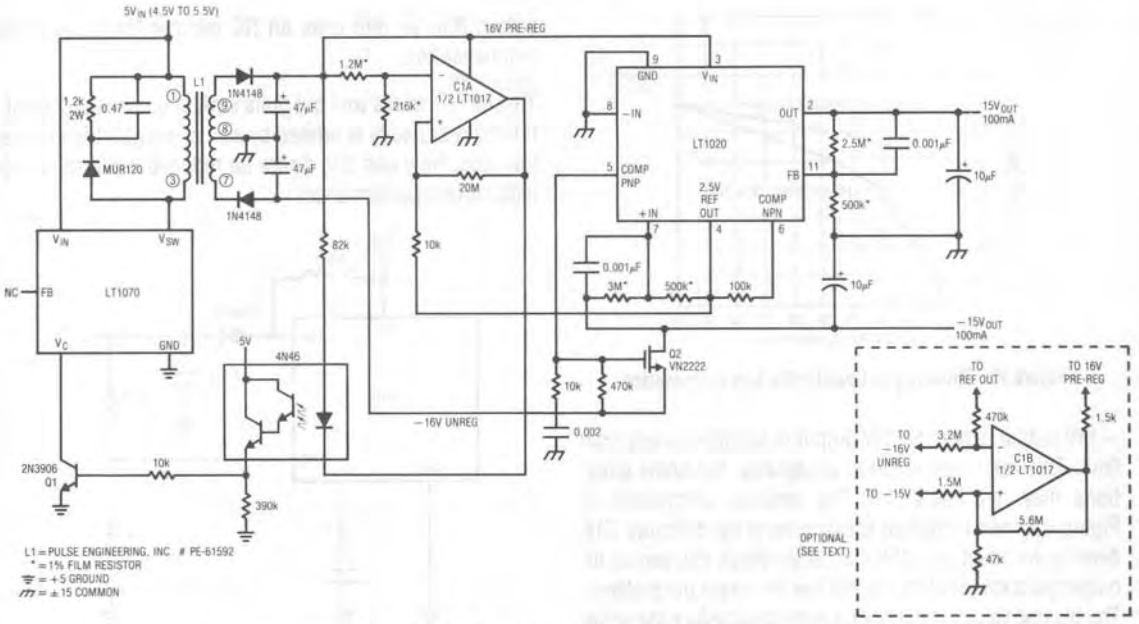


Figure 8. Low I_Q, Isolated 5V to ±15V Converter

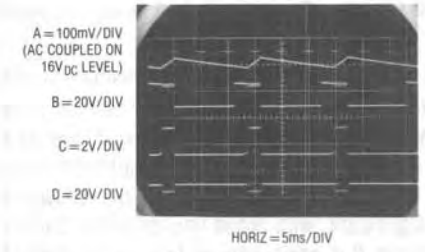


Figure 9. Waveforms for the Low I_Q 5V to ±15V Converter

LT1070's control pin (V_C) pulls high (trace C). This causes full duty cycle 40kHz switching at the V_{SW} pin (trace D). The resultant energy into L1 forces the 16V output to ramp quickly positive, turning off C1A's output. The 20M value combined with the 4N46's slow response (note the delay between C1A going high and the V_C pin rise) gives about 40mV of hysteresis. The LT1070's on-off duty cycle is load dependent, saving significant power when the converter is lightly loaded. This characteristic is largely responsible for the 10mA quiescent current. The opto-isolator preserves the converters input-output isolation. The LT1020, a low quiescent current regulator with low drop-out, further regulates the 16V line, giving the 15V output. The linear regulation eliminates the 40mV ripple and improves transient response. The –16V output tends to follow the regulated –16V line, but regulation is poor. The LT1020's auxiliary on-board comparator is compensated to function as an op amp by the RC damper at pin 5. This amplifier linearly regulates the –16V line. MOSFET Q2 provides low drop-out current boost, sourcing the –15V output. The –15V output is stabilized with the op amp by comparing it with the 2.5V reference via the 500K — 3M current summing resistors. 1000pF capacitors frequency compensate each regulating loop. This converter functions well, providing ±15V outputs at 100mA with only 10mA quiescent current. Figure 10 plots efficiency vs. a conventional design over a range of loads. For high loads results are comparable, but the low quiescent circuit is superior at lower current.

A possible problem with this circuit is related to the poor regulation of the –16V line. If the positive output is lightly loaded L1's magnetic flux is low. Heavy negative output loading under this condition results in the –16V line falling below its output regulators drop-out value. Specifically, with no load on the 15V output only 20mA is available from the –15V output. The full 100mA is only available from the

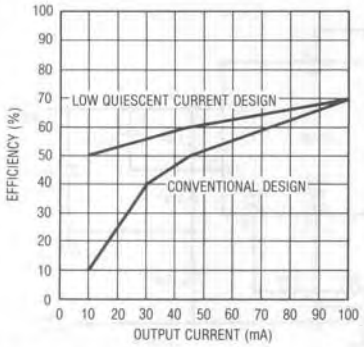


Figure 10. Efficiency vs Load for the Low I_Q Converter

– 15V output when the 15V output is supplying more than 8mA. This restriction is often acceptable, but some situations may not tolerate it. The optional connection in Figure 8 (shown in dashed lines) corrects the difficulty. C1B detects the onset of – 16V line decay. When this occurs its output pulls low, loading the 16V line to correct the problem. The biasing values given permit correction before the negative linear regulator drops out.

MICROPOWER QUIESCENT CURRENT CONVERTERS

Many battery powered applications require very wide ranges of power supply output current. Normal conditions require currents in the ampere range, while standby or "sleep" modes draw only microamperes. A typical lap top computer may draw 1 to 2 amperes running while needing only a few hundred microamps for memory when turned off. In theory, any DC-DC converter designed for loop stability under no-load conditions will work. In practice, a converter's relatively large quiescent current may cause unacceptable battery drain during low output current intervals.

Figure 11 shows a typical flyback based converter. In this case the 6V battery is converted to a 12V output by the inductive flyback voltage produced each time the LT1070's V_{SW} pin is internally switched to ground (for commentary on inductor selection in flyback converters see Appendix D, "Inductor Selection for Flyback Converters"). An internal 40kHz clock produces a flyback event every 25μs. The energy in this event is controlled by the IC's internal error amplifier, which acts to force the feedback (FB) pin to a 1.23V reference. The error amplifiers high impedance output (the V_C pin) uses an RC damper for stable loop compensation.

This circuit works well but pulls 9mA of quiescent current. If battery capacity is limited by size or weight this may be too high. How can this figure be reduced while retaining high current performance?

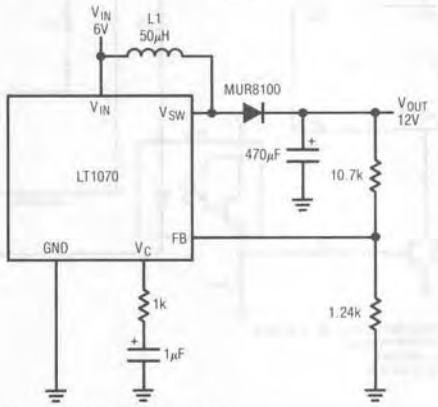


Figure 11. 6V to 12V, 2 Amp Converter with 9mA Quiescent Current

A solution is suggested by considering an auxiliary V_C pin function. If the V_C pin is pulled within 150mV of ground the IC shuts down, pulling only 50 microamperes. Figure 12's special loop exploits this feature, reducing quiescent current to only 150 microamperes. The technique shown is particularly significant, with broad implication in battery powered systems. It is easily applied to a wide variety of DC-DC converters, meeting an acknowledged need across a wide spectrum of applications.

Figure 12's signal flow is similar to Figure 11, but additional circuitry appears between the feedback divider and the V_C pin. The LT1070's internal feedback amplifier and reference are not used. Figure 13 shows operating waveforms under no load conditions. The 12V output (trace A) ramps down over a period of seconds. During this time comparator A1's output (trace B) is low, as are the 74C04 paralleled inverters. This pulls the V_C pin (trace C) low, putting the IC in its 50μA shutdown mode. The V_{SW} pin (trace D) is high, and no inductor current flows. When the 12V output drops about 20mV, A1 triggers and the inverters go high, pulling the V_C pin up and turning on the

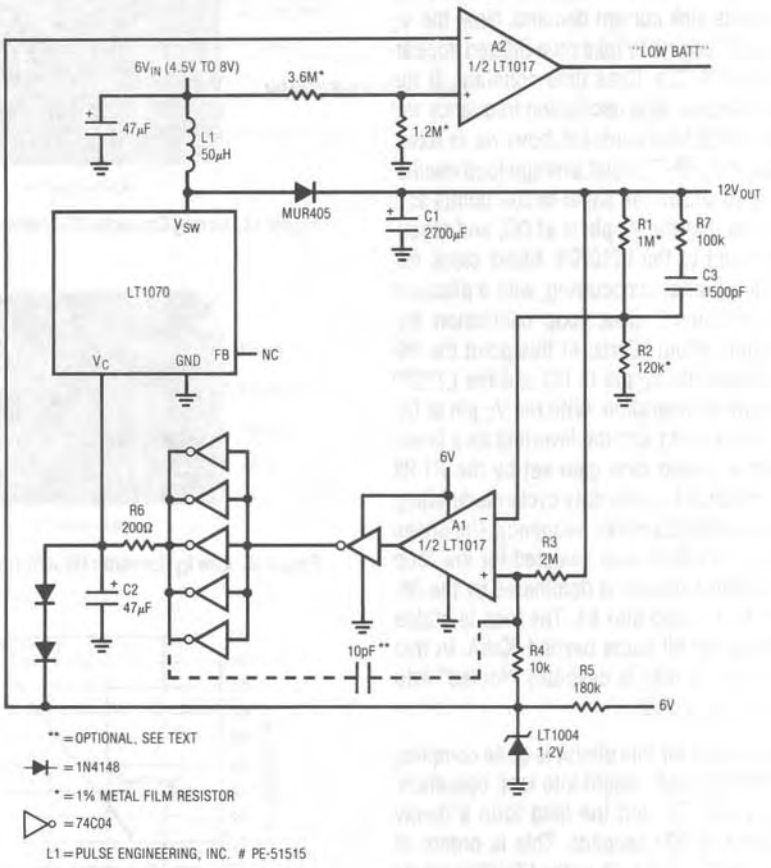


Figure 12. 6V to 12V, 2 Amp Converter with 150μA Quiescent Current

regulator. The V_{SW} pin pulses the inductor at the 40kHz clock rate, causing the output to abruptly rise. This action trips A1 low, forcing the V_C pin back into shutdown. This "bang-bang" control loop keeps the 12V output within the 20mV ramp hysteresis window set by R3-R4. Diode clamps prevent V_C pin overdrive. Note that the loop oscillation period of 4-5 seconds means the R6-C2 time constant at V_C is not a significant term. Because the LT1070 spends almost all of the time in shutdown, very little quiescent current (150μA) is drawn.

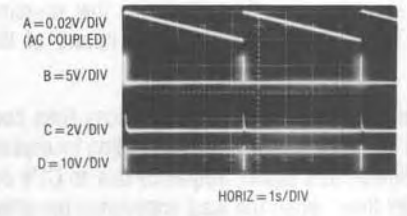


Figure 13. Low I_Q Converter Waveforms with No Load (Traces B and D Retouched for Clarity)

Figure 14 shows the same waveforms with the load increased to 3mA. Loop oscillation frequency increases to keep up with the loads sink current demand. Now, the V_C pin waveform (trace C) begins to take on a filtered appearance. This is due to R6-C2's 10ms time constant. If the load continues to increase, loop oscillation frequency will also increase. The R6-C2 time constant, however, is fixed. Beyond some frequency, R6-C2 must average loop oscillations to DC. Figure 15 shows the same circuit points at 1 ampere loading. Note that the V_C pin is at DC, and repetition rate has increased to the LT1070's 40kHz clock frequency. Figure 16 plots what is occurring, with a pleasant surprise. As output current rises, loop oscillation frequency also rises until about 500Hz. At this point the R6-C2 time constant filters the V_C pin to DC and the LT1070 transitions into "normal" operation. With the V_C pin at DC it is convenient to think of A1 and the inverters as a linear error amplifier with a closed loop gain set by the R1-R2 feedback divider. In fact, A1 is still duty cycle modulating, but at a rate far above R6-C2's break frequency. The phase error contributed by C1 (which was selected for low loop frequency at low output currents) is dominated by the R6-C2 roll off and the R7-C3 lead into A1. The loop is stable and responds linearly for all loads beyond 80mA. In this high current region the LT1070 is desirably "fooled" into behaving like Figure 11's circuit.

A formal stability analysis for this circuit is quite complex, but some simplifications lend insight into loop operation. At 100μA loading (120kΩ) C1 and the load form a decay time constant exceeding 300 seconds. This is orders of magnitude larger than R7-C3, R6-C2, or the LT1070's 40kHz commutation rate. As a result, C1 dominates the loop. Wideband A1 sees phase shifted feedback, and very low frequency oscillations similar to Figure 13's occur[1]. Although C1's *decay* time constant is long, its *charge* time constant is short because the circuit has low sourcing impedance. This accounts for the ramp nature of the oscillations.

Increased loading reduces the C1-load decay time constant. Figure 16's plot reflects this. As loading increases, the loop oscillates at a higher frequency due to C1's decreased decay time. When the load impedance becomes low enough C1's decay time constant ceases to dominate the loop. This point is almost entirely determined by R6 and C2. Once R6 and C2 "take over" as the dominant time constant the loop begins to behave like a linear system. In this region (e.g. above about 75mA, per Figure 16) the LT1070 runs continuously at its 40kHz rate. Now, the R7-C3 time constant becomes significant, performing as a simple feedback lead[2] to smooth output response. There is a fundamental trade-off in the selection of the R7-C3 lead network values. When the converter is running in its linear

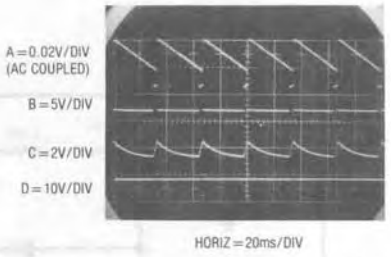


Figure 14. Low I_Q Converter Waveforms at Light Loading

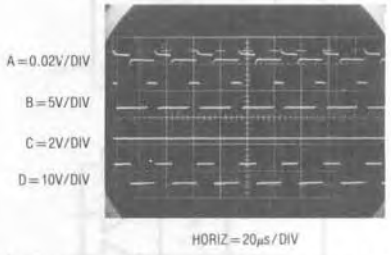


Figure 15. Low I_Q Converter Waveforms at 1 Amp Loading

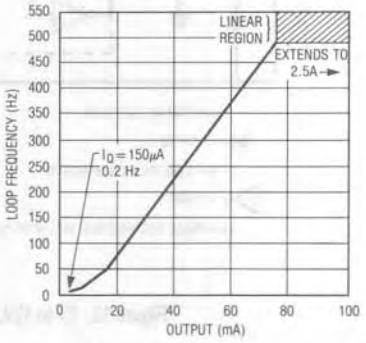


Figure 16. Figure 12's Loop Frequency vs Output Current. Note Linear Loop Operation Above 80mA.

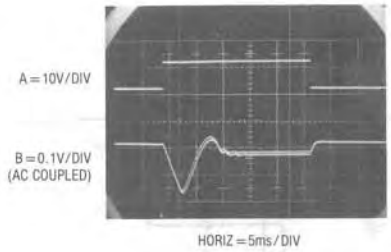


Figure 17. Load Transient Response for Figure 12's Low I_Q Regulator

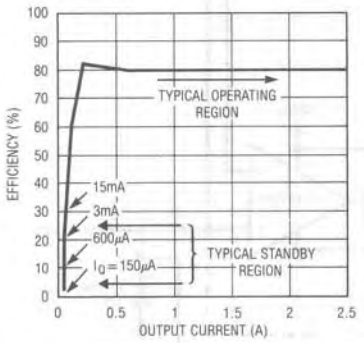


Figure 18. Efficiency vs Output Current for Figure 12. Standby Efficiency is Poor, But Power Loss Approaches Battery Self-Discharge.

region they must dominate the DC hysteresis deliberately generated by R3-R4. As such, they have been chosen for the best compromise between output ripple at high load and loop transient response.

Despite the complex dynamics transient response is quite good. Figure 17 shows performance for a step from no load to 1 ampere. When trace A goes high a 1 ampere load appears across the output (trace B). Initially, the output sags almost 150mV due to slow loop response time (the R6-C2 pair delay V_C pin response). When the LT1070 comes on (signaled by the 40kHz "fuzz" at the bottom extreme of trace B) response is reasonably quick and surprisingly well behaved considering circuit dynamics. The multi-time constant decay[3] ("rattling" is perhaps more appropriate) is visible as trace B approaches steady state between the 4th and 5th vertical divisions.

A2 functions as a simple low battery detector, pulling low when V_{IN} drops below 4.8V.

Figure 18 plots efficiency vs. output current. High power efficiency is similar to standard converters. Low power efficiency is somewhat better, although poor in the lowest ranges. This is not particularly bothersome, as *power* loss is very small.

This loop provides a controlled, conditional instability instead of the more usually desirable (and often elusive) unconditional stability. This deliberately introduced characteristic lowers converter quiescent current by a factor of 60 without sacrificing high power performance. Although demonstrated in a boost converter, it is readily exportable to other configurations. Figure 19A's step down (buck mode) configuration uses the same basic loop with almost no component changes. P-channel MOSFET Q1 is driven from the LT1072 (a low power version of the LT1070) to convert 12V to a 5V output. Q2 and Q3 provide current limiting, while Q4 supplies turn off drive to Q1. The lower output voltage mandates slightly different hysteresis biasing than Figure 12, accounting for the 1MΩ value at the comparators positive input. In other respects the loop and its performance are identical. Figure 19B uses the loop in a transformer based multi-output converter. Note that the floating secondaries allow a –12V output to be obtained with a positive voltage regulator.

Low Quiescent Current Micropower 1.5V to 5V Converter

Figure 20 extends our study of low quiescent current converters into the low voltage, micropower domain. In some circumstances, due to space or reliability considerations, it is preferable to operate circuitry from a single 1.5V cell. This eliminates almost all IC's as design candidates. Although it is possible to design circuitry which runs directly

1 Some layouts may require substantial trace area to A1's inputs. In such cases the optional 10pF capacitor shown ensures clean transitions at A1's output.
2 "Zero Compensation" for all you technosnobs out there.
3 Once again, "multi-pole settling" for those who adore jargon.

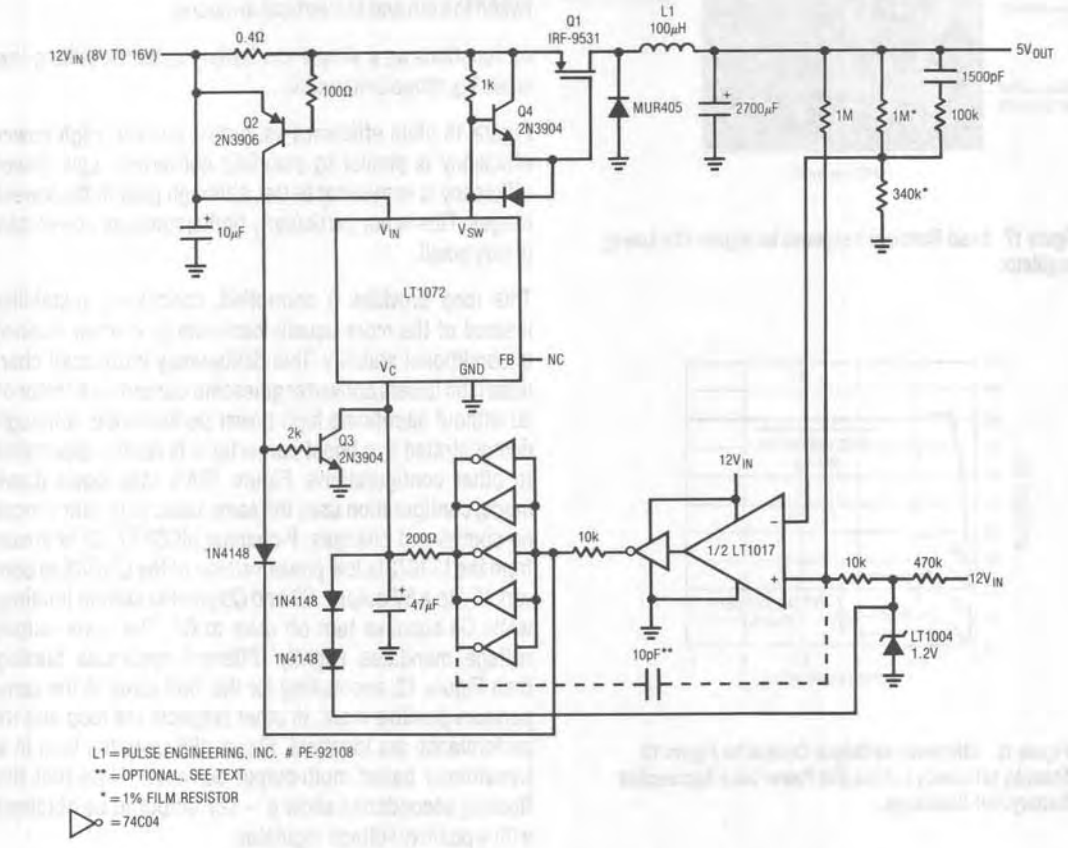


Figure 19A. The Low Quiescent Current Loop Applied to a Buck Converter

from a single cell (see LTC Application Note AN-15, "Circuitry For Single Cell Operation") a DC-DC converter permits using higher voltage IC's. Figure 20's design converts a single 1.5V cell to a 5V output with only 125μA quiescent current. Oscillator C1A's output is a 2kHz square wave (trace D, Figure 21). The configuration is conventional, except that the biasing accommodates the narrow common mode range dictated by the 1.5V supply. To maintain low power, C1A's integrating capacitor is small, with only 50mV of swing. The parallel connected sides of C2 drive L1. When the 5V output (trace A) coasts down far enough C1B goes low (trace B), pulling both C2 positive inputs close to ground. C1A's clock now appears at the paralleled C2 outputs (trace C), forcing energy into L1. The paralleled outputs minimize saturation losses. L1's flyback pulses, rectified and stored in the 47μF capacitor, form the circuits DC output. C1B on-off modulates C2 at whatever duty cycle is required to maintain the circuits 5V output. The LT1004 is the reference, with the resistor divider at C1B's positive input setting the output voltage. Schottky clamping of C2's outputs prevents negative going overdrives due to parasitic L1 behavior.

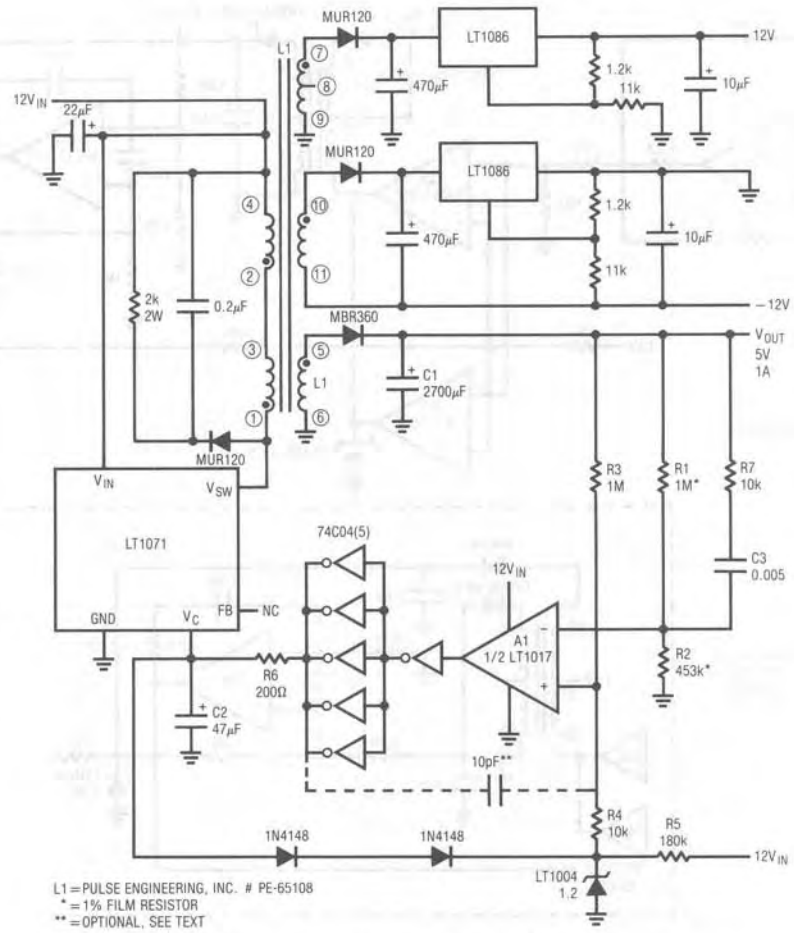


Figure 19B. Multi-Output, Transformer Coupled Low Quiescent Current Converter

The 1.2V LT1004 reference biasing is bootstrapped to the 5V output, permitting circuit operation down to 1.1V. A 10M bleed to supply ensures start-up. The 1M resistors divide down the 1.2V reference, keeping C1B inside common mode limits. C1B's positive feedback RC pair sets about 100mV hysteresis and the 22pF unit suppresses high frequency oscillation.

The micropower comparators and very low duty cycles at light load minimize quiescent current. The 125µA figure noted is quite close to the LT1017's steady state currents. As load increases the duty cycle rises to meet the demand, requiring more battery power. Decrease in battery voltage produces similar behavior. Figure 22 plots available output current vs. battery voltage. Predictably, the highest power is available with a fresh cell (e.g. 1.5V–1.6V), although regulation is maintained down to 1.15V for 250µA loading. The plot shows that the test circuit continued to regulate below this point, but this cannot be relied on in practice (LT1017 V_{MIN} = 1.15V). The low supply voltage makes saturation and other losses in this circuit difficult to control. As such, efficiency is about 50%.

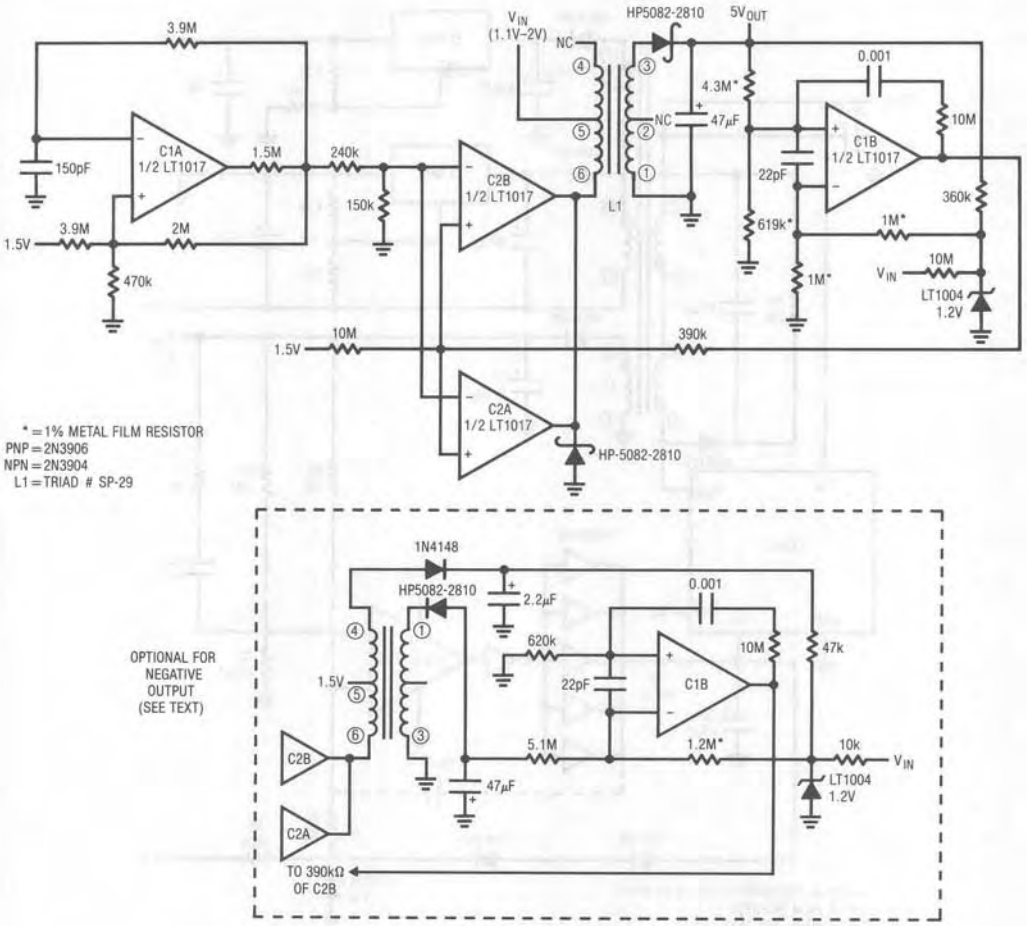


Figure 20. 800μA Output 1.5V to 5V Converter

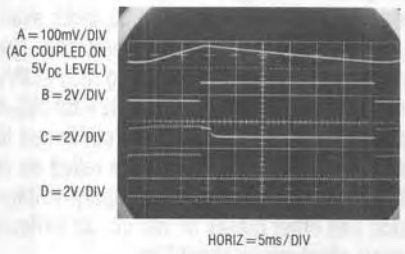


Figure 21. Waveforms for Low Power 1.5V to 5V Converter

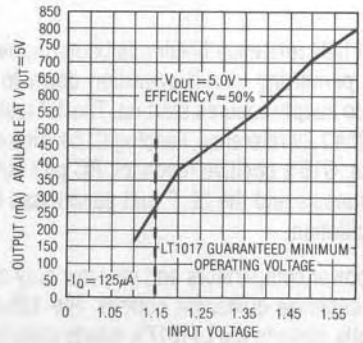


Figure 22. Output Current Capability vs Input Voltage for Figure 20

The optional connection in Figure 20 (shown in dashed lines) takes advantage of the transformers floating secondary to furnish a –5V output. Drive circuitry is identical, but C1B is rearranged as a current summing comparator. The LT1004's bootstrapped positive bias is supplied by L1's primary flyback spikes.

200mA Output 1.5V to 5V Converter

Although useful, the preceding circuit is limited to low power operation. Some 1.5V powered systems (survival 2-way radios, remote, transducer fed data acquisition systems, etc.) require much more power. Figure 23's design supplies a 5V output with 200mA capacity. Some sacrifice in quiescent current is made in this circuit. This is predicated on the assumption that it operates continuously at high power. If lowest quiescent current is necessary the technique detailed back in Figure 12 is applicable.

The circuit is essentially a flyback regulator, similar to Figure 11. The LT1070's low saturation losses and ease of use permit high power operation and design simplicity. Unfortunately, this device has a 3V minimum supply requirement. Bootstrapping its supply pin from the 5V output is possible, but requires some form of start-up mechanism. Dual comparator C1 and the transistors form a start-up loop. When power is applied C1A oscillates (trace A, Figure 24) at 5kHz. Q1 biases, driving Q2's base hard. Q2's collector (trace B) pumps L1, causing voltage step-up flyback events. These events are rectified and stored in the 500µF capacitor, producing the circuits DC output. C1B is set up so it (trace C) goes low when circuit

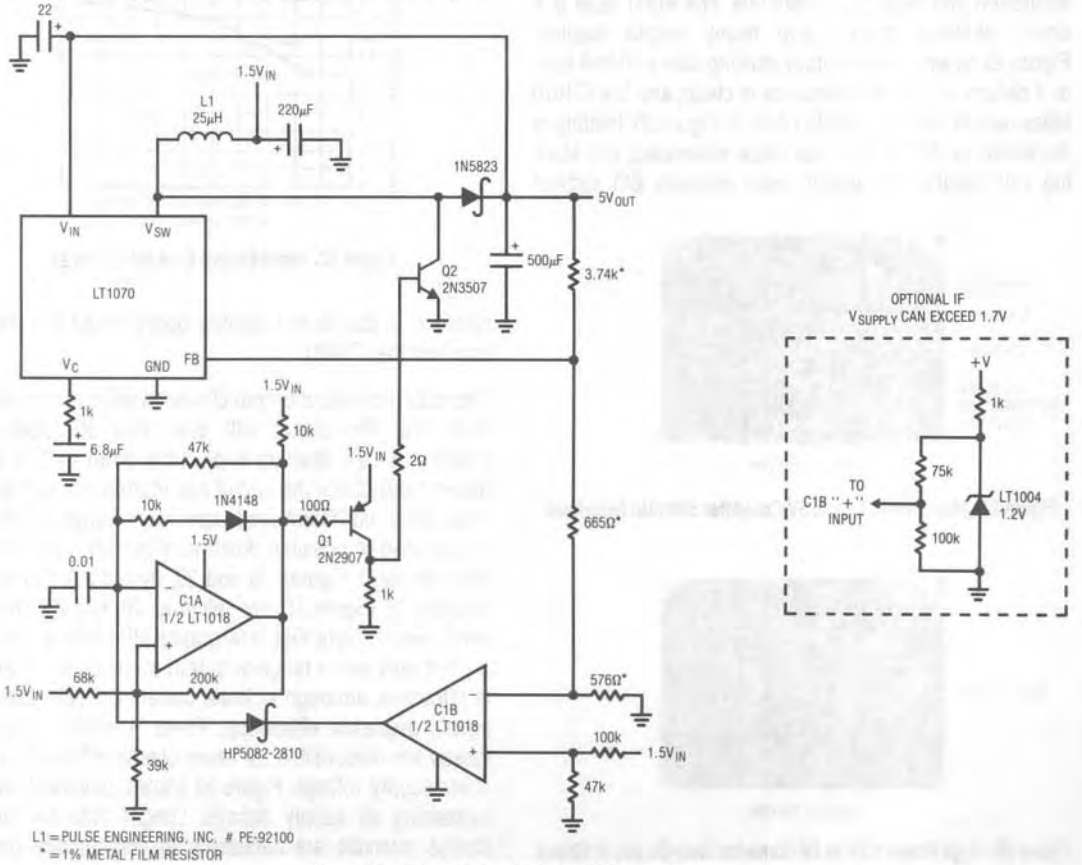


Figure 23. 200mA Output 1.5V to 5V Converter

output crosses about 4.5V. When this occurs C1A's integration capacitor is pulled low, stopping it from oscillating. Under these conditions Q2 can no longer drive L1, but the LT1070 can. This behavior is observable at the LT1070's V_{SW} pin (the junction of L1, Q2's collector and the LT1070), trace D. When the start-up circuit goes off, the LT1070 V_{IN} pin has adequate supply voltage and it begins operation. This occurs at the 4th vertical division of the photograph. There is some overlap between start-up loop turn-off and LT1070 turn-on, but is has no detrimental effect. Once the circuit is running it functions similarly to Figure 11.

The start-up loop must be carefully designed to function over a wide range of loads and battery voltages. Start-up currents exceed 1 ampere, necessitating attention to Q2's saturation and drive characteristics. The worst case is a nearly depleted battery and heavy output loading. Figure 25 shows circuit output starting into a 100mA load at V battery = 1.2V. The sequence is clean, and the LT1070 takes over at the appropriate point. In Figure 26, loading is increased to 200mA. Start-up slope decreases, but starting still occurs. The abrupt slope increase (6th vertical division) is due to overlapping operation of the start-up loop and the LT1070.

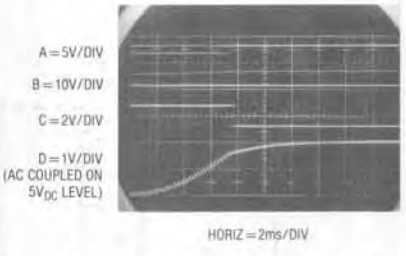


Figure 24. High Power 1.5V to 5V Converter Start-Up Sequence

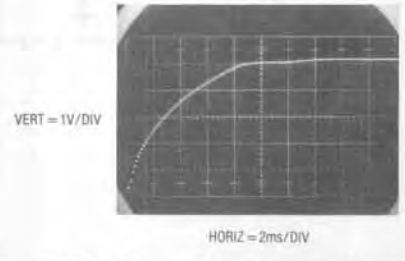


Figure 25. High Power 1.5V to 5V Converter Turn-On Into A 100mA Load at V_{BATT} = 1.2V

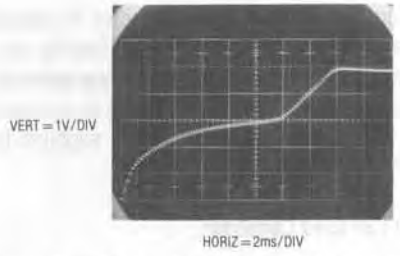


Figure 26. High Power 1.5V to 5V Converter Turn-On Into A 200mA Load at V_{BATT} = 1.2V

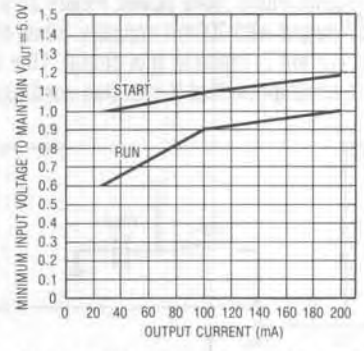


Figure 27. Input-Output Data for Figure 23

Figure 27 plots input-output characteristics for the circuit. Note that the circuit will start into all loads with V battery = 1.2V. Start-up is possible down to 1.0V at reduced loads. Once the circuit has started, the plot shows it will drive full 200mA loads down to V battery = 1.0V. Reduced drive is possible down to V battery = 0.6V (a very dead battery)! Figures 28 and 29, dynamic XY crossplot versions of Figure 27, are taken at 20 and 200 milliamperes, respectively. Figure 30 graphs efficiency at two supply voltages over a range of output currents. Performance is attractive, although at lower currents circuit quiescent power degrades efficiency. Fixed junction saturation losses are responsible for lower overall efficiency at the lower supply voltage. Figure 31 shows quiescent current increasing as supply decays. Longer inductor current charge intervals are necessary to compensate the decreased supply voltage.

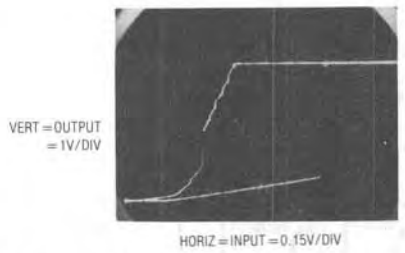


Figure 28. Input-Output XY Characteristics of the 1.5V to 5V Converter at 20mA Loading

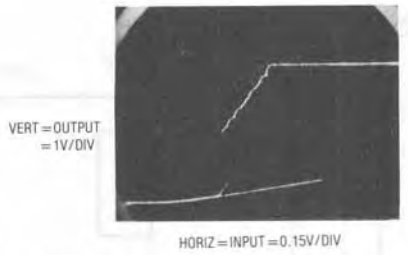


Figure 29. Input-Output XY Characteristics of the 1.5V to 5V Converter at 200mA Loading

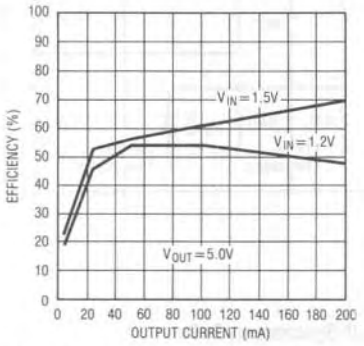


Figure 30. Efficiency vs Operating Point for Figure 23

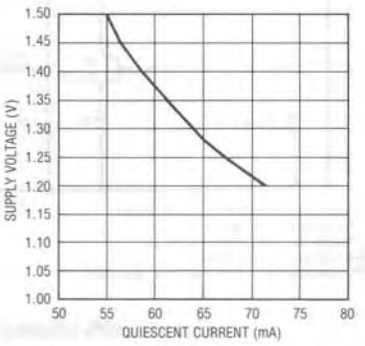


Figure 31. I_Q vs Supply Voltage for Figure 23

HIGH EFFICIENCY CONVERTERS

High Efficiency 12V to 5V Converter

Efficiency is sometimes a prime concern in DC-DC converter design (see Appendix E, "Optimizing Converters for Efficiency"). In particular, small portable computers frequently use a 12V primary supply which must be converted down to 5V. A 12V battery is attractive because it offers long life when all trade-offs and sources of loss are considered. Figure 32 achieves 90% efficiency. This circuit can be recognized as a positive buck converter. Transistor Q1 serves as the pass element. The catch diode is replaced with a synchronous rectifier, Q2, for improved efficiency. The input supply is nominally 12V but can vary from 9.5V to 14.5V. Power losses are minimized by utilizing low source-to-drain resistance, 0.028Ω, NMOS transistors for the catch diode and pass element. The inductor, Pulse Engineering PE-92210K, is made from a low loss core material which squeezes a little more efficiency out of the circuit. Also, keeping the current sense threshold voltage low minimizes the power lost in the current limit circuit.

Figure 33 shows the operating waveforms. Q5 drives the synchronous rectifier, Q2, when the V_{SW} pin (trace A) is turned "off". Q2 is turned off through D1 and D2 when the V_{SW} pin is "on". To turn on Q1, the gate (trace B) must be driven above the input voltage. This is accomplished by bootstrapping the capacitor, C1, off the drain of Q2 (trace C). C1 charges up through D1 when Q2 is turned on. When Q2 is turned off, Q3 is able to conduct, providing a path for C1 to turn Q1 on. During this time current flows through Q1 (trace D), through the inductor (trace E) and into the load. To turn Q1 off, the V_{SW} pin must be "off." Q5 is now able to turn on Q4 and the gate of Q1 is pulled low through D3 and the 50Ω resistor. This resistor is used to reduce the voltage noise generated by fast switching characteristics of Q1. When Q2 is conducting (trace F), Q1

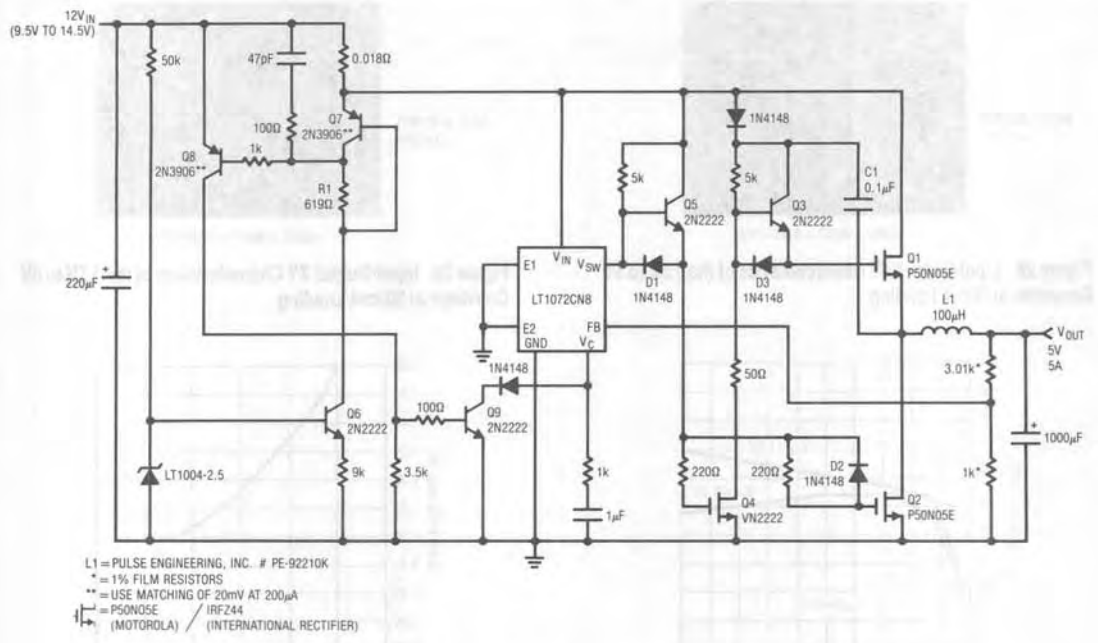


Figure 32. 90% Efficiency Positive Buck Converter with Synchronous Switch

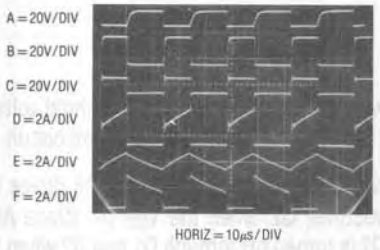


Figure 33. Waveforms for 90% Efficiency Buck Converter

must be off. The efficiency will be decreased if both transistors are conducting at the same time. The 220Ω resistors and D2 are used to minimize the overlap of the switch cycles. Figure 34 shows the efficiency vs. load plot for the circuit as shown. The other plots are for non-synchronously switched buck regulators (see indicated Figures).

Short circuit protection is provided by Q6 through Q9. A 200μA current source is generated from an LT1004, Q6 and the 9k resistor. This current flows through R1 and generates a threshold voltage of 124mV for the comparator, Q7 and Q8. When the voltage drop across the 0.018Ω sense resistor exceeds 124mV, Q8 is turned on. The LT1072's V_{SW} pin goes off when the V_C pin is pulled below 0.9V. This occurs when Q8 forces Q9 to saturate. An RC damper suppresses line transients that might prematurely turn on Q8.

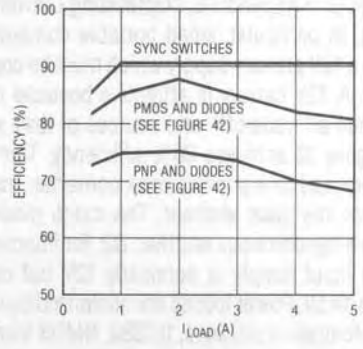
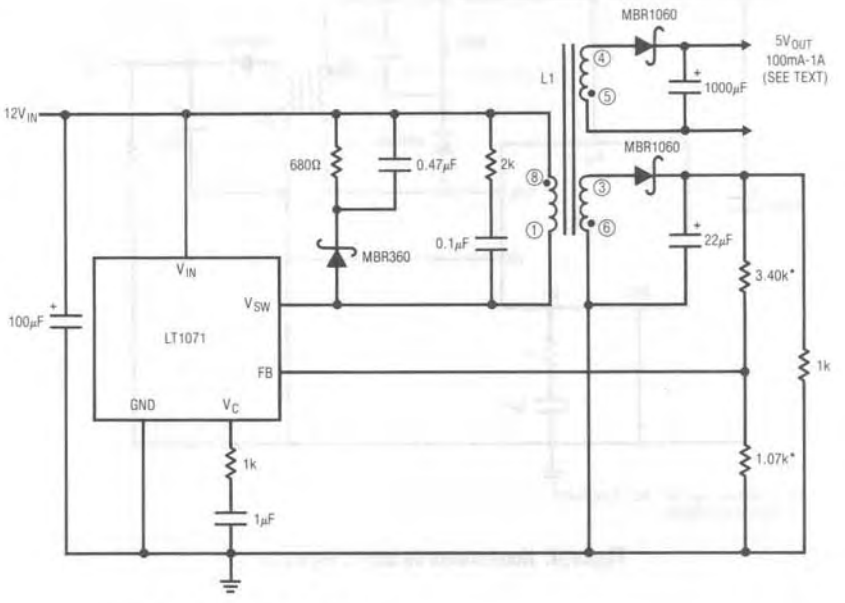


Figure 34. Efficiency vs Load for Figure 32. The Synchronous Switches Give Higher Efficiency than Simple FET or Bipolar Transistors and Diodes.



L1 = PULSE ENGINEERING, INC. # PE-65066
* = 1% FILM RESISTORS
MBR1060 = MOTOROLA

Figure 35. High Efficiency Flux Sensed Isolated Converter

High Efficiency, Flux Sensed Isolated Converter

Figure 35's 75% efficiency is not as good as the previous circuit, but it has a fully floating output. This circuit uses a bifilar wound flux sensing secondary to provide isolated voltage feedback. In operation the LT1070's V_{SW} pin (trace A, Figure 36) pulses L1's primary, producing identical waveforms at the floating power and flux sensing secondaries (traces B and C). Feedback occurs from the flux sense winding via the diode and capacitive filter. The 1k resistor provides a bleed current, while the 3.4k-1.07k divider sets output voltage. The diode partially compensates the diode in the power output winding, resulting in an overall temperature coefficient of about 100ppm/°C. The oversize diode aids efficiency, although significant improvement (e.g. 5%-10%) is possible if synchronous rectification is employed, as in Figure 32. The primary damper network is unremarkable, although the 2k-0.1µF network has been added to suppress excessive ringing at low output current. This ringing is not deleterious to circuit operation, and the network is optional. Below about 10% loading non-ideal transformer behavior introduces significant regulation error. Regulation stays within ±100mV from 10% to 100% of output rating, with excursion exceeding 900mV at no load. Figure 37's circuit trades away isolation for tight regulation with no output loading restrictions. Efficiency is the same.

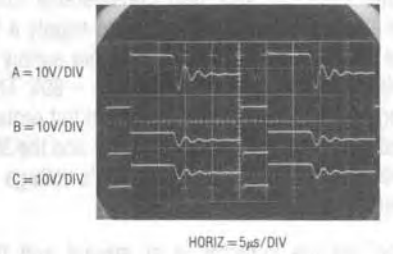


Figure 36. Waveforms for Flux Sensed Converter

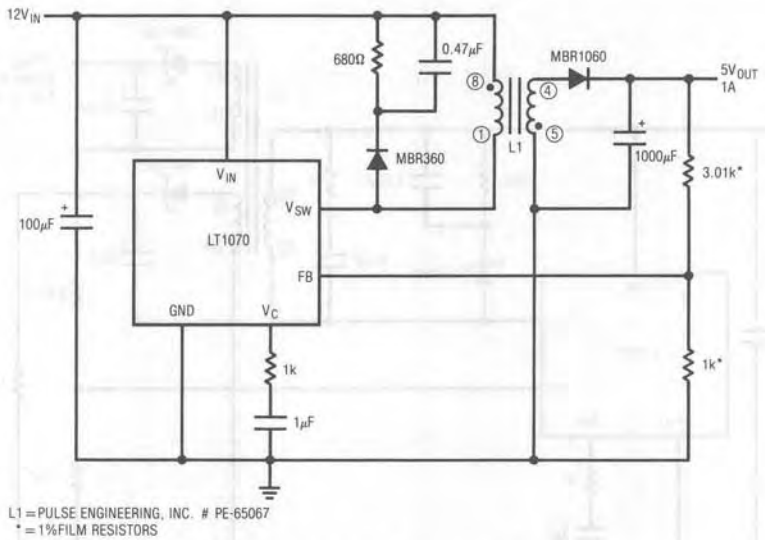


Figure 37. Non-Isolated Version of Figure 35

WIDE RANGE INPUT CONVERTERS

Wide Range Input – 48V to 5V Converter

Often converters must accommodate a wide range of inputs. Telephone lines can vary over considerable tolerances. Figure 38's circuit uses an LT1072 to supply a 5V output from a telecom input. The raw telecom supply is nominally –48V but can vary from –40V to –60V. This range of voltages is acceptable to the V_{SW} pin but protection is required for the V_{IN} pin (V_{MAX} = 60V). Q1 and the 30V zener diode serve this purpose, dropping V_{IN}'s voltage to acceptable levels under all line conditions.

Here, the "top" of the inductor is at ground and the LT1072's ground pin at –V. The feedback pin senses with respect to the ground pin, so a level shift is required from the 5V output. Q2 serves this purpose, introducing only –2mV/°C drift. This is normally not objectionable in a logic supply. It can be compensated with the optional appropriately scaled diode-resistor shown in Figure 38.

Frequency compensation uses an RC damper at the V_C pin. The 68V zener is a type designed to clamp and absorb excessive line transients which might otherwise damage the LT1072 (V_{SW} maximum voltage is 75V).

Figure 39 shows operating waveforms at the V_{SW} pin. Trace A is the voltage and trace B the current. Switching is crisp, with well controlled waveforms. A higher current version of this circuit appears in LTC Application Note AN-25, "Switching Regulators For Poets."

3.5V to 35V_{IN} – 5V_{OUT} Converter

Figure 40's approach has an even wider input range. In this case it produces either a –5V or 5V output (shown in dashed lines). This circuit is an extension of Figure 11's basic flyback topology. The coupled inductor allows the option for buck, boost, or buck-boost converters. This circuit can operate down to 3.5V for battery applications while accepting 35V inputs.

Figure 41 shows the operating waveforms for this circuit. During the V_{SW} (trace A) "on" time, current flows through the primary winding (trace B). No current is transferred to the secondary because the catch diode, D1, is reverse biased. The energy is stored in the magnetic field. When the switch is turned "off" D1 forward biases and the energy is transferred to the secondary winding. Trace C is

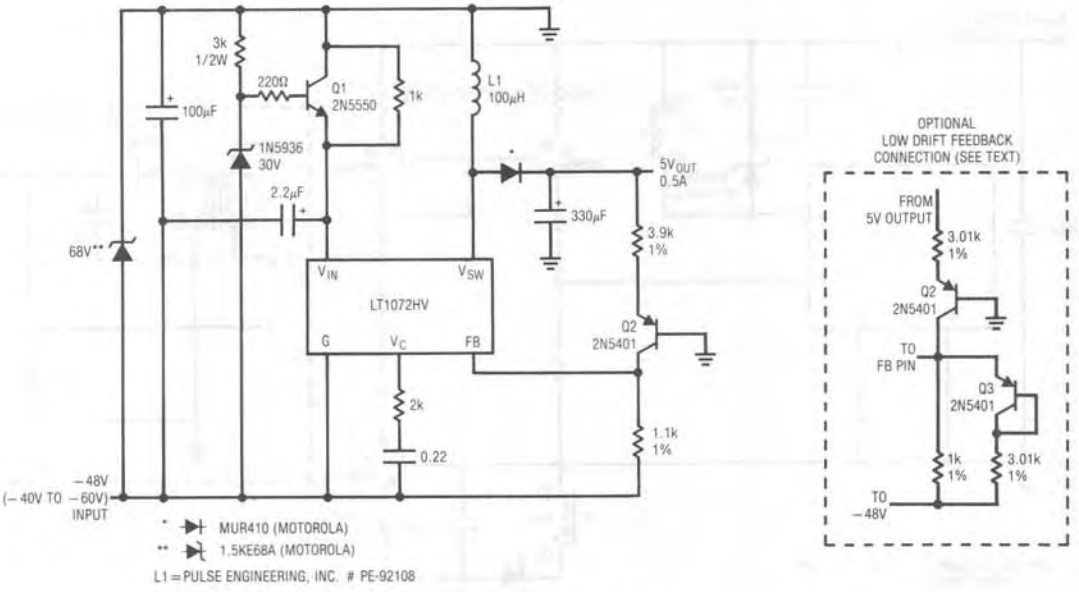


Figure 38. Wide Range Input Converter

the voltage seen on the secondary and trace D is the current flowing through it. This is not an ideal transformer so not all of the primary windings energy is coupled into the secondary. The energy left in the primary winding causes the overvoltage spikes seen on the V_{SW} pin (trace E). This phenomenon is modeled by a leakage inductance term which is placed in series with the primary winding. When the switch is turned "off" current continues to flow in the inductor causing the snubber diode to conduct (trace F). The snubber diode current falls to zero as the inductor loses its energy. The snubber network clamps the voltage spike. When the snubber diode current reaches zero, the V_{SW} pin voltage settles to a potential related to the turns ratio, output voltage and input voltage.[1]

The feedback pin senses with respect to ground, so Q1 through Q3 provides the level shift from the –5V output. Q1 introduces a –2mV/°C drift to the circuit. This effect can be compensated by a circuit similar to the one shown in Figure 38. Line regulation is degraded due to Q3's output impedance. If this is a problem, an op amp must be used to perform the level shift (see AN-19, Figure 29).

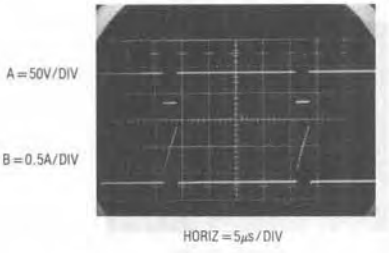


Figure 39. Waveforms for Wide Range Input Converter

Wide Range Input Positive Buck Converter

Figure 42 is another example of a positive buck converter. This is a simpler version compared to the synchronous switch buck, Figure 32. However, efficiency isn't as high (see Figure 34). If the PMOS transistor is replaced with a Darlington PNP transistor (shown in dashed lines) efficiency decreases further.

[1] Application Note AN-19, "LT1070 Design Manual," page 25.

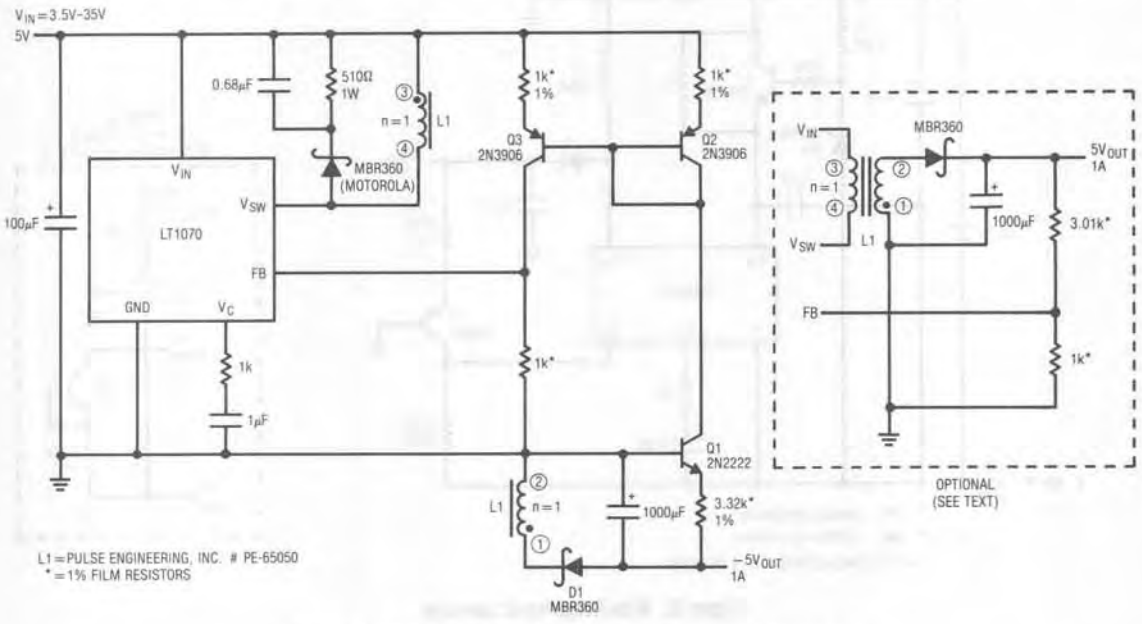


Figure 40. Wide Range Input Positive to Negative Flyback Converter

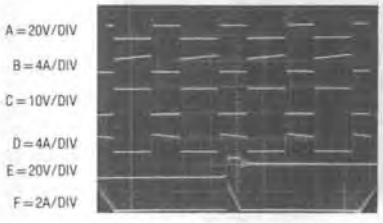


Figure 41. Waveforms for Wide Range Input Positive –5V Output Flyback Converter

Figure 43A shows the operating waveforms for this circuit. The pass transistor's (Q1) drive scheme is similar to the one shown in Figure 32. During the V_{SW} (trace A) "on" time, the gate of the pass transistor is pulled down through D1. This forces Q1 to saturate. Trace B is the voltage seen on the drain of Q1 and trace C is the current passing through Q1. The supply current flows through the inductor (trace D) and into the load. During this time energy is being stored in the inductor. When voltage is applied to the inductor, current does not instantly rise. As the magnetic field builds up, the current builds. This is seen in the inductor current waveform (trace D). When the V_{SW} pin is "off," Q2 is able to conduct and turns Q1 off. Current can no longer flow through Q1, instead D2 is conducting (trace E). During this period some of the energy stored in the inductor will be transferred to the load. Current will be generated from the inductor as long as there is any energy in it. This can be seen in Figure 43A. This is known as continuous mode operation. If the inductor is completely discharged, no current will be generated (see Figure 43B). When this happens neither switch, Q1 or D2, is conducting. The inductor looks like a short and the voltage on the cathode of D2 will settle to the output voltage. These "boingies" can be seen in trace B of Figure 43B. This is known as discontinuous mode operation. Higher input voltages can be handled with the gate-source zener clamped by D2. The 400 milliwatt zener's current must be rescaled by adjusting the 50Ω value. Maximum gate-source voltage is 20V. The circuit will function up to $35V_{IN}$. At inputs beyond 35V all semiconductor breakdown voltages must be considered.

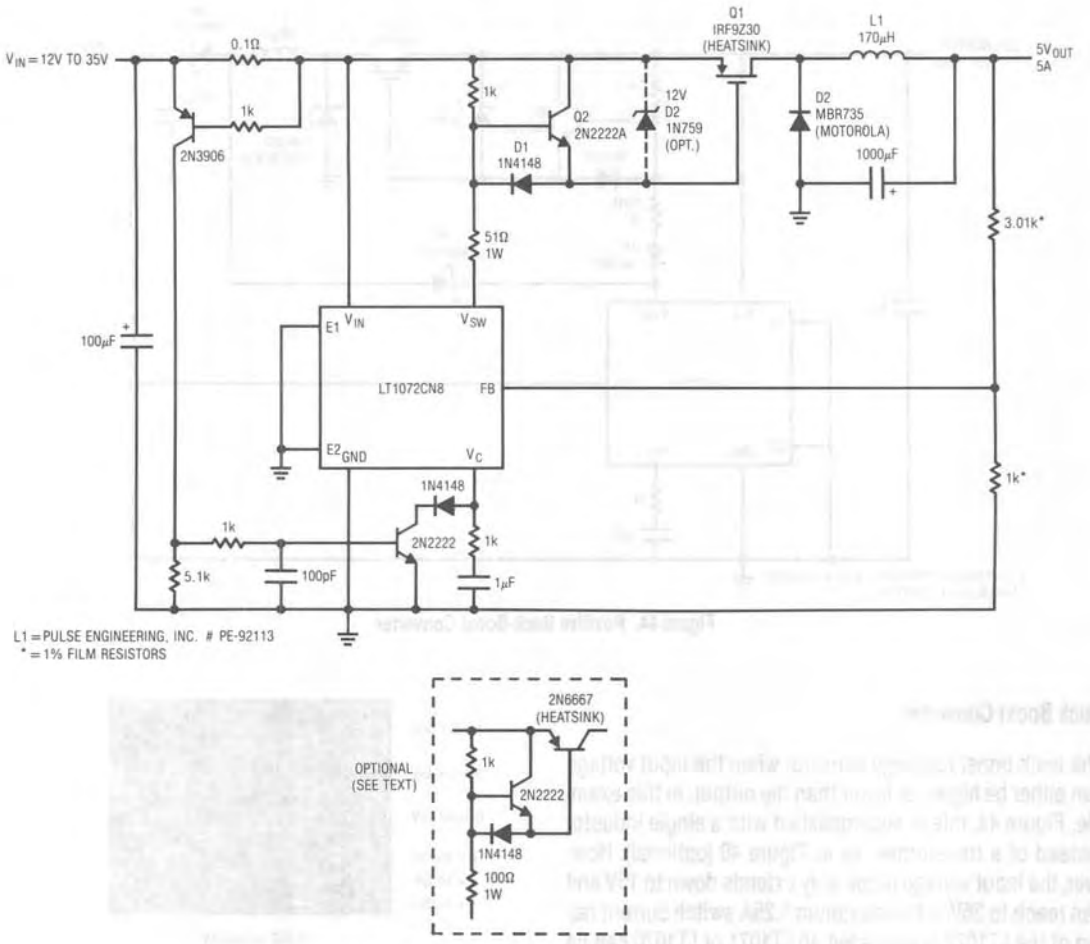


Figure 42. Positive Buck Converter

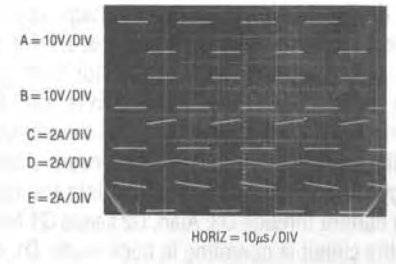


Figure 43A. Waveforms for Wide Range Input Positive Buck Converter (Continuous Mode)

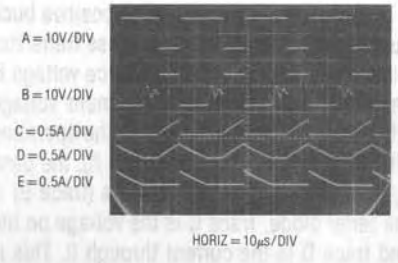


Figure 43B. Waveforms for Wide Range Input Positive Buck Converter (Discontinuous Mode)

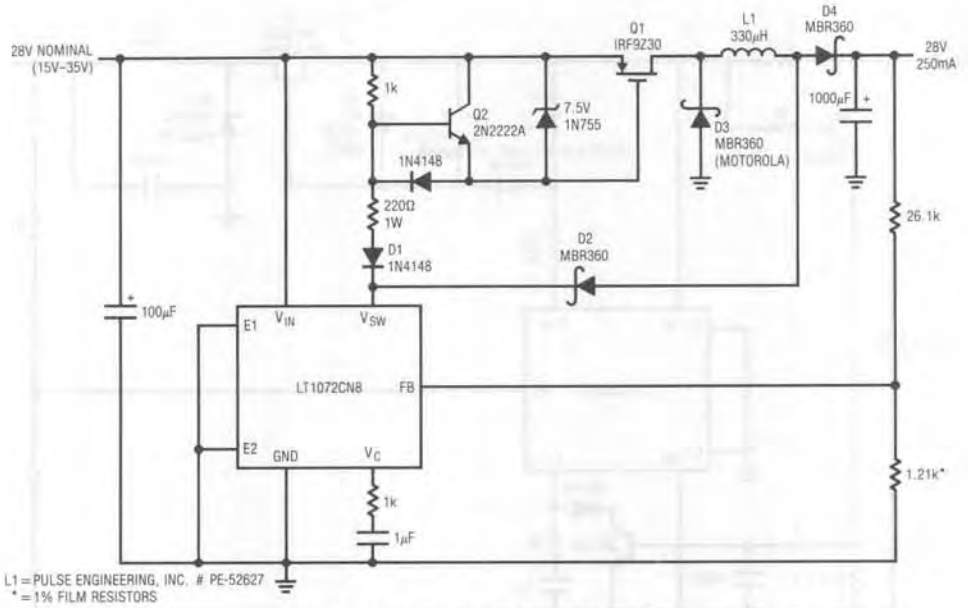


Figure 44. Positive Buck-Boost Converter

Buck Boost Converter

The buck boost topology is useful when the input voltage can either be higher or lower than the output. In this example, Figure 44, this is accomplished with a single inductor instead of a transformer, as in Figure 40 (optional). However, the input voltage range only extends down to 15V and can reach to 35V. If the maximum 1.25A switch current rating of the LT1072 is exceeded an LT1071 or LT1070 can be used instead. At high power levels package thermal characteristics should be considered.

The operation of the circuit is similar to the positive buck converter, Figure 42. The gate drive to the pass transistor is derived the same way except the gate-source voltage is clamped. Remember, the gate-source maximum voltage rating is specified at ±20V. Figure 45 shows the operating waveforms. When the V_{SW} pin is "on" (trace A), the pass transistor, Q1, is saturated. The gate voltage (trace B) is clamped by the zener diode. Trace C is the voltage on the drain of Q1 and trace D is the current through it. This is where the similarities between the two circuits end. Notice the inductor is pulled to within a diode drop, D2, above

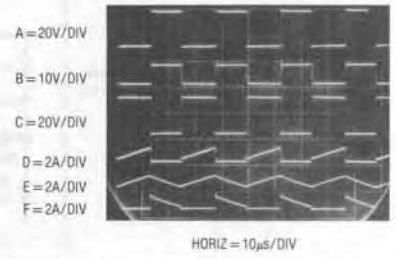


Figure 45. Waveforms for Positive Buck-Boost Converter

ground, instead of being tied to the output (see Figure 42). In this case, the inductor has the input voltage applied across it, except for a Vbe and saturation losses. D4 is reverse biased and blocks the output capacitor from discharging into the V_{SW} pin. When the V_{SW} pin is "off" Q1 and D2 cease to conduct. Since the current in the inductor (trace E) continues to flow, D3 and D4 are forward biased and the energy in the inductor is transferred into the load. Trace F is the current through D3. Also, D2 keeps Q1 from staying on if the circuit is operating in buck mode. D1, on the other hand, blocks current from flowing into the gate drive circuit when operating in boost mode.

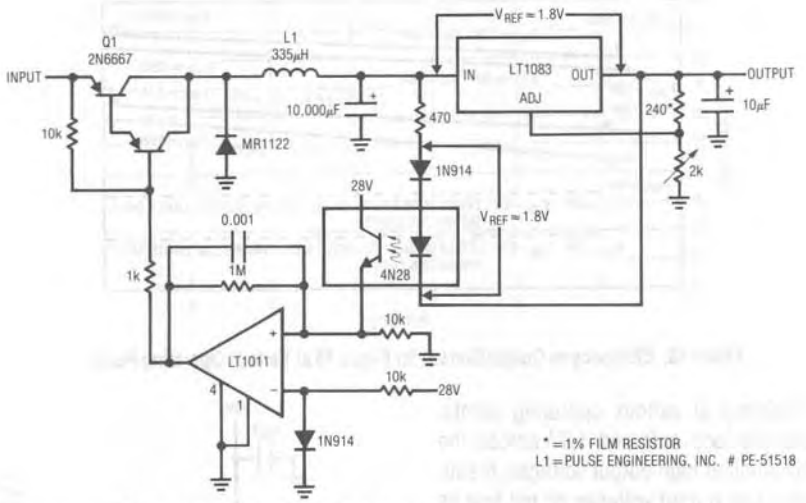


Figure 46. High Power Linear Regulator with Switching Pre-Regulator

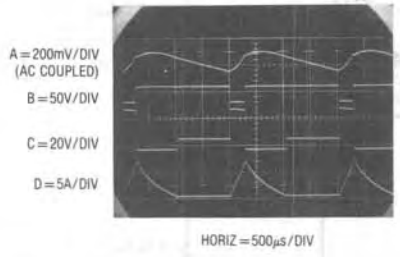


Figure 47. Switching Pre-Regulated Linear Regulators Waveforms

Wide Range Switching Pre-Regulated Linear Regulator

In a sense, linear regulators can be considered extraordinarily wide range DC-DC converters. They do not face the dynamic problems switching regulators encounter under varying ranges of input and output. Excess energy is simply dissipated as heat. This elegantly simplistic energy management mechanism pays dearly in terms of efficiency and temperature rise. Figure 46 shows a way a linear regulator can more efficiently control high power under widely varying input and output conditions.

The regulator is placed within a switched-mode loop that servo-controls the voltage *across* the regulator. In this arrangement the regulator functions normally while the switched-mode control loop maintains the voltage across it at a minimal value, regardless of line, load or output setting changes. Although this approach is not quite as efficient as a classical switching regulator, it offers lower noise and the fast transient response of the linear regulator. The LT1083 functions in the conventional fashion, supplying a regulated output at 7.5A capacity. The remaining components form the switched-mode dissipation limiting control. This loop forces the potential across the LT1083 to equal the 1.8V value of V_{REF}. The opto-isolator furnishes a convenient way to single end the differentially sensed voltage across the LT1083. When the input of the regulator (trace A, Figure 47) decays far enough, the LT1011 output (trace B) switches low, turning on Q1 (Q1 collector is trace C). This allows current flow (trace D) from the circuit input into the 10,000μF capacitor, raising the regulator's input voltage.

When the regulator input rises far enough, the comparator goes high, Q1 cuts off and the capacitor ceases charging. The MR1122 damps the flyback spike of the current limiting inductor. The 0.001μF-1M combination sets loop hysteresis at about 100mVp-p. This free-running oscillation control mode substantially reduces dissipation in the regulator, while preserving its performance. Despite changes in the input voltage, different regulated outputs or load shifts, the loop always ensures minimum dissipation in the regulator.

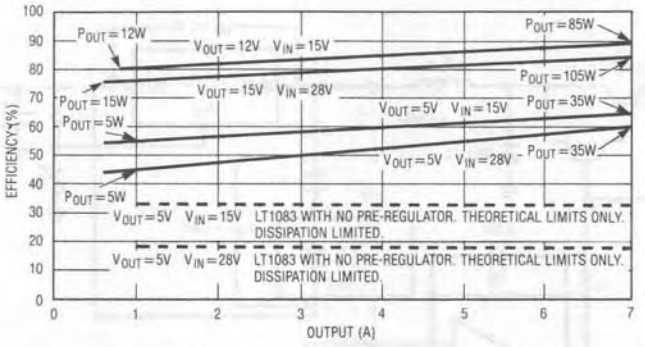


Figure 48. Efficiency vs Output Current for Figure 46 at Various Operating Points

Figure 48 plots efficiency at various operating points. Junction losses and the loop enforced 1.8V across the LT1083 are relatively small at high output voltages, resulting in good efficiency. Low output voltages do not fare as well, but compare very favorably to the theoretical data for the LT1083 with no pre-regulator. At the higher theoretical dissipation levels the LT1083 will shut down, precluding practical operation.

HIGH VOLTAGE CONVERTERS

High Voltage Converter — 1000V_{OUT}, Non-Isolated

Photomultiplier tubes, ion generators, gas based detectors, image intensifiers and other applications need high voltages. Converters frequently supply these potentials. Generally, the limitation on high voltage is transformer insulation breakdown. A transformer is almost always used because a simple inductor forces excessive voltages on the semiconductor switch. Figure 49's circuit, reminiscent of Figure 11's basic flyback configuration, is a 15V to 1000V_{OUT} converter. The LT1072 controls output by modulating the flyback energy into L1, forcing its feedback (FB) pin to 1.23V (the internal reference value). In this example loop compensation is heavily overdamped by the V_C pin capacitor. L1's damper network limits flyback spikes within the V_{SW} pin's 75V rating.

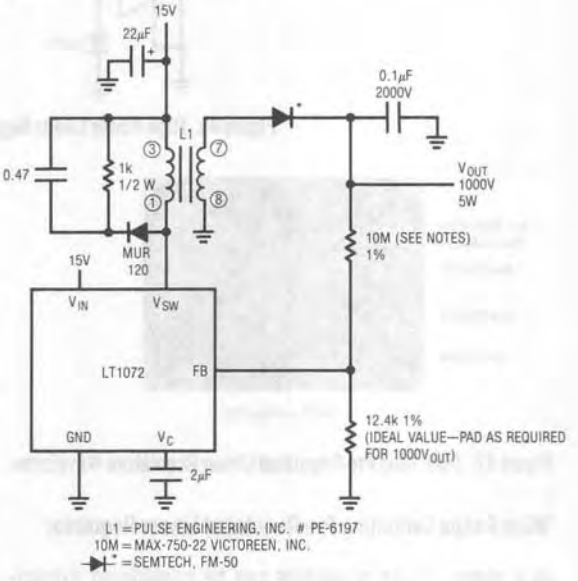


Figure 49. Non-Isolated 15V to 1000V Converter

Fully Floating, 1000V_{OUT} Converter

Figure 50 is similar to Figure 49 but features a fully floating output. This provision allows the output to be referenced off system ground, often desirable for noise or biasing reasons. Basic loop action is as before, except that the LT1072's internal error amplifier and reference are replaced with galvanically isolated equivalents. Power for these components is bootstrapped from the output via source follower Q1 and its 2.2M ballast resistor. A1 and the LT1004, micropower components, minimize dissipation in Q1 and its ballast. Q1's gate bias, tapped from the output divider string, produces about 15V at its source. A1 compares the scaled divider output with the LT1004 reference. The error signal, A1's output, drives the optocoupler.

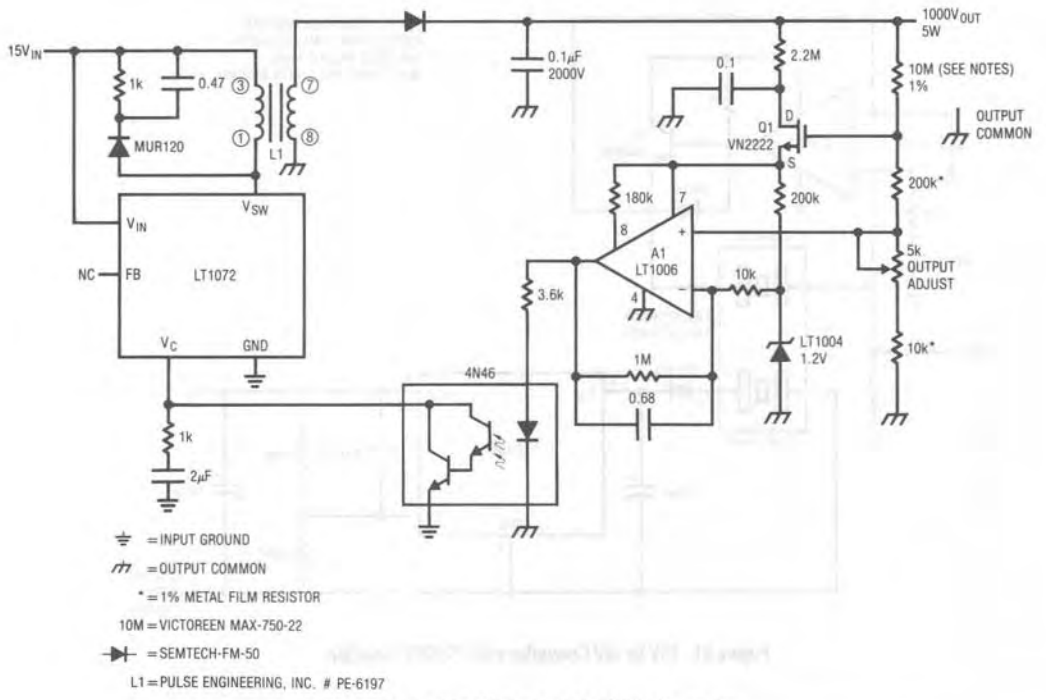


Figure 50. Isolated Output 15V to 1000V Converter

Photocurrent is kept low to save power. The optocoupler output pulls down on the V_C pin, closing a loop. Frequency compensation at the V_C pin and A1 stabilizes the loop.

The transformers isolated secondary and optical feedback produce a regulated, fully galvanically floating output. Common mode voltages of 2000V are acceptable.

20,000V_{CMV} Breakdown Converter

Figure 50's common mode breakdown limits are imposed by transformer and optocoupler restrictions. Isolation amplifiers, transducer measurement at high common mode voltages (e.g. winding temperature of a utility company transformer and ESD sensitive applications) require high breakdowns. Additionally, very precise floating measurements, such as signal conditioning for high impedance bridges, can require extremely low leakage to ground.

Achieving high common mode voltage capability with minimal leakage requires a different approach. Magnetics is usually considered the only approach for isolated transfer of appreciable amounts of electrical energy. Transformer action is, however, achievable in the acoustic domain. Some ceramic materials will transfer electrical energy with galvanic isolation. Conventional magnetic transformers work on an electrical-magnetic-electrical basis using the magnetic domain for electrical isolation. The acoustic transformer uses an acoustic path to get isolation. The high voltage breakdown and low electrical conductance associated with ceramics surpasses isolation characteristics of magnetic approaches. Additionally, the acoustic transformer is simple. A pair of leads bonded to each end of the ceramic material forms the device. Insulation resistance exceeds $10^{12}\Omega$, with primary-secondary capacitances of 1-2pF. The material and its physical configuration determine its resonant frequency. The device may be considered as a high Q resonator, similar to a quartz crystal. As such, drive circuitry excites the device in the positive feedback path of a wideband gain element. Unlike a crystal, drive circuitry is arranged to pass substantial current through the ceramic, maximizing power into the transformer.

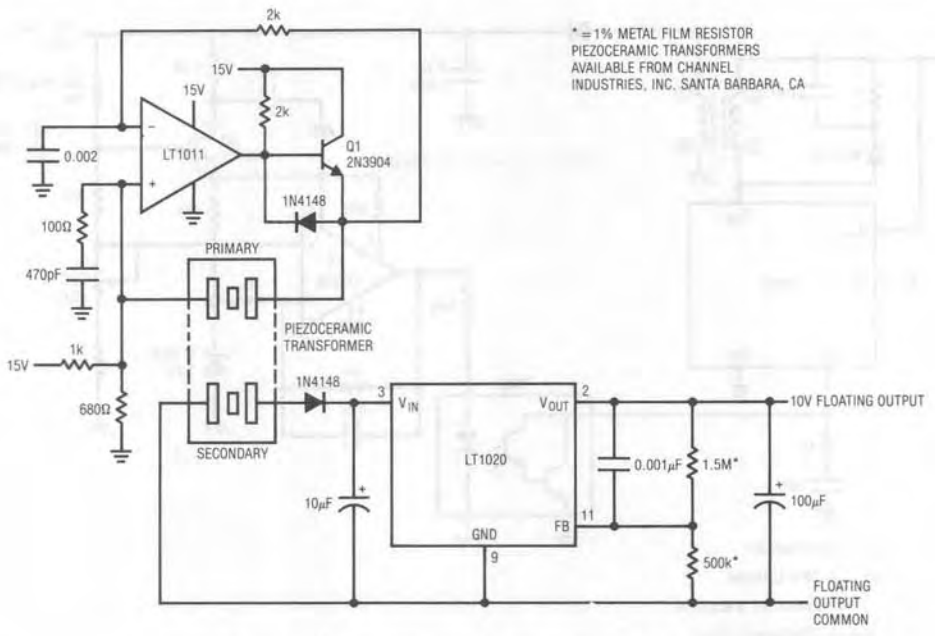


Figure 51. 15V to 10V Converter with 20,000V Isolation

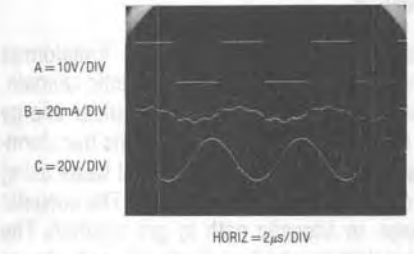


Figure 52. Waveforms for the 20,000V Isolation Converter

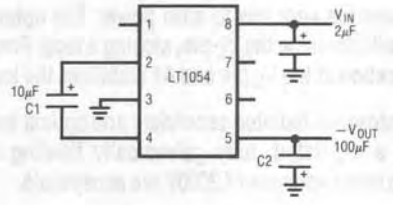


Figure 53. A Basic Switched Capacitor Converter

In Figure 51 the piezo-ceramic transformer is in the LT1011 comparators positive feedback loop. Q1 is an active pull-up for the LT1011, an open collector device. The 2k-0.002μF path biases the negative input. Positive feedback occurs at the transformers resonance, and oscillation commences (trace A, Figure 52 is Q1's emitter). Similar to quartz crystals, the transformer has significant harmonic and overtone modes. The 100Ω-470pF damper suppresses spurious oscillations and "mode hopping."

Drive current (trace B) approximates a sine wave, with peaking at the transitions. The transformer looks like a highly resonant filter to the resultant acoustic wave propagated in it. The secondary voltage (trace C) is sinosodial. Additionally, the transformer has voltage gain. The diode and 10μF capacitor convert the secondary voltage to DC. The LT1020 low quiescent current regulator gives a stabilized 10V output. Output current for the circuit is a few milliamperes. Higher currents are possible with attention to transformer design.

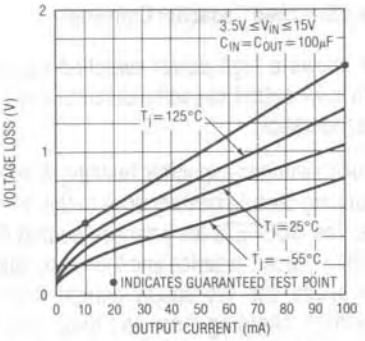


Figure 54. Losses for the Basic Switched Capacitor Converter

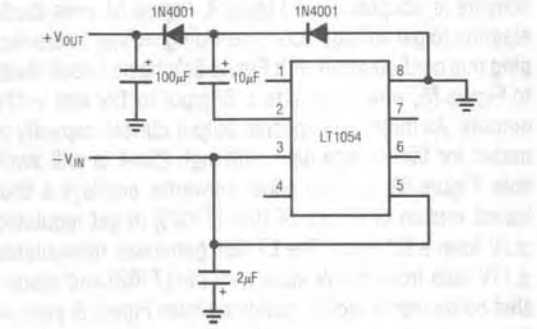


Figure 55. Switched Capacitor – V_{IN} to + V_{OUT} Converter

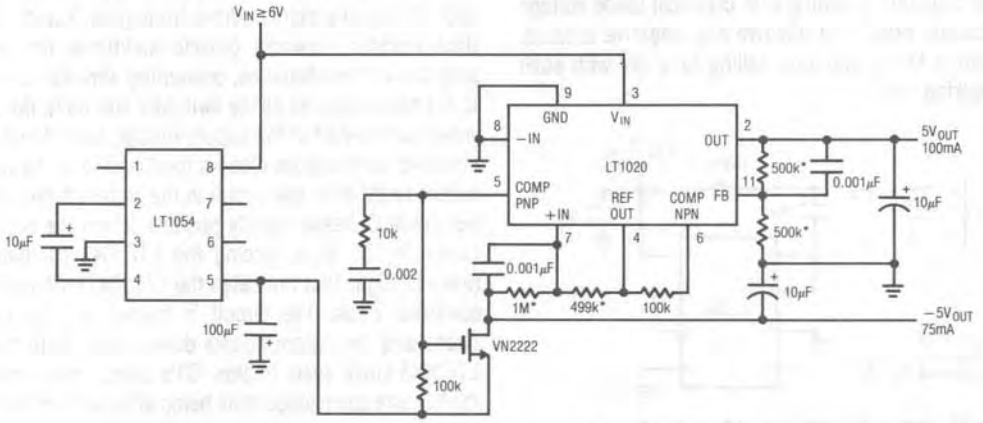


Figure 56. High Current Switched Capacitor 6V to ± 5V Converter

SWITCHED CAPACITOR BASED CONVERTERS

Inductors are used in converters because they can store energy. This stored magnetic energy, released and expressed in electrical terms, is the basis of converter operation. Inductors are not the only way to store energy with efficient release expressed in electrical terms. Capacitors store charge (already an electrical quantity) and as such, can be used as the basis for DC-DC conversion. Figure 53 shows how simple a switched capacitor based converter can be (the fundamentals of switched capacitor based conversion are presented in Appendix B, "Switched Capacitor Voltage Converters — How They Work"). The LT1054 provides clocked drive to charge C1. A second clock phase discharges C1 into C2. The internal switching is arranged so C1 is "flipped" during the discharge interval, producing a negative output at C2. Continuous clocking allows C2 to charge to the same absolute value as C1. Junction and other losses preclude ideal results, but performance is quite good. This circuit will convert V_{IN} to $-V_{OUT}$ with losses shown in Figure 54. Adding an external resistive divider allows regulated output (see Appendix B).

With some additional steering diodes this configuration can effectively run "backwards" (Figure 55), converting a negative input to a positive output. Figure 56's variant gives low dropout linear regulation for 5V and –5V outputs from $6V_{IN}$. The LT1020 based dual output regulation

scheme is adapted from Figure 8. Figure 57 uses diode steering to get voltage boost, providing $\approx 2V_{IN}$. Bootstrapping this configuration with Figure 54's basic circuit leads to Figure 58, which converts a 5V input to 12V and −12V outputs. As might be expected output current capacity is traded for the voltage gain, although 25mA is still available. Figure 59, another boost converter, employs a dedicated version of Figure 58 (the LT1026) to get regulated ±7V from a 6V input. The LT1026 generates unregulated ±11V rails from the 6V input with the LT1020 and associated components (again, purloined from Figure 8) producing regulation. Current and boost capacity are reduced from Figure 58's levels, but the regulation and simplicity are noteworthy. Figure 60 combines the LT1054's clocked switched capacitor charging with classical diode voltage multiplication, producing positive and negative outputs. At no load ±13V is available, falling to ±10V with each side supplying 10mA.

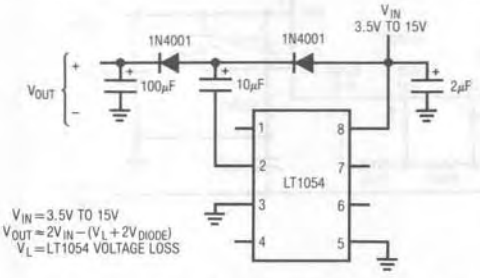


Figure 57. Voltage Boost Switched Capacitor Converter

High Power Switched Capacitor Converter

Figure 61 shows a high power switched capacitor converter with a 1A output capacity. Discrete devices permit high power operation.

The LTC1043 switched-capacitor building block provides non-overlapping complementary drive to the Q1-Q4 power MOSFETs. The MOSFETs are arranged so that C1 and C2 are alternately placed in series and then in parallel. During the series phase, the 12V supply current flows through both capacitors, charging them and furnishing load current. During the parallel phase, both capacitors deliver current to the load. Traces A and B, Figure 62, are the LTC1043-supplied drives to Q3 and Q4, respectively. Q1 and Q2 receive similar drive from pins 3 and 11. The diode-resistor networks provide additional non-overlapping drive characteristics, preventing simultaneous drive to the series-parallel phase switches. Normally, the output would be one-half of the supply voltage, but C1 and its associated components close a feedback loop, forcing the output to 5V. With the circuit in the series phase, the output (trace C) heads rapidly positive. When the output exceeds 5V, C1 trips, forcing the LTC1043 oscillator pin (trace D) high. This truncates the LTC1043's triangle wave oscillator cycle. The circuit is forced into the parallel phase and the output coasts down slowly until the next LTC1043 clock cycle begins. C1's output diode prevents the triangle down-slope from being affected and the 100pF capacitor provides sharp transitions. The loop regulates

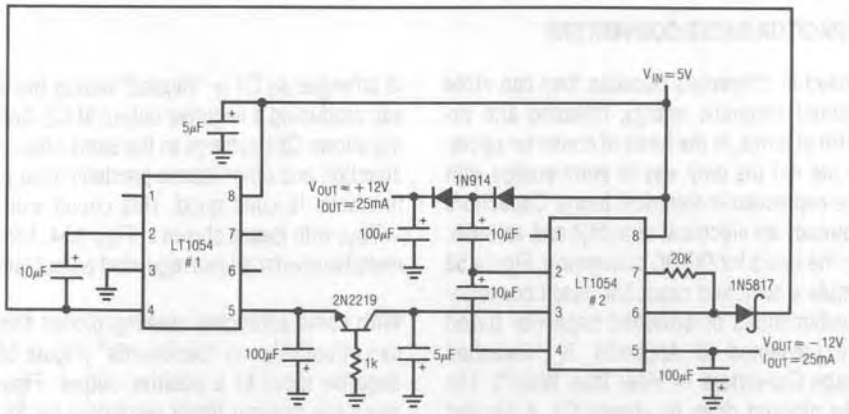


Figure 58. Switched Capacitor 5V to ±12V Converter

the output to 5V by feedback controlling the turn-off point of the series phase. The circuit constitutes a large scale switched-capacitor voltage divider which is never allowed to complete a full cycle. The high transient currents are easily handled by the power MOSFETs and overall efficiency is 83%.

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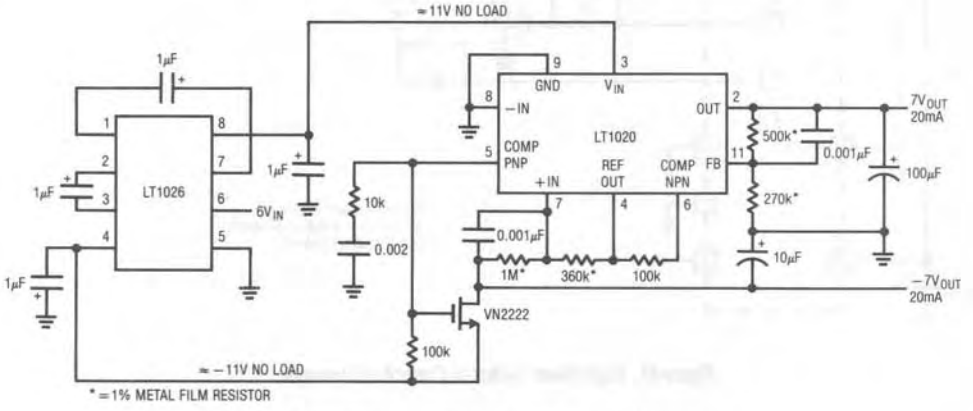

Figure 59. Switched Capacitor Based 6V to ±7V Converter

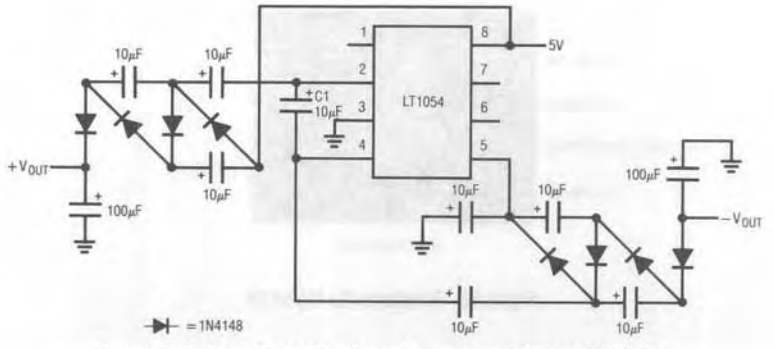

Figure 60. Switched Capacitor Charge Pump Based Voltage Multiplier

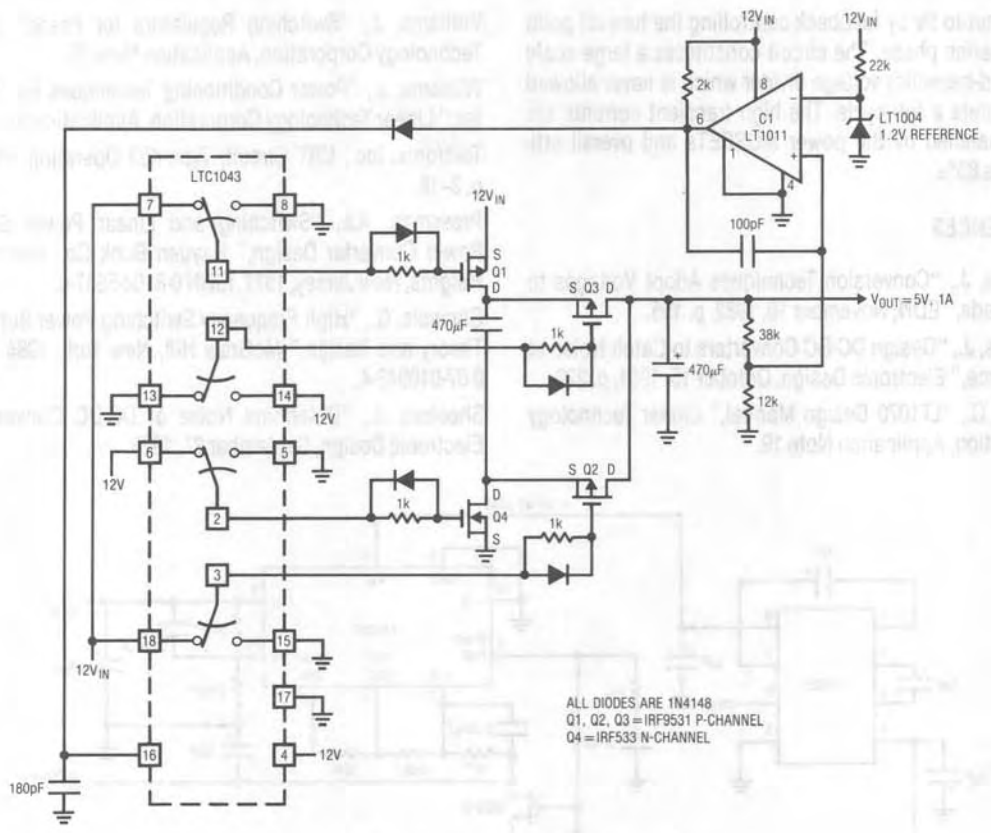

Figure 61. High Power Switched Capacitor Converter

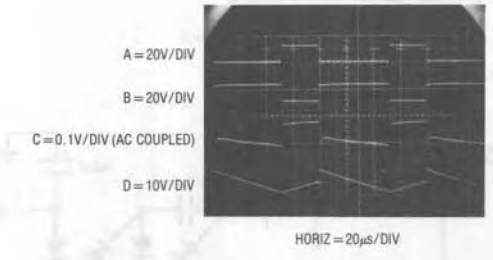

Figure 62. Waveforms for Figure 61

APPENDIX A

The 5V to ±15V Converter — A Special Case

Five volt logic supplies have been standard since the introduction of DTL logic over twenty years ago. Preceding and during DTL's infancy the modular amplifier houses standardized on ±15V rails. As such, popular early monolithic amplifiers also ran from ±15V rails (additional historical perspective on amplifier power supplies appears in AN-11's appended section, "Linear Power Supplies—Past, Present, and Future"). The 5V supply offered process, speed and density advantages to digital IC's. The ±15V rails provided a wide signal processing range to the analog components. These disparate needs defined power supply requirements for mixed analog-digital systems at 5V and ±15V. In systems with large analog component populations the ±15V supply was and still is usually derived from the AC line. Such line derived ±15V power becomes distinctly undesirable in predominantly digital systems. The inconvenience, difficulty and cost of distributing analog rails in heavily digital systems makes local generation attractive. 5V to ±15V DC-DC converters were developed to fill this need and have been with us for about as long as 5V logic.

Figure A1 is a conceptual schematic of a typical converter. The 5V input is applied to a self-oscillating configuration composed of transistors, a transformer and a biasing network. The transistors conduct out of phase, switching (Figure A2, traces A and C are Q1's collector and base, while traces B and D are Q2's collector and base) each time the transformer saturates. Transformer saturation causes a quickly rising, high current to flow (trace E). This current spike, picked up by the base drive winding, switches the transistors. Transformer current abruptly drops and then slowly rises until saturation again forces switching. This alternating operation sets transistor duty cycle at 50%. The transformers secondary is rectified, filtered and regulated to produce the outputs.

This configuration has a number of desirable features. The complementary high frequency (typically 20kHz) square wave drive makes efficient use of the transformer and allows relatively small filter capacitors. The self-oscillating primary drive tends to collapse under overload, providing desirable short circuit characteristics. The transistors switch in saturated mode, aiding efficiency. This hard switching, combined with the transformer's deliberate saturation does, however, have a drawback. During the saturation interval a significant, high frequency current

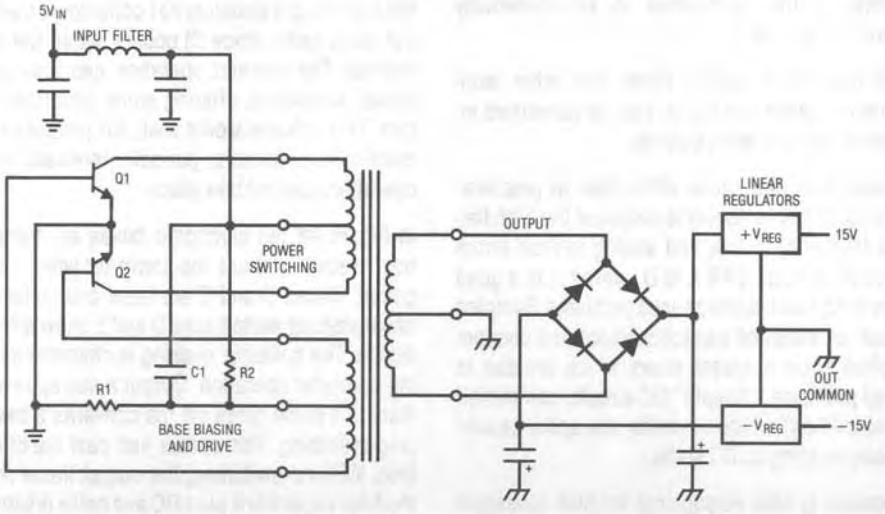

Figure A1. Conceptual Schematic of a Typical 5V to ±15V Converter

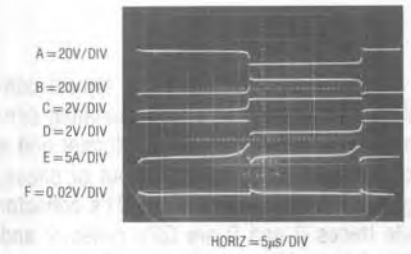

Figure A2. Typical 5V to ± 15V Saturating Converters Waveforms

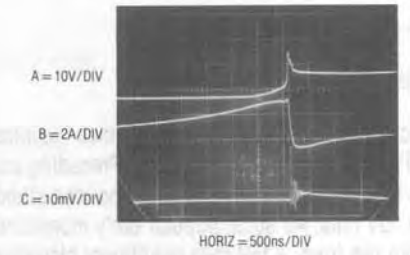

Figure A3. Switching Details of Saturating Converter

spike is generated (again, trace E). This spike causes noise to appear at the converter outputs (trace F is the AC coupled 15V output). Additionally, it pulls significant current from the 5V supply. The converters input filter partially smooths the transient, but the 5V supply is usually so noisy the disturbance is acceptable. The spike at the output, typically 20mV high, is a more serious problem. Figure A3 is a time and amplitude expansion of Figure A2's traces B, E and F. It clearly shows the relationship between transformer current (trace B, Figure A3), transistor collector voltage (trace A, Figure A3) and the output spike (trace C, Figure A3). As transformer current rises the transistor starts coming out of saturation. When current rises high enough the circuit switches, causing the characteristic noise spike. This condition is exacerbated by the other transistors concurrent switching, causing both ends of the transformer to simultaneously conduct current to ground.

Selection of transistors, output filters and other techniques can reduce spike amplitude, but the converters inherent operation ensures noisy outputs.

This noisy operation can cause difficulties in precision analog systems. IC power supply rejection at the high harmonic spike frequency is low, and analog system errors frequently result. A 12-bit SAR A-to-D converter is a good candidate for such spike-noise caused problems. Sampled data IC's such as switched capacitor filters and chopper amplifiers often show apparent errors which are due to spike induced problems. "Simple" DC circuits can exhibit baffling "instabilities" which in reality are spike caused problems masquerading as DC shifts.

The drive scheme is also responsible for high quiescent current consumption. The base biasing always supplies full drive, ensuring transistor saturation under heavy loading but wasting power at lighter loads. Adaptive bias schemes will mitigate this problem, but increase complexity and almost never appear in converters of this type.

The noise problem is, however, the main drawback of this approach to 5V to ± 15V conversion. Careful design, layout, filtering and shielding (for radiated noise) can reduce noise, but cannot eliminate it.

Some techniques can help these converters with the noise problem. Figure A4 uses a "bracket pulse" to warn the powered system when a noise pulse is about to occur. Ostensibly, noise sensitive operations are not carried out during the bracket pulse interval. The bracket pulse (trace A, Figure A5) drives a delayed pulse generator which triggers (trace B) the flip-flop. The flip-flop output biases the switching transistors (Q1 collector is trace C). The output noise spike (trace D) occurs within the bracket pulse interval. The clocked operation can also prevent transformer saturation, offering some additional noise reduction. This scheme works well, but presumes the powered system can tolerate periodic intervals where critical operations cannot take place.

In Figure A6 the electronic tables are turned. Here, the host system silences the converter when low noise is required. Traces B and C are base and collector drives for one transistor while traces D and E show drive to the other device. The collector peaking is characteristic of saturating converter operation. Output noise appears on trace F. Trace A's pulse gates off the converter's base bias, stopping switching. This occurs just past the 6th vertical division. With no switching, the output linear regulator sees the filter capacitor's pure DC and noise disappears.

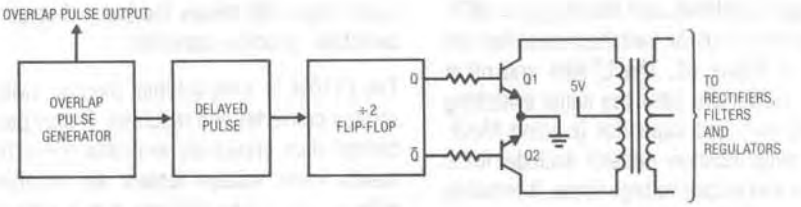

Figure A4. Overlap Generator Provides a "Bracket Pulse" Around Noise Spikes

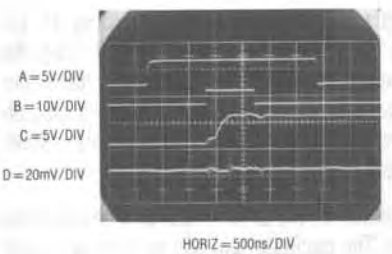

Figure A5. Waveforms for the Bracket Pulse Based Converter

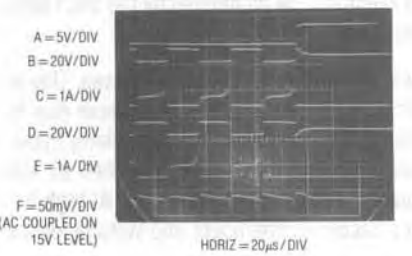

Figure A6. Detail of the Strobed Operation Converter

This arrangement also works nicely but assumes the control pulse can be conveniently generated by the system. It also requires larger filter capacitors to supply power during the low noise interval.

Other methods involve clock synchronization, timing skewing and other schemes which prevent noise spikes from coinciding with sensitive operations. While useful, none of these arrangements offer the flexibility of the inherently noise free converters shown in the text.

APPENDIX B

Switched Capacitor Voltage Converters — How They Work

To understand the theory of operation of switched capacitor converters, a review of a basic switched capacitor building block is helpful.

In Figure B1, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be Q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is Q2 = C1V2. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$Q = Q1 - Q2 = C1(V1 - V2)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$1 = fx\,Q = fxC1\,(V1 - V2)$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$1 = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}$$

A new variable, R_{EQUIV}, is defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure B2. The LT1054 and other switched capacitor converters have the same switching action as the basic switched capacitor building block. Even though this simplification doesn't include finite switch on-resistance and output voltage ripple, it provides an intuitive feel for how the device works.

These simplified circuits explain voltage loss as a function of frequency. As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and voltage losses will rise.

Note that losses also rise as frequency increases. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and voltage losses again rise.

The oscillators of practical converters are designed to run in the frequency band where voltage losses are at a minimum. Figure B3 shows the block diagram of the LT1054 switched capacitor converter.

The LT1054 is a monolithic, bipolar, switched capacitor voltage converter and regulator. It provides higher output current then previously available converters with significantly lower voltage losses. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5mA.

The LT1054 also provides regulation. By adding an external resistive divider, a regulated output can be obtained. This output will be regulated against changes in input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shutdown is less than 100μA.

The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency, or to externally synchronize the LT1054.

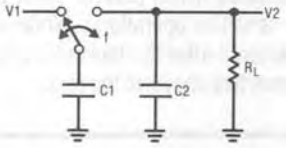

Figure B1. Switched Capacitor Building Block

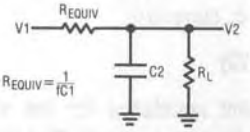

Figure B2. Switched Capacitor Equivalent Circuit

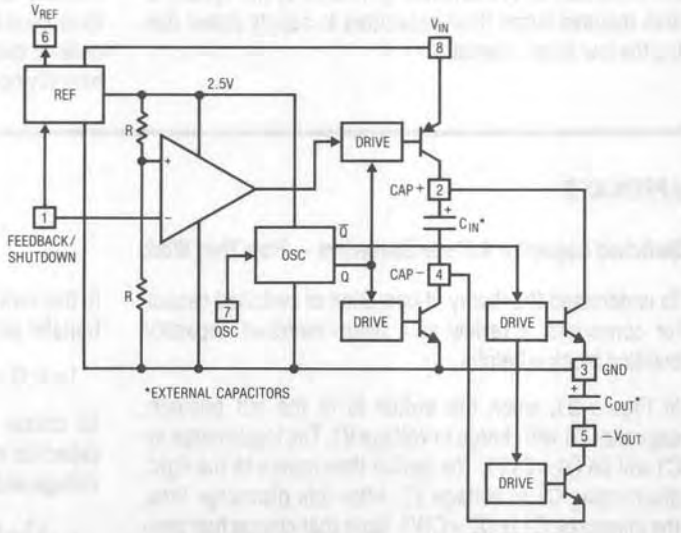

Figure B3. LT1054 Switched Capacitor Converter Block Diagram

APPENDIX C

Physiology of the LT1070

The LT1070 is a current-mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to Figure C1, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs

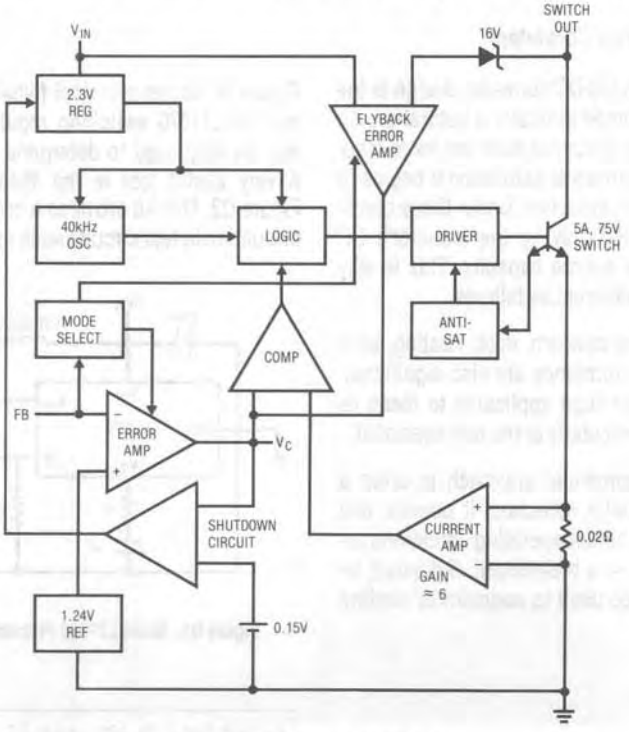

Figure C1. LT1070 Internal Details

the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback topology regulator. By regulating the amplitude of the flyback pulse the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft-starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft-start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown with only 50μA supply current for shutdown circuitry biasing. For more details, see Linear Technology Application Note AN-19, pages 4-8.

APPENDIX D

Inductor Selection for Flyback Converters

A common problem area in DC-DC converter design is the inductor, and the most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions current flow is limited only by the inductor's DC copper resistance and the source capacity. This is why saturation often results in destructive failures.

While saturation is a prime concern, cost, heating, size, availability and desired performance are also significant. Electromagnetic theory, although applicable to these issues, can be confusing, particularly to the non-specialist.

Practically speaking, an empirical approach is often a good way to address inductor selection. It permits real time analysis under actual circuit operating conditions using the ultimate simulator — a breadboard. If desired, inductor design theory can be used to augment or confirm experimental results.

Figure D1 shows a typical flyback based converter utilizing the LT1070 switching regulator. A simple approach may be employed to determine the appropriate inductor. A very useful tool is the #845 inductor kit[1] shown in Figure D2. This kit provides a broad range of inductors for evaluation in test circuits such as Figure D1.

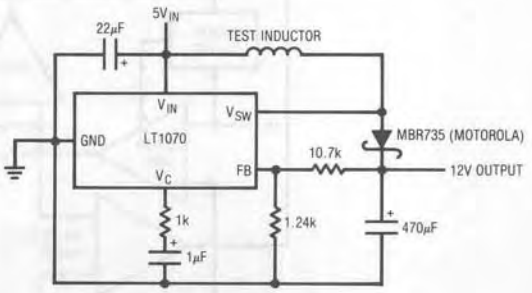

Figure D1. Basic LT1070 Flyback Converter Test Circuit

[1] Available from Pulse Engineering, Inc., P.O. Box 12235, San Diego, CA 92112, 619-268-2400

Figure D3 was taken with a 450μH value, high core capacity inductor installed. Circuit operating conditions such as input voltage and loading are set at levels appropriate to the intended application. Trace A is the LT1070's V_{SW} pin voltage while trace B shows its current. When V_{SW} pin voltage is low, inductor current flows. The high inductance means current rises relatively slowly, resulting in the shallow slope observed. Behavior is linear, indicating no saturation problems. In Figure D4, a lower value unit with equivalent core characteristics is tried. Current rise is steeper, but saturation is not encountered. Figure D5's selected inductance is still lower, although core characteristics are similar. Here, the curent ramp is quite pronounced, but well controlled. Figure D6 brings some informative surprises. This high value unit, wound on a low capacity core, starts out well but heads rapidly into saturation, and is clearly unsuitable.

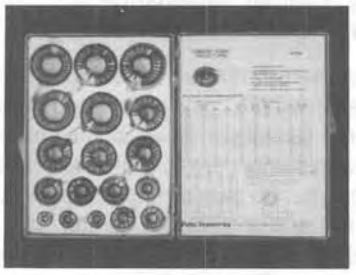

Figure D2. Model 845 Inductor Selection Kit from Pulse Engineering, Inc. (Includes 18 Fully Specified Devices)

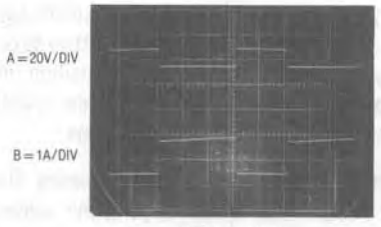

Figure D3. Waveforms for 450μH, High Capacity Core Unit

The described procedure narrows the inductor choice within a range of devices. Several were seen to produce acceptable electrical results, and the "best" unit can be further selected on the basis of cost, size, heating and other parameters. A standard device in the kit may suffice, or a derived version can be supplied by the manufacturer.

Using the standard products in the kit minimizes specification uncertainties, accelerating the dialogue between user and inductor vendor.

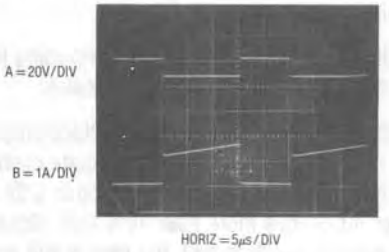

Figure D4. Waveforms for 170μH, High Capacity Core Unit

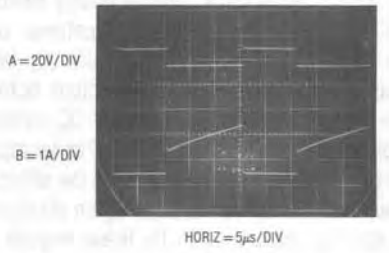

Figure D5. Waveforms for 55μH, High Capacity Core Unit

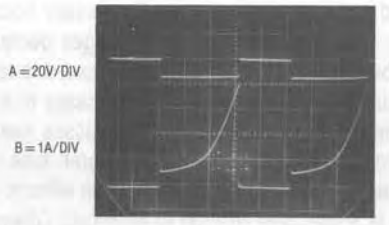

Figure D6. Waveforms for 500μH, Low Capacity Core Inductor (Note Saturation Effects)

APPENDIX E

Optimizing Converters for Efficiency

Squeezing the utmost efficiency out of a converter is a complex, demanding design task. Efficiency exceeding 80–85% requires some combination of finesse, witchcraft and just plain luck. Interaction of electrical and magnetic terms produces subtle effects which influence efficiency. A detailed, generalized method for obtaining maximum converter efficiency is not readily described but some guidelines are possible.

Losses fall into several loose categories including junction, ohmic, drive, switching, and magnetic losses.

Semiconductor junctions produce losses. Diode drops increase with operating current and can be quite costly in low voltage output converters. A 700mV drop in a 5V output converter introduces more than 10% loss. Schottky devices will cut this nearly in half, but loss is still appreciable. Germanium (rarely used) is lower still, but switching losses negate the low DC drop at high speeds. In very low power converters Germanium's reverse leakage may be equally oppressive. Synchronously switched rectification is more complex, but can sometimes simulate a more efficient diode (see text Figure 32). When evaluating such a scheme remember to include both AC and DC drive losses in efficiency estimates. DC losses include base or gate current in addition to DC consumption in any driver stage. AC losses might include the effects of gate (or base) capacitance, transition region dissipation (the switch spends some time in its linear region) and power lost due to timing skew between drive and actual switch action.

Transistor saturation losses are also a significant term. Channel and collector-emitter saturation losses become increasingly significant as operating voltages decrease. The most obvious way to minimize these losses is to select low saturation components. In some cases this will work, but remember to include the drive losses (usually higher) for lower saturation devices in overall loss estimates. Actual losses caused by saturation effects and diode drops is sometimes difficult to ascertain. Changing duty cycles and time variant currents make determination tricky. One simple way to make relative loss judgements is to measure device temperature rise. Appropriate tools here include thermal probes and (at low voltages) the perhaps more readily available human finger. At lower power (e.g., less dissipation, even though loss percentage may be as great) this technique is less effective. Sometimes deliberately adding a known loss to the component in question and noting efficiency change allows loss determination.

Ohmic losses in conductors are usually only significant at higher currents. "Hidden" ohmic losses include socket and connector contact resistance and equivalent series resistance (ESR) in capacitors. ESR generally drops with capacitor value and rises with operating frequency, and should be specified on the capacitor data sheet. Consider the copper resistance of inductive components. It is often necessary to evaluate trade-offs of an inductors copper resistance vs magnetic characteristics.

Drive losses were mentioned, and are important in obtaining efficiency. MOSFET gate capacitance draws substantial AC drive current per cycle, implying higher average currents as frequency goes up. Bipolar devices have lower capacitance, but DC base current eats power. Large area devices may appear attractive for low saturation, but evaluate drive losses carefully. Usually, large area devices only make sense when operating at a significant percentage of rated current. Drive stages should be thought out with respect to efficiency. Class A type drives (e.g., resistive pull-up or pull-down) are simple and fast, but wasteful. Efficient operation usually requires active source-sink combinations with minimal cross conduction and biasing losses.

Switching losses occur when devices spend significant amounts of time in their linear region relative to operating frequency. At higher repetition rates transition times can become a substantial loss source. Device selection and drive techniques can minimize these losses.

Magnetics design also influences efficiency. Design of inductive components is well beyond the scope of this appended section, but issues include core material selection, wire type, winding techniques, size, operating frequency, current levels, temperature and other issues.

Some of these topics are discussed in LTC Application Note AN-19, but there is no substitute for access to a skilled magnetics specialist. Fortunately, the other categories mentioned usually dominate losses, allowing good efficiencies to be obtained with standard magnetics. Custom magnetics are usually only employed after circuit losses have been reduced to lowest practical levels.

APPENDIX F

Instrumentation for Converter Design

Instrumentation for DC-DC converter design should be selected on the basis of *flexibility*. Wide bandwidths, high resolution and computational sophistication are valuable features, but are usually not required for converter work. Typically, converter design requires simultaneous observation of many circuit events at relatively slow speeds. Single ended and differential voltage and current signals are of interest, with some measurements requiring fully floating inputs. Most low level measurement involves AC signals and is accommodated with a high sensitivity plug-in. Other situations call for observation of small, slowly changing (e.g., 0.1Hz to 10Hz) events on top of DC levels. This range falls outside the AC coupled cut-off of most oscilloscopes, mandating differential DC nulling or "slide-back" plug-in capability. Other requirements include high impedance probes, filters and oscilloscopes with very versatile triggering and multi-trace capability. In our converter work we have found a number of particularly noteworthy instruments in several categories.

PROBES

For many measurements standard 1x and 10x scope probes are fine. In most cases the ground strap may be used, but low level measurements, particularly in the presence of wideband converter switching noise, should be taken with the shortest possible ground return. A variety of probe tip grounding accessories are available, and are usually supplied with good quality probes (see Figure F1). In some cases, directly connecting the breadboard to the 'scope may be necessary (Figure F2).

Wideband FET probes are not normally needed, but a moderate speed, high input impedance buffer probe is quite useful. Many converter circuits, especially micropower designs, require monitoring of high impedance nodes. The 10MΩ loading of standard 10x probes usually suffices, but sensitivity is traded away. 1x probes retain sensitivity, but introduce heavier loading. Figure F3 shows an almost absurdly simple, but useful, circuit which greatly aids probe loading problems. The LT1022 high speed FET op amp drives an LT1010 buffer. The LT1010's output allows cable and probe driving and also biases the circuits input shield. This bootstraps the input capacitance, reducing its effect. DC and AC errors of this circuit are low enough for almost all converter work, with enough bandwidth for most circuits. Built into a small enclosure with its own power supply, it can be used ahead of a 'scope or DVM with good results. Pertinent specifications appear in the diagram.

Figure F4 shows a simple probe filter which sets high and low bandwidth restrictions. This circuit, placed in series with the 'scope input, is useful for eliminating switching artifacts when observing circuit nodes.

An *isolated* probe allows fully floating measurements, even in the presence of high common mode voltages. It is often desirable to look across floating points in a circuit. The ability to directly observe an ungrounded transistor's saturation characteristics or monitor waveforms across a floating shunt makes this probe valuable. One probe, the Signal Acquisition Technologies, Inc. Model SL-10, has 10MHz bandwidth and 600V common mode capability.

Current probes are an indispensable tool in converter design. In many cases current waveforms contain more valuable information than voltage measurements. The clip-on types are quite convenient. Hall effect based versions respond down to DC, with bandwidths of 50MHz. Transformer types are faster, but roll off below several hundred cycles (Figure F5). Both types have saturation limitations which, when exceeded, cause odd results on the CRT, confusing the unwary. The Tektronix P6042 (and the more recent AM503) Hall type and P6022/134 transformer based type give excellent results. The Hewlett-Packard 428B

Figure F1. Proper Probing Technique for Low Level Measurements in the Presence of High Frequency Noise

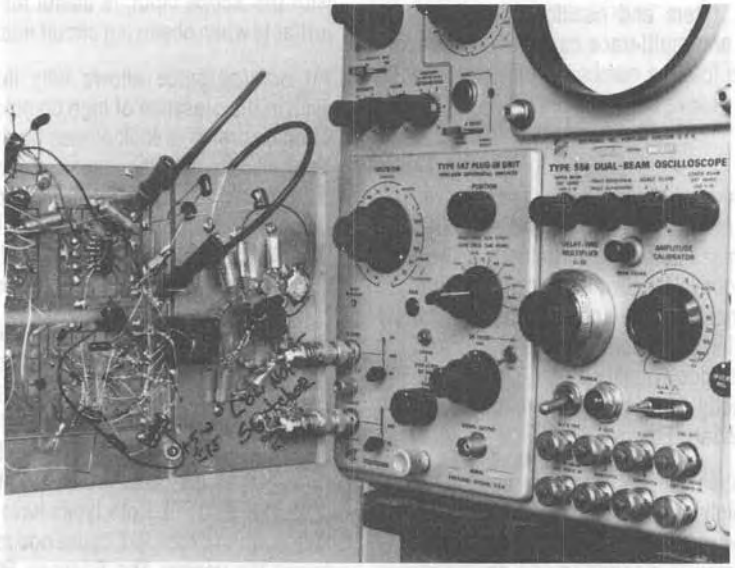

Figure F2. Direct Connections to the Oscilloscope Give Best Low Level Measurements. Note Ground Reference Connection to the Differential Plug-In's Negative Input.

clip-on current probe responds from DC to only 400Hz, but features 3% accuracy over a 100μA to 10A range. This instrument, useful for determining efficiency and quiescent current, eliminates shunt caused measurement errors.

OSCILLOSCOPES AND PLUG-INS

The oscilloscope plug-in combination is an important choice. Converter work almost demands multi-trace capability. Two channels are barely adequate, with four far preferable. The Tektronix 2445/6 offers four channels, but two have limited vertical capability. The Tektronix 547 (and the more modern 7603), equipped with a type 1A4 (2 dual trace 7A18's required for the 7603) plug-in, has four full capability input channels with flexible triggering and superb CRT trace clarity. This instrument, or its equivalent, will handle a wide variety of converter circuits with minimal restrictions. The Tektronix 556 offers an extraordinary array of features valuable in converter work. This dual beam instrument is essentially two fully independent oscilloscopes sharing a single CRT. Independent vertical, horizontal and triggering permit detailed display of almost any converters operation. Equipped with two type 1A4

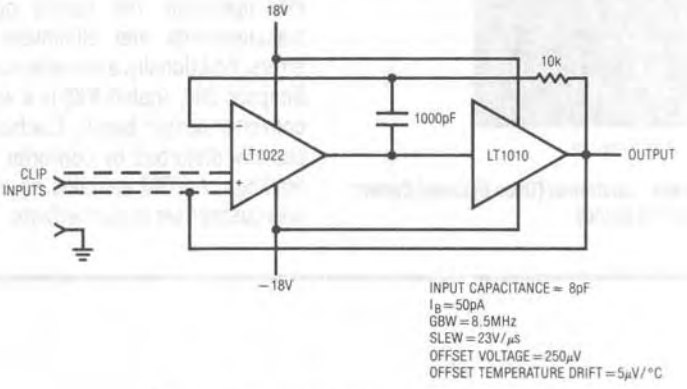

Figure F3. A Simple High Impedance Probe

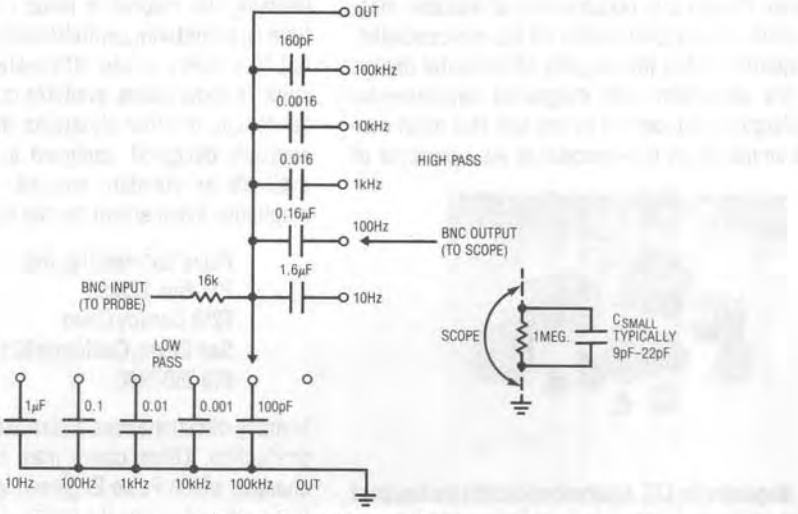

Figure F4. Oscilloscope Filter

plug-in's, the 556 will display eight real time inputs. The independent triggering and time bases allow stable display of asynchronous events. Cross beam triggering is also available, and the CRT has exceptional trace clarity.

Two oscilloscope plug-in types merit special mention. At low level, a high sensitivity differential plug-in is indispensable. The Tektronix 1A7 and 7A22 feature 10μV sensitivity, although bandwidth is limited to 1MHz. The units also have selectable high and low pass filters and good high frequency common mode rejection. Tektronix types W, 1A5 and 7A13 are differential comparators. They have calibrated DC nulling ("slideback") sources, allowing observation of small, slowly moving events on top of common mode DC.

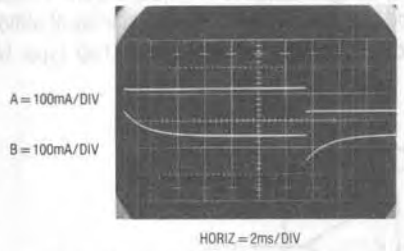

Figure F5. Hall (Trace A) and Transformer (Trace B) Based Current Probes Responding to Low Frequency

VOLTMETERS

Almost any DVM will suffice for converter work. It should have current measurement ranges and provision for battery operation. The battery operation allows floating measurements and eliminates possible ground loop errors. Additionally, a *non-electronic* (VOM) voltmeter (e.g., Simpson 260, Triplett 630) is a worthwhile addition to the converter design bench. Electronic voltmeters are occasionally disturbed by converter noise, producing erratic readings. A VOM contains no active circuitry, making it less susceptible to such effects.

APPENDIX G

The Magnetics Issue

Magnetics is probably the most formidable issue in converter design. Design and construction of suitable magnetics is a difficult task, particularly for the non-specialist. It is our experience that the majority of converter design problems are associated with magnetics requirements. This consideration is accented by the fact that most converters are employed by non-specialists. As a purveyor of switching power IC's we incur responsibility towards addressing the magnetics issue (our publicly spirited attitude is, admittedly, capitalistically influenced). As such, it is LTC's policy to use off-the-shelf magnetics in our circuits. In some cases, available magnetics serve a particular design. In other situations the magnetics have been specially designed, assigned a part number and made available as standard product. In these endeavors our magnetics supplier and partner is;

Figure G1. Magnetics for LTC Applications Circuits are Designed and Supplied as Standard Product by Pulse Engineering, Inc.

Pulse Engineering, Inc.
P.O. Box 12235
7250 Convoy Court
San Diego, California 92112
619-268-2400

In many circumstances a standard product is suitable for production. Other cases may require modifications or changes which Pulse Engineering can provide. Hopefully, this approach serves the needs of all concerned.