A TRANSISTOR FOR 100 kHz CONVERTERS : ETD

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INTRODUCTION

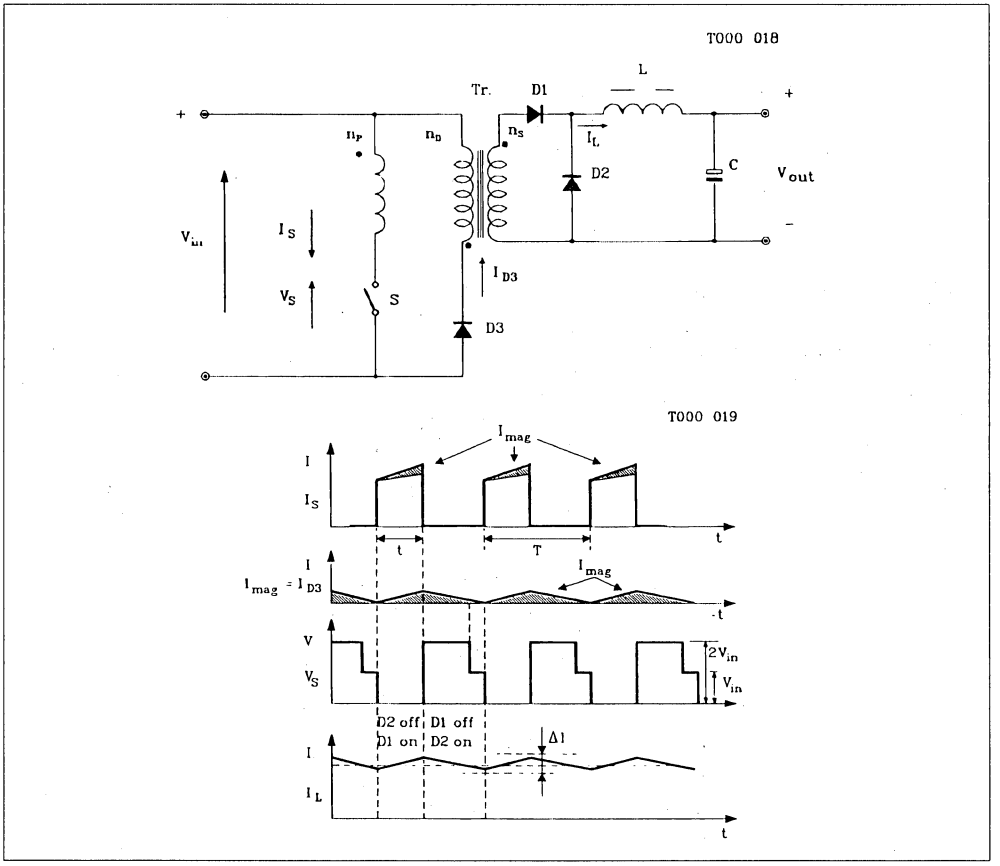
Power converter designers aim to reduce the size and the weight of their equipment. Hence, there is a trend towards higher operating frequencies. Consequently for the semiconductor manufacturers, there is a growing demand for fast switches. The POWER MOSFET transistor is now well known as a fast device.

However, the development of ultra fast "ETD" bipolar transistors is now challenging this way of thinking in certain applications. As an illustration, we have selected an example of a "300W - 100kHz forward" switch mode power supply (SMPS).

VOLTAGE CONSTRAINTS

This "forward" converter contains a single power switch and operates directly from the 220V AC mains. The principle wave forms are illustrated in figure 1.

Figure 1 : Basic Theoretical Wave Forms of the Forward SMPS.



The switch must be capable of withstanding a static collector-emitter voltage which, to a first approximation, is given by :

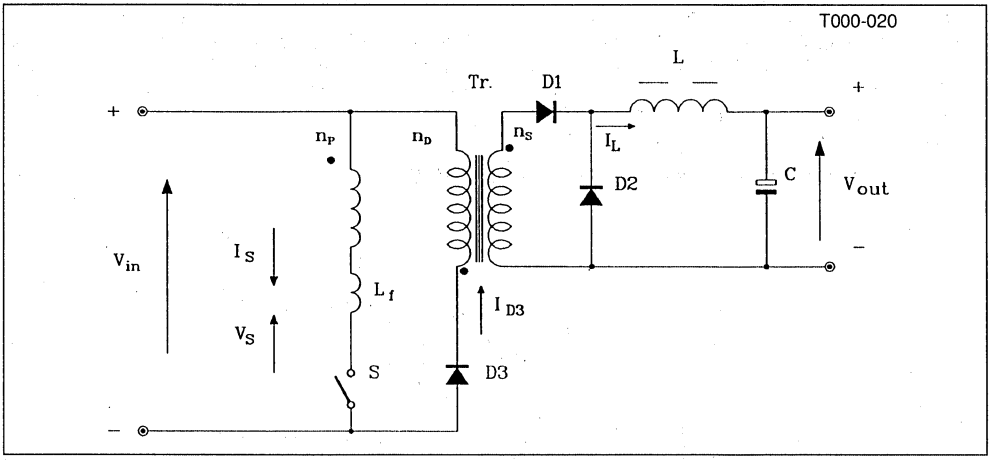
$(1 + n_P/n_D) \times V_{in}$, where,

- n_P = number of turns in the primary winding
- n_D = number of turns in the demagnetization winding
- V_{in} = rectified mains voltage

When operating on the 220V AC mains and when n_P equals n_D, the voltage across the switch terminals should only reach 750V in the worst case (corresponding to a maximum rectified mains value of 375V AC).

In reality, the voltage across the switch terminals reaches a peak value (V_{peak}) which is much higher. The peak value depends upon the switching time, the circuit capacitance and the leakage inductance L_f between primary winding n_P and the demagnetization winding n_D (see figure 2).

Figure 2 : Leakage Inductance L_f between Primary Winding n_P and Demagnetization Winding n_D.



DESIGN OF SNUBBER CIRCUIT

At turn-off, energy stored in the transformer leakage inductance generates a voltage spike (figure 3). In order to limit this voltage spike, the energy must be transferred to the capacitor C_{min} in the snubber circuit. The energy depends on the switching current. In a 300W SMPS, the peak value of the current I_{max} is 5A. It is this value of current which is used to calculate the value of the capacitance C_{min} required.

With a maximum voltage V_{peak}, the value of C_{min} can be calculated using the following formula :

$$C_{min} = \frac{L_f \times I_{max}^2}{V_{peak}^2 - V_{in\,max}^2 (1 + N_P/N_D)^2}$$

Figure 3a : Wave Forms of Switching Current and Voltage Across the Switch Terminals at Turn-off.

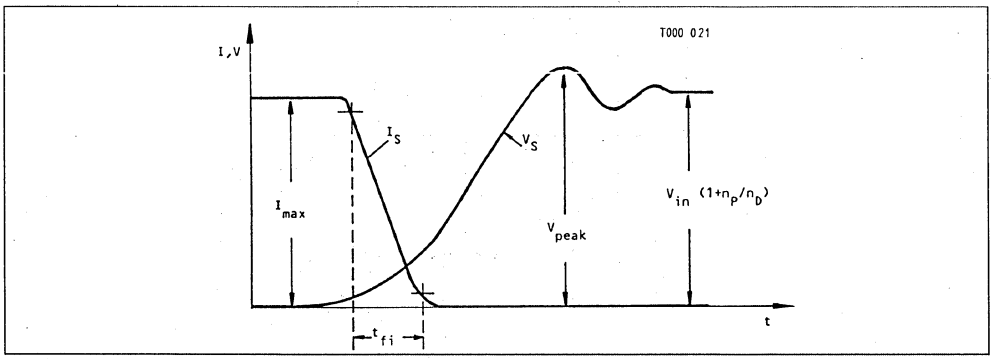
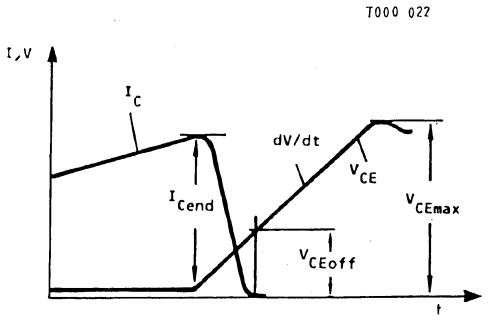


Figure 3b : Definition of the Voltage V_{CEoff}. V_{CEoff} is measured when the Collector Current Reaches 2 % of the Collector I_{Cend}.



We call V_{CEoff} the voltage which appears during the turn-off at the moment when the collector current I_C reaches 2% of its value I_{Cend}. If the value V_{CEoff} measured in the circuit is low compared to the rating V_{CEW} of the transistor, the safety margin between the SOAR and the stress on the transistor is large. V_{CEW} is the maximum V_{CE} voltage at turn-off with current.

In practice, V_{peak} can be set between 800 and 900V. To provide a safety margin, a switch with a blocking voltage capability of 1000V must be used. This voltage corresponds to parameter V_{CEV} for bipolar transistors and to V_{DSS} for POWER MOSFET components.

For bipolar transistors, an additional parameter must be considered : the Reverse Biased Safe Operating Area : (RBSOA). The turn-off cycle must remain within the RBSOA, otherwise, the value of capacitance must be increased from C_{min} to a higher value C_r.

Thermal dissipation in the snubber resistor, R_s (figure 6), will be increased in the same ratio :

$$C_r = \frac{t_{fi} \times I_{max}}{2 \times V_{CEoff}}$$

For the selected transistor, V_{CEoff} must be less than the specified V_{CEW} (see figures 3a and 3b).

SWITCH TYPE

In this application, three different types of switch using different technologies are considered. These are :

- conventional bipolar transistor,
- POWER MOSFET,
- ultrafast bipolar "ETD" transistor (see appendix).

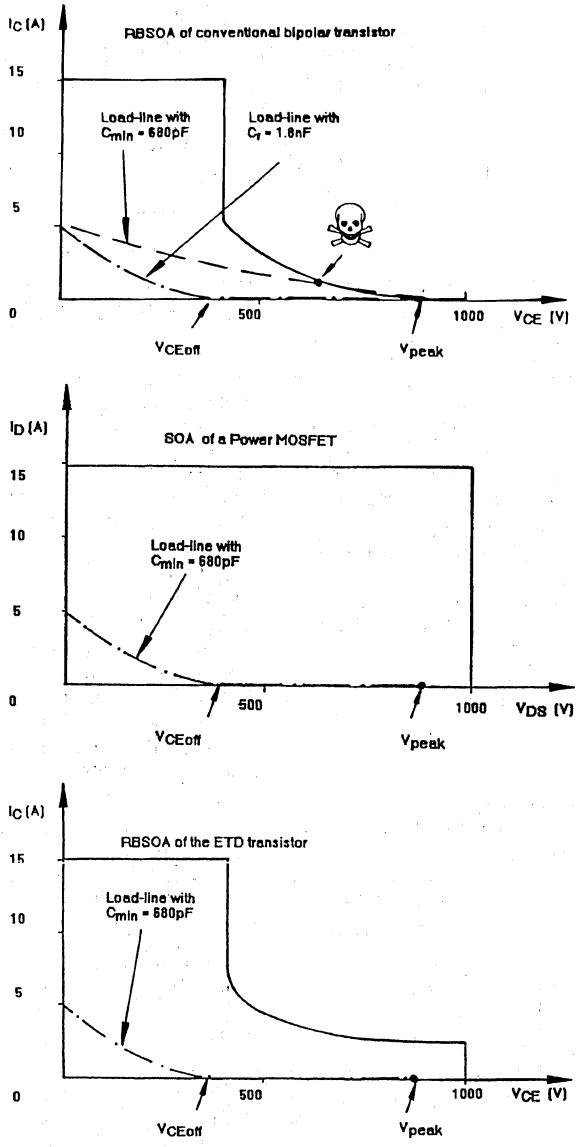
Table 1 summarizes the performances of these types of switches under operating conditions, i.e., for a junction temperature of 100°C and with a well adapted gate/base drive (optimized totem-pole drive for POWER MOSFETs and negative bias drive for bipolar transistors).

Table 1 : Transistor Characteristics.
Characteristics at Tj = 100°C "Totempole" gate drive. Base drive with negative bias. Same silicon area for each switch.

	Blocking Voltage Capability	Switching Time (Tj = 100°C)		Conduction (T_j = 100°C)
		t_r	t_{fi}	R_{DSon}, V_{CEsat}
STHV 102 VDMOS	1000V	100ns	100ns	5.4Ω
BUV 48 Conventional Transistor	1000V	85ns (60A/µs)	250ns	2.8V (5A)
BUF 410A ETD Transistor	1000V	50ns (100A/µs)	100ns	2.8V (5A)

The first point to notice is that at turn-off, an ETD transistor is as fast as a POWER MOSFET.
More surprisingly, the ETD transistor is twice as fast as a POWER MOSFET at turn-on.
Let us now consider the effects of the characteristics upon the size of the snubber. With a leakage inductance of 6.5µH and a current of 5A, a capacitor C_{min} of value 680pF is sufficient to limit the voltage V_{peak} to 900V (fig. 4) :

Figure 4 : Comparison of Turn-off Cycle Within the Safe Operating Areas for the Three Different Switches.



- However, a capacitor C_r of 1.8nF is required to limit the V_{CEoff} voltage to a value that is within the RBSOA of the bipolar conventional transistor.
- In comparison, the POWER MOSFET and ETD transistors can be kept within their safe operating areas with a capacitor of only 680pF.

LOSS EVALUATION

For the 300W forward SMPS operating at 100kHz, the following assumptions have been made.

The losses have been evaluated assuming a current I_{nom} of 4A, corresponding to the nominal output power. A current of 2.8A rms is obtained with a duty cycle of 48.5%. For a realistic comparison, conduction losses were reduced by paralleling two POWER MOSFETs (the conduction losses of a single POWER MOSFETs would be approximately 43W). The results of this evaluation are as shown in Table 2.

Table 2 : Results of Loss Evaluation for the Conventional Bipolar Transistor, the two paralleled Power MOSFET and the ETD BUF 410A Transistor.

	BUV48A	2 x STHV102	BUF410A
Silicon Area	30mm^2	40mm^2	30mm^2
Snubber (RCD) C_r	1.8nF	680pF	680pF
P_R*	51W	19W	19W
Losses in the Switch	30W	34W	17.5W
Conduction	5.4W	21.3W	5.4W
Switching	20.7W	12.3W	9.2W
Drive	3.9W	0.4W	2.9W
TOTAL LOSSES (RCD + COM)	81W	53W	36.5W

* P_R is the power dissipated in the resistor of the snubber circuit.

- for this application, the ETD transistor requires no more silicon area than a conventional bipolar transistor.
- the ETD transistor uses the same value of snubber capacitance as a POWER MOSFET.
- conduction losses in the ETD and the conventional bipolar transistor are the same.
- the ETD transistor has the lowest switching losses of the three devices considered.

In our example, at 100kHz, the superior performance of an ETD transistor results in about a 50% reduction in losses as compared to the BUV48A and 30% compared with POWER MOSFETs.

CONCLUSION

The example described in this paper (300W - 100kHz SMPS), figure 6 shows that of the three devices considered, the ETD transistor is the optimum cost/performance solution.

In addition, as a result of its fast switching capability ($t_r < 50ns$; $t_{fi} < 100ns$) and its extended RBSOA, the ETD transistor can be successfully used in other applications such as resonant converters, motor drives or uninterruptible power supplies.

ETD transistors with blocking voltage capability higher than 1000V are under development. These transistors will enable higher switching frequencies to be used in equipment supplied directly from the 380/440V mains supply.

APPENDIX I

WHAT MAKES ETD TRANSISTORS SO ATTRACTIVE ?

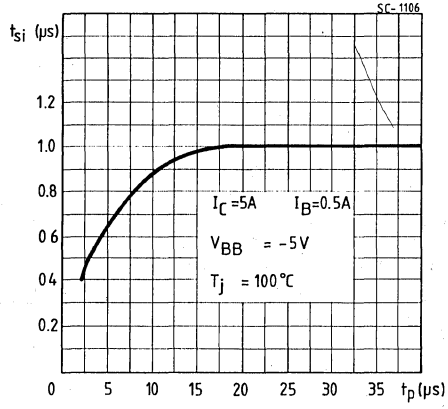
The new generation of ETD transistors adapted for high voltage applications is designed with an inovative technology utilizing a high degree of interdigitation.

The most innovative feature of this technology consists of the replacement of the traditional bipolar structure with emitter fingers (size : 250µm) by a cellular structure with much smaller dimensions (80µm cells). This cell design considerably eases the extraction of charge stored in the transistor during each switching cycle, since access to the intrinsic base is easier. This makes it possible to reduce switching times to values as low as 100ns.

The "Planar" technology has been selected for two reasons :

It permits extension of safe operating area at turn-off. Moreover, it requires a reduced number of masking levels with respect to conventional high voltage "mesa" power technologies.

Figure 5 : Curve Illustrating the Variation of Storage Time t_{si} versus Conduction Time t_p. (ETD transistor BUF410A).



REGULATION DYNAMICS

In SMPS or motor drive applications, the minimum conduction time is a fundamental parameter when considering the dynamic regulation. The delay time at turn-off of the POWER MOSFETs specified in the data sheet is sufficiently low.

In the case of bipolar transistors, storage time depends on conduction time. In our application at 100kHz, conduction time must vary from less than one microsecond to five microseconds. In the BUF410A data sheet, the curve showing the variation of storage time, t_s, versus conduction time, t_p, shows that storage time varies from zero to 750ns maximum (see Figure 5). Consequently, the regulation dynamics are not limited.

Figure 6 : Schematic Diagram of an ETD BUF410A Transistor Implemented in a 300W – 100kHz Forward SMPS Application.