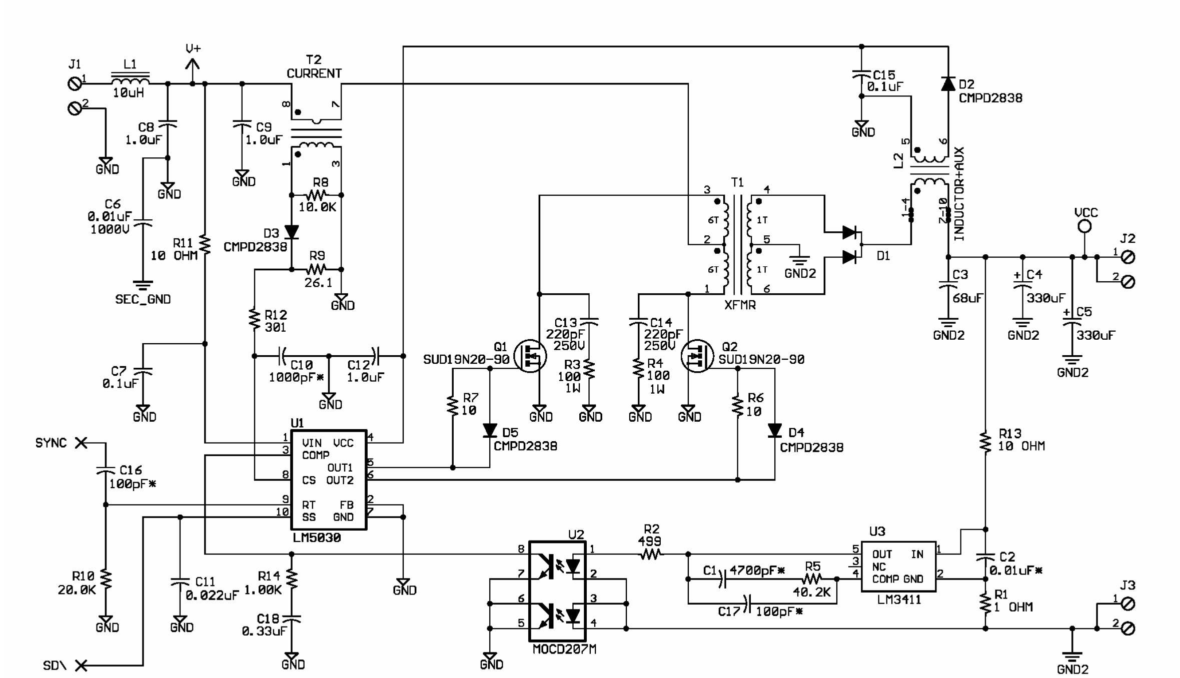
SWITCHING POWER SUPPLY DESIGN:
LM5030 PUSH-PULL CONVERTER

Written by Michele Sclocchi
michele.sclocchi@nsc.com
National Semiconductor



Push-pull topology is a derivative of two forward converters operating 180 degrees out of phase. This configuration allows operation in the first and third quadrant of the hysteresis loop, with a better utilization of the magnetic core of the transformer. The maximum voltage stress of the switching MOSFETs is twice the input voltage which is the same as the the forward topology. A current mode PWM converter avoids run away of the flux core by monitoring the current of each of the push-pull transistors and forcing alternate current pulses to have equal amplitude.

This document is an explanation of the equations used in an accompanying Mathcad file. The Mathcad file helps with the calculation of the external components of a typical Push-Pull topology.

Notes for the Mathcad file:
Write down the power supply requirements in the following boxes: $X_{xx} :=$

Get the results from the following boxes: $Rsults_{xx} :=$

Listed below are the equations used to calculate the circuit:
Input voltage:

- Minimum input voltage: $Vi_{min} := 35\cdot volt$

- Maximum input voltage: $Vi_{max} := 75\cdot volt$

- Nominal input voltage: $Vi_{nom} := 48\cdot volt$

Output:
- Nominal output voltage, maximum output ripple, minimum output current, maximum output current

$Vo1 := 12\cdot volt$ $Vrp1 := 100\cdot mV$ $Io1_{min} := 0.5\cdot amp$ $Io1_{max} := 5\cdot amp$

$Vo2 := 3.7 \cdot volt$ $Vrp2 := 120 \cdot mV$ $Io2_{min} := 0.1 \cdot amp$ $Io2_{max} := 0.500 \cdot amp$

$Vd_{fw} := 0.9 \cdot volt$ (diode's forward voltage drop)

$$Po_{min} := (Vo1 + Vd_{fw}) \cdot Io1_{min} + (Vo2 + Vd_{fw}) \cdot Io2_{min} \qquad Po_{min} = 6.91 watt$$

$$Po_{max} := (Vo1 + Vd_{fw}) \cdot Io1_{max} + (Vo2 + Vd_{fw}) \cdot Io2_{max} \qquad Po_{max} = 66.8 watt$$

- Switching Frequency: $fsw := 250 \cdot kHz$

$$T := \frac{1}{fsw} \qquad T = 4 \mu sec$$

Each phase switches at half the switching frequency:

$$T_{ch} := \frac{2}{fsw} \qquad T_{ch} = 8 \mu sec$$

- Transformer's Efficiency: $\eta := 0.95$ (Guessed value)

- Maximum voltage drop across the switching MOSFET during the on time:

- On resistance of the MOSFET: $Rds_{on} := 0.10 \cdot ohm$

$$Vds_{on} := \frac{Po_{max}}{\eta \cdot Vi_{min}} \cdot Rds_{on} \qquad Vds_{on} = 0.2 volt$$

1) Maximum duty cycle, minimum duty cycle, secondary/primary turn ratio:

Choose the maximum duty cycle of each phase: $D_{max} := 0.365$

At minimum operating voltage the duty cycle of each phase has to be << 40%

$$Ton_{max} := T_{ch} \cdot D_{max} \qquad Ton_{max} = 2.92 \mu sec$$

-The turns ratio between secondary and primary winding:

$$Nsp1 := \frac{\frac{Vo1}{D_{max} \cdot 2} + Vd_{fw}}{Vi_{min} - Vds_{on}} \qquad Nsp1 = 0.5$$

- Minimum duty cycle at maximum input voltage:

$$Dmin := \frac{Vo1}{2 \cdot Nsp1 \cdot (Vi_{max} - Vds_{on}) - Vd_{fw}} \qquad Dmin = 0.16$$

- Duty cycle at nominal input voltage:

$$Dnom := \frac{Vo1}{2 \cdot Nsp1 \cdot (Vi_{nom} - Vds_{on}) - Vd_{fw}} \qquad Dnom = 0.26$$

2) Maximum stress voltage across the drain source of the external switching MOSFETs:

The maximum DC input voltage plus the spikes due to the leakage inductance. (assume spikes of 30% of Vdc)

$$Vsw_{max} := 2 \cdot (1.15 \cdot Vi_{max}) \qquad Vsw_{max} = 172.5 volt$$

3) Primary and secondary currents:

Input power: Pin=Vi_{min}*Ipft*max.duty cycle*2

$$Idc := \frac{Po_{max}}{(Vi_{min} - Vds_{on})}$$

Ipft is the equivalent flat topped primary current

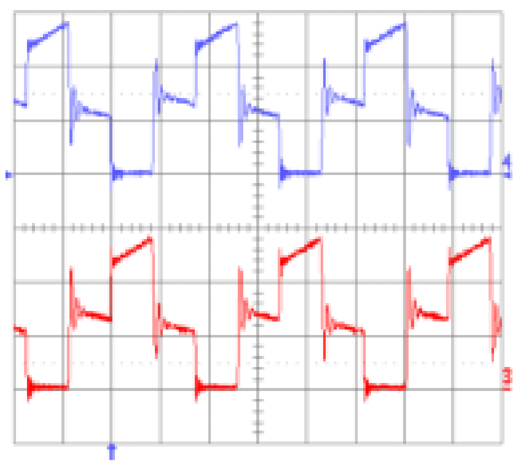
$$Ip_{dc} := \frac{Po_{max}}{(Vi_{min} - Vds_{on}) \cdot \eta} \qquad Ip_{dc} = 2.02\text{amp}$$

$$Ip_{ft} := \frac{Po_{max}}{(Vi_{min} - Vds_{on}) \cdot \eta \cdot 2 \cdot D_{max}} \qquad Ip_{ft} = 2.77\text{amp}$$

Primary rms current: $Ip_{rms} := Ip_{ft} \cdot \sqrt{D_{max}}$ $\quad Ip_{rms} = 1.67\text{amp}$ $\quad$ (*1)

$$Ip_{ac} := Ip_{ft} \cdot \sqrt{D_{max} \cdot (1 - D_{max})} \qquad Ip_{ac} = 1.33\text{amp}$$

Secondary rms current: it's assumed that the peak of the center top ramp is equal to the DC output current.



(Current waveform on the secondary windings)

$$Is1_{rms} := Io1_{max} \cdot \sqrt{D_{max}} \qquad Is1_{rms} = 3.02\text{amp}$$

$$Is2_{rms} := Io2_{max} \cdot \sqrt{D_{max}} \qquad Is2_{rms} = 0.3\text{amp}$$

$$Is1_{ac} := Io1_{max} \cdot \sqrt{D_{max} \cdot (1 - D_{max})}$$

$$Is2_{ac} := Io2_{max} \cdot \sqrt{D_{max} \cdot (1 - D_{max})} \qquad Is2_{ac} = 0.24\text{ amp}$$

4) Maximum stress across the output diodes: Vdiode

-Maximum stress voltage on the cathode of the diodes

$$Vdiode1_{max} := 2 \cdot Vi_{max} \cdot Nsp1 \qquad Vdiode1_{max} = 74.74\text{volt}$$

Select a diode with Va-c>> Vdiode.max, and ultra-fast switching diode

- The total output diodes' power losses:

$Pdiode1_{max} := Io1_{max} \cdot Vd_{fw}$ $\quad Pdiode1_{max} = 4.5\,watt$ (first output)

$Pdiode2_{max} := Io2_{max} \cdot Vd_{fw}$ $\quad Pdiode2_{max} = 0.45\,watt$ (second output)

For high current and low output voltage applications, a synchronous rectification solution, with external MOSFET is usually preferred

$Pdiode_{tot} := Pdiode1_{max} + Pdiode2_{max}$ $\quad Pdiode_{tot} = 4.95\,watt$

5) Output ripple specifications and output capacitors

- the output inductors should not be permitted to go discontinuous, this occurs when the DC current has dropped to half the ramp, dI:

$V_L = L*di/dt$ $\quad dI = 2*Io_{min} = V_L * Ton/Lo = (Vf-Vo)Ton/Lo$ $\quad$ But Vo = Vf(2*Ton/T)

$$Vf2 := \frac{Vo2}{2 \cdot Ton_{max}} \cdot T_{ch} \qquad Vf2 = 5.07\,volt$$

$$Vf1 := \frac{Vo1}{2 \cdot Ton_{max}} \cdot T_{ch} \qquad Vf1 = 16.44\,volt$$

$$Lo1 := \frac{(Vf1 - Vo1) \cdot Ton_{max}}{2 \cdot Io1_{min}} \qquad Lo1 = 12.96\,\mu H$$

$$Lo2 := \frac{(Vf2 - Vo2) \cdot Ton_{max}}{2 \cdot Io2_{min}} \qquad Lo2 = 19.98\,\mu H$$

The Output inductor has to be greater than >> Lo1 and 2

Inductance used:

$Lo1_u := 25 \cdot \mu H$ $\qquad Lo2_u := 25 \cdot \mu H$

$$dI1 := \frac{(Vf1 - Vo1) \cdot Ton_{max}}{Lo1_u} \qquad dI1 = 0.52\,amp$$

$$dI2 := \frac{(Vf2 - Vo2) \cdot Ton_{max}}{Lo2_u} \qquad dI2 = 0.16\,amp$$

To meet the output ripple specifications, the output capacitors have to meet two criteria:

- Satisfy the standard capacitance definition: **I=C*dV/dt** where t is the Toff time, and V is 25% of the allowable output ripple.

- The Equivalent Series Resistance (ESR) of the capacitor has to provide less than 75% of the maximum output ripple. (Vripple=dI*ESR)

-Maximum output ripple: $\quad Vrp1 = 100\,mV$ $\qquad Vrp2 = 120\,mV$

-Minimum output capacitance:

$$Co1 := dI1 \cdot \frac{(Ton_{max})}{Vrp1 \cdot 0.25}$$ $Co1 = 60.55\mu F$

-Maximum ESR value:

$$ESR1 := \frac{Vrp1 \cdot 0.75}{dI1}$$ $ESR1 = 0.14ohm$

-Minimum output capacitance:

$$Co2 := dI2 \cdot \frac{(Ton_{max})}{Vrp2 \cdot 0.25}$$ $Co2 = 15.56\mu F$

-Maximum ESR value:

$$ESR2 := \frac{0.75 \cdot Vrp2}{dI2}$$ $ESR2 = 0.56ohm$

6) Input capacitor

The input capacitor has to meet the maximum ripple current rating Ip(rms) and the maximum input voltage ripple ESR value.

7) Switching MOSFET power dissipation

The MOSFET is chosen based on maximum stress voltage (section1), maximum peak input current (section 3), total power losses, maximum allowed operating temperature, and driver capability of the LM5030

-The drain to source breakdown of the MOSFET (Vdss) has to be greater than:

$Vsw_{max} = 172.5volt$

- Maximum drive voltage: $Vdr := 9 \cdot volt$

$Idrive := 3amp$ (Drivercurrent)

$Rdr_{on} := \frac{Vdr}{Idrive}$ $Rdr_{on} = 3ohm$

-Total the MOSFET's losses and calculate the maximum junction temperature:

The goal in selecting a MOSFET is to minimize junction temperature rise by minimizing the power loss while being cost effective. Besides maximum voltage rating, and maximum current rating, the other three important parameters of a MOSFET are Rds(on), gate threshold voltage, and gate capacitance.

The switching MOSFET has three types of losses, which are conduction loss, switching loss, and gate charge losses.

-**Conduction losses** are I^2*R losses, therefore the total resistance between the source and drain during the on state, Rds(on) has to be as low as possible.

-The **switching loss** equation is Switching-time*Vds*I*frequency. The switching time, rise time and fall time are a function of: a) the gate to drain Miller-charge of the MOSFET, Qgd, b) the internal resistance of the driver and c) the Threshold Voltage, Vgs(th), which is the minimum gate voltage which enables the current through the drain source of the MOSFET.

-Gate charge losses are caused by charging up the gate capacitance and then dumping the charge to ground every cycle. The gate charge losses are equal to: frequency * Qg(tot) * Vdr

Unfortunately, the lowest on resistance devices tend to have higher gate capacitance.

Because this loss is frequency dependent, in very high current supplies with very large FETs with large gate capacitance, a more optimal design may result from reducing the operating frequency.

Switching losses are also effected by gate capacitance. If the gate driver has to charge a larger capacitance, then the time the MOSFET spends in the linear region increases and the losses increase. The faster the rise time, the lower the switching loss. Unfortunately this causes high frequency noise.

MOSFET: SUD19N20-90

$Rds_{on} := 0.090 \cdot ohm$ (Total resistance between the source and drain during the on state)

$Coss := 180 \cdot pF$ (Output capacitance)

$Qg_{tot} := 34 \cdot n \cdot coul$ (Total gate charge)

$Qgd := 12 \cdot n \cdot coul$ (Gate drain Miller charge)

$Qgs := 8 \cdot n \cdot coul$ (Gate to source charge)

$Vgs_{th} := 2 \cdot volt$ (Threshold voltage)

- Conduction losses: Pcond

$Pcond := Rds_{on} \cdot Ip_{ft}^{2} \cdot D_{max}$ $Pcond = 0.25 watt$

- Switching losses: Psw(max): V*I/2*freq*(Tswon+Tswoff) (*2)

$$Idriver_{LH} := \frac{Vdr - Vgs_{th}}{Rdr_{on}} \qquad Idriver_{LH} = 1.4 amp$$

(Peak current of the driver from low to high)

$$Idriver_{HL} := \frac{Vdr - Vgs_{th}}{Rdr_{off}} \qquad Idriver_{HL} = 14 amp$$

(Peak current of the driver from high to low)

$$Qg_{sw} := Qgd + \frac{Qgs}{2} \qquad Qg_{sw} = 16 coul\, n$$

- Estimated turn on time:

$$tsw_{LH} := \frac{Qg_{sw}}{Idriver_{LH}} \qquad tsw_{LH} = 11.43 sec\, n$$

- Estimated turn off time:

$$tsw_{HL} := \frac{Qg_{sw}}{Idriver_{HL}} \qquad tsw_{HL} = 1.14 sec\, n$$

$$Psw_{max} := Vi_{min} \cdot Ip_{ft} \cdot fsw \cdot (tsw_{LH} + tsw_{HL}) + \frac{Coss \cdot Vi_{min}^{2} \cdot fsw}{2}$$

$Psw_{max} = 0.33 watt$

- Gate charge losses: Pgate

Average current required to drive the gate capacitor of the MOSFET:

$Igate_{awg} := fsw \cdot Qg_{tot}$ $Igate_{awg} = 8.5 \times 10^{-3} amp$

$Pgate := Igate_{awg} \cdot Vdr$ $Pgate = 0.08 watt$

-Total losses: Ptot(max) (for each phase)

$Pmosfet_{tot} := Pcond + Psw_{max} + Pgate$ $Pmosfet_{tot} = 0.66 watt$

-Maximum junction temperature and heat sink requirement:

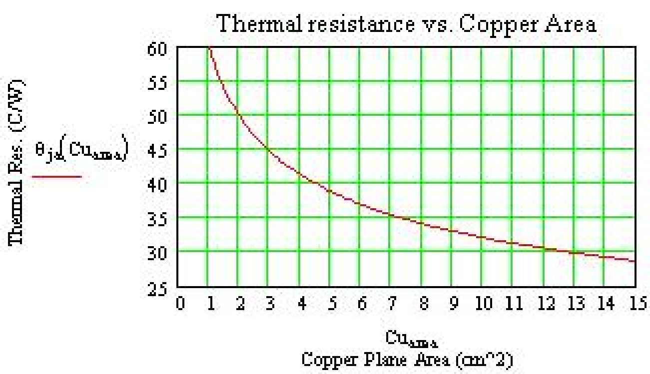
Maximum junction temperature desired: $Tj_{max} := 120$ Celsius

Maximum ambient temperature: $Ta_{max} := 70$ Celsius

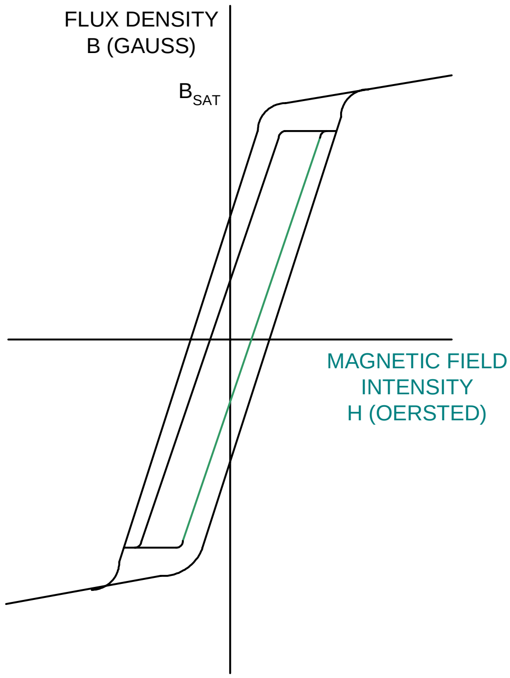
-Required junction to ambient thermal resistance:

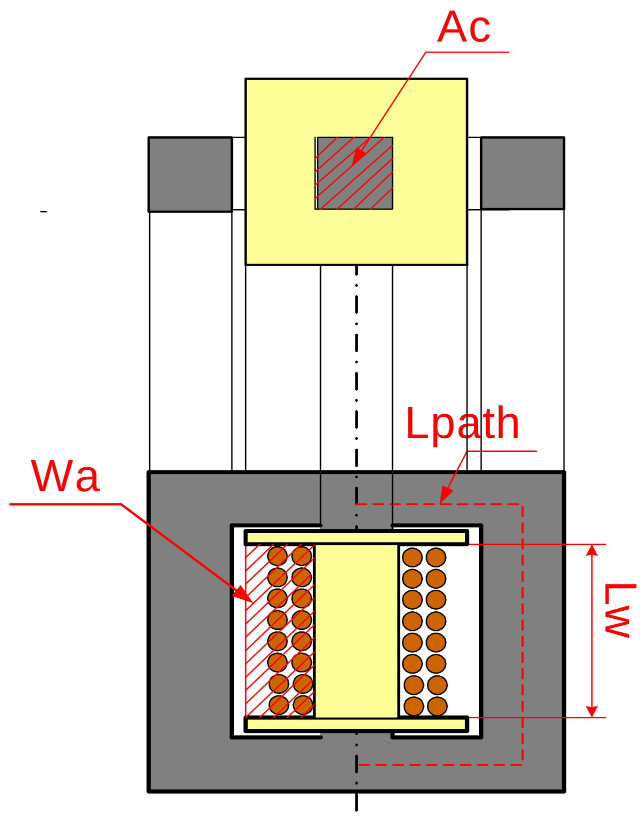
$$\theta ja := \frac{Tj_{max} - Ta_{max}}{Pmosfet_{tot}} \qquad \theta ja = 75.73 \frac{1}{watt} \text{ Celsius}$$

If the thermal resistance calculated is lower than that one specified on the MOSFET's data sheet a heat sink or higher copper area is needed.
For Example for a T0-263 (D2pak) package the Theta ja of the MOSFET versus copper plane area is:



11) Transformer design





The power handling capacity of the transformer core can be determined by its WaAc product area , where Wa is the available core window area, and Ac is the effective core cross-selectional area.
The WaAc power output relationship is obtained with the Faraday's law:

E = 4 B Ac Nf 10^-8

Where:

E = applied voltage	J = current density amp/cm^2
B = flux density in gauss	K = winding factor
Ac = core area in cm^2	(magnetic cross-section area)
Wa = window area in cm^2	(window area available for the winding)
I = current (rms)	f = frequency
N = number of turns	Po = output power

-Select maximum current density of the windings: J (280- 390 amp/cm^2, or 400-500 circular-mils/amp)

$J := 390 \cdot \frac{amp}{cm^2}$ $\qquad$ $cir\_mil := 5.07 \cdot 10^{-6} \cdot cm^2$ $\qquad$ $\frac{1}{J} = 505.74 \frac{cir\_mil}{amp}$

- winding factor: $\qquad$ $Kxxx := 0.5$

-Select core material and maximum flux density:

It is assumed that at high switching frequency (fsw>>25KHz) the limitation factor is the core losses, and temperature rise of the transformer
The type of ferrite material chosen will influence the core losses at the given operating conditions:
- F material has its lowest losses at room temperature to 40°C.
- P material has lowest losses at 70°C-80°C.
- R material has lowest losses at 100°C-110°C.
- K material has lowest losses at 40°C-60°C at elevated frequencies.

At high switching frequency it is necessary to adjust the flux density in order to limit core temperature rise.

Limiting core loss density to 100mW/cm^3 would keep the temperature rise at approximately 40°C.
Use the following formula to select the most appropriate maximum flux density:

-Maximum core loss density: $Pcored := 75$ mW/cm^3

for P material:

a = 0.158	b = 1.36	c = 2.86	for frequency f<100kHz
a = 0.0434	b = 1.63	c = 2.62	for frequency 100kHz<f<500kHz
a = 7.36*10^-7	b = 3.47	c = 2.54	for frequency f>500kHz

for K material:

a = 0.0530	b = 1.60	c = 3.15	for frequency f<500kHz
a = 0.00113	b = 2.19	c = 3.10	for frequency 500kHz<f<1 MHz
a = 1.77*10^-9	b = 4.13	c = 2.98	for frequency f>1MHz

$a1 := 0.158$ $b1 := 1.36$ $c1 := 2.86$

$$B := \left[\frac{Pcored}{a1\cdot\left(\frac{fsw}{kHz}\right)^{b1}}\right]^{\frac{1}{c1}}\cdot 10^3\cdot gauss \qquad B = 624.49\ gauss$$

===> $\Delta B := B\cdot 2$ $\qquad \Delta B = 1.25\times 10^3\, gauss$

-Topology constant:

$$Kt := \frac{0.0005}{1.97}\cdot 10^3$$

$$WaAc := \frac{Po_{max}}{Kt\cdot\Delta B\cdot fsw\cdot J} \qquad WaAc = 0.22cm^4$$

- Select a core with area product larger than : ---> $WaAc = 0.22cm^4$

Core selected:

- Manufacture: Magnetics
- Material: P
- Shape: E core
- Part number: EFD30-3C90
- Core Area: Ac
- Bobbin area: Wa
- Core volume: Ve
- Window length: lw (length of the bobbin)
- Area product Used --->
- Inductance per 1000 turns without airgap :
- first turn-length:

$Ac := 0.69\cdot cm^2$ $\qquad Wa := 0.520\cdot cm^2$

$lw := 2.01\cdot cm$ $\qquad Ve := 4.7\cdot cm^3$

$Ac\cdot Wa = 0.36cm^4$ $\qquad Lt := 4.8\cdot cm$ $\qquad 1.6\cdot in = 4.06cm$

-
Magnetic Path Length: Lpath $\qquad Lpath := 6.8\cdot cm$

Core permeability: $\qquad \mu_r := 1720$

- Primary turns

$$Np_c := \frac{(Vi_{min} - Vds_{on}) \cdot T_{ch} \cdot D_{max}}{\Delta B \cdot Ac}$$ $Np_c = 11.79$ turns

The number of turns has to be rounded to the higher or lower integer value: $Np := 12$

- Secondary turns

$$Ns1_c := \left(\frac{Vo1 \cdot T_{ch}}{2 \cdot Ton_{max}} + Vd_{fw} \right) \cdot \frac{Np}{(Vi_{min} - Vds_{on})}$$ $Ns1_c = 5.98$ turns

The number of turns has to be rounded to the higher or lower integer value: $Ns1 := 6$

$$Ns2_c := \left(\frac{Vo2 \cdot T_{ch}}{2 \cdot Ton_{max}} + Vd_{fw} \right) \cdot \frac{Np}{(Vi_{min} - Vds_{on})}$$ $Ns2_c = 2.06$ turns

The number of turns has to be rounded to the higher or lower integer value: $Ns2 := 2$

- Primary inductance: $\mu_o := 4 \cdot \pi \cdot 10^{-7} \frac{henry}{m}$

$$Lp2 := \frac{Ac \cdot Np^2 \cdot \mu_o \cdot \mu_r}{Lpath}$$ $Lp2 = 315.82 \mu H$

- Magnetizing current:

$$I_{mag} := \frac{Vi_{min} \cdot Ton_{max}}{Lp2}$$ $I_{mag} = 0.32 amp$

Usually the magnetizing current is small enough to ignore when sizing the switching transistors and primary winding. It is typically less than 10% of the reflected load current.

- Primary and secondary wire size:

Maximum current density: $J = 390 \frac{amp}{cm^2}$

Primary rms current: $Ip_{rms} = 1.67 amp$

Primary:

by wire area:

$$Wp_{cu} := \frac{Ip_{rms}}{J}$$ $Wp_{cu} = 4.29 \cdot 10^{-3} \cdot cm^2$

or by wire size:

$$AWGp := -4.2 \cdot \ln \left(\frac{Wp_{cu}}{cm^2} \right)$$ $AWGp = 22.9$

(Approximated AWG wire size, for more precision refer to wire size table)

Primary Wire selected:

Wire size: $AWG_{Lp} := 21$

Bare area (copper plus insulation): $Wa_{Lp} := 4.84 \cdot 10^{-3} \cdot cm^2$

Copper area: $Wcu_{Lp} := 4.12 \cdot 10^{-3} \cdot cm^2$

Diameter: $Dcu_{Lp} := 0.078 \cdot cm$

Number of strands: $Nst_{Lp} := 1$

- Number of primary turns per layer:

$$Ntl_{Lp} := \mathrm{floor}\left(\frac{lw}{Dcu_{Lp}}\right) \qquad Ntl_{Lp} = 25$$

- Number of primary layers:

$$Nly_{Lp} := \mathrm{ceil}\left(\frac{Np \cdot Nst_{Lp}}{\frac{Ntl_{Lp}}{2}}\right) \qquad Nly_{Lp} = 1$$

(total layers for two primary windings)

Secondary: Master

by wire area:

$$Ws1_{cu} := \frac{Is1_{rms}}{J} \qquad Ws1_{cu} = 7.7510^{-3} \cdot cm^2$$

or by wire size:

$$AWGs1 := -4.2 \cdot \ln\left(\frac{Ws1_{cu}}{cm^2}\right) \qquad AWGs1 = 20.41$$

Secondary Wire selected:

Wire size: $AWG_{Ls1} := 21$

Bare area (copper plus insulation): $Wa_{Ls1} := 4.84 \times 10^{-3} \cdot cm^2$

Copper area: $Wcu_{Ls1} := 4.12 \cdot 10^{-3} \cdot cm^2$

Diameter: $Dcu_{Ls1} := 0.078 \cdot cm$

Number of strands: $Nst_{Ls1} := 2$

- Number of secondary turns per layer:

$$Ntl_{Ls1} := \mathrm{floor}\left(\frac{lw}{Dcu_{Ls1}}\right) \qquad Ntl_{Ls1} = 25$$

- Number of secondary layers:

$$Nly_{Ls1} := \mathrm{ceil}\left(\frac{Ns1 \cdot Nst_{Ls1}}{\frac{Ntl_{Ls1}}{2}}\right) \qquad Nly_{Ls1} = 1$$

(total layers for two secondary windings)

Secondary: Slave

by wire area:

$$Ws2_{cu} := \frac{Is2_{rms}}{J} \qquad Ws2_{cu} = 0.7710^{-3} \cdot cm^2$$

or by wire size:

$$AWGs2 := -4.2 \cdot \ln\left(\frac{Ws2_{cu}}{cm^2}\right) \qquad AWGs2 = 30.09$$

Secondary Wire selected:

Wire size: $AWG_{Ls2} := 30$

Bare area (copper plus insulation): $Wa_{Ls2} := 0.67 \cdot 10^{-3} \cdot cm^2$

Copper area: $Wcu_{Ls2} := 0.50 \cdot 10^{-3} \cdot cm^2$

Diameter: $Dcu_{Ls2} := 0.0294 \cdot cm$

Number of strands: $Nst_{Ls2} := 1$

- Number of secondary turns per layer:

$$Ntl_{Ls2} := \mathrm{floor}\left(\frac{lw}{Dcu_{Ls2}}\right) \qquad Ntl_{Ls2} = 68$$

- Number of secondary layers:

$$Nly_{Ls2} := \mathrm{ceil}\left(\frac{Ns2 \cdot Nst_{Ls2}}{\frac{Ntl_{Ls2}}{2}}\right) \qquad Nly_{Ls2} = 1$$

- Copper area:

$$Wcu_{tot} := \left(Dcu_{Lp} \cdot Nly_{Lp} + Dcu_{Ls1} \cdot Nly_{Ls1} + Dcu_{Ls2} \cdot Nly_{Ls2}\right) \cdot 1.15 \cdot lw \qquad Wcu_{tot} = 0.43cm^2$$

- Window utilization:

$$Wu := \frac{Wcu_{tot}}{Wa} \qquad Wu = 82.41\%$$

Important: if the window utilization is greater than 95%, (copper area>> than bobbin area) a core with larger window area, or smaller wire sizes must be selected. (In push-pull the transformer has two primary and two secondary windings)

- Core losses:

$$Pcore := Ve \cdot \left[\left(\frac{B}{10^3 \cdot gauss}\right)^{c1} \cdot a1 \cdot \left(\frac{fsw}{kHz}\right)^{b1}\right] \cdot \frac{10^{-3} \cdot watt}{cm^3} \qquad Pcore = 0.35watt$$

- Winding copper losses:

There are two effects that can cause the winding losses to be significantly greater than (I^2*Rcu). These are

skin and proximity effects.
The skin effect causes current in a wire to flow only in the thin outer skin of the wire.
The skin depth is the distance below the surface where the current density has fallen to 1/e of its value at the surface: (Sd)

$$Sd := \frac{6.61}{\sqrt{\frac{fsw}{Hz}}}\cdot cm \qquad Sd = 0.01cm$$

$$Lt = 4.8cm \qquad Nly_{Lp} = 1$$

To minimize the AC copper losses in a transformer, if the wire diameter is greater than two times the skin depth a multiple strand winding or litz wires should be considered.

If $Dcu_{Lp} = 0.08cm$ is greater than $Sd\cdot 2 = 0.03cm$

Primary winding length:

$$Ldf_{Lp} := \left| \begin{array}{l} L1 \leftarrow Lt \\ \text{for } i \in 1..\left(Nly_{Lp} - 1\right) \\ \quad L1 \leftarrow L1 + 4\cdot Dcu_{Lp} \\ L1 \end{array} \right.$$

$$Lcu_{Lp} := \left| \begin{array}{l} L1 \leftarrow Lt \\ L \leftarrow 0\cdot cm \\ \text{for } i \in 1..\left(Nly_{Lp} - 1\right) \\ \quad \left| \begin{array}{l} L \leftarrow L + L1\cdot Ntl_{Lp} \\ L1 \leftarrow L1 + 4\cdot Dcu_{Lp} \end{array} \right. \\ \left[L + L1\cdot\left[Np - \left(Nly_{Lp} - 1\right)\cdot Ntl_{Lp}\right]\right] \end{array} \right.$$

$Np = 12$ $\qquad Lcu_{Lp} = 312.89cm$

$Ldf_{Lp} = 5.42cm$

$7.15\cdot Np = 85.8$

Copper resistivity: (20C) $\qquad \rho_{20} := 1.724\cdot 10^{-6}\cdot ohm\cdot cm$

-Maximum temperature of the winding: $Tmax_{cu} := 80$

$$\rho := \rho_{20}\cdot\left[1 + 0.0042\cdot\left(Tmax_{cu} - 20\right)\right]$$

$$Rdc_{Lp} := \rho\cdot\frac{Lcu_{Lp}}{Wcu_{Lp}\cdot Nst_{Lp}} \qquad Rdc_{Lp} = 0.16ohm$$

$$Rac_{Lp} := \frac{Rdc_{Lp}\cdot\left(\frac{Dcu_{Lp}}{2\cdot Sd}\right)^2}{\left(\frac{Dcu_{Lp}}{2\cdot Sd}\right)^2 - \left(\frac{Dcu_{Lp}}{2\cdot Sd} - 1\right)^2} \qquad Rac_{Lp} = 0.29ohm$$

$$\frac{Rac_{Lp}}{Rdc_{Lp}} = 1.78$$

$$Pcu_{Lp} := Rdc_{Lp}\cdot\left(\frac{Ip_{dc}}{2}\right)^2 + Rac_{Lp}\cdot\left(\frac{Ip_{ac}}{2}\right)^2 \qquad Pcu_{Lp} = 0.3\,watt$$

Secondary winding length:

$$Ldf_{Ls1} := \left|\begin{array}{l} L1 \leftarrow Ldf_{Lp} \\ \text{for } i \in 1..\left(Nly_{Ls2} - 1\right) \\ \quad L1 \leftarrow L1 + 4\cdot Dcu_{Ls1} \\ L1 \end{array}\right.$$

$$Lcu_{Ls1} := \left|\begin{array}{l} L1 \leftarrow Ldf_{Lp} \\ L \leftarrow 0\cdot cm \\ \text{for } i \in 1..\left(Nly_{Ls1} - 1\right) \\ \quad \left|\begin{array}{l} L \leftarrow L + L1\cdot Ntl_{Ls1} \\ L1 \leftarrow L1 + 4\cdot Dcu_{Ls1} \end{array}\right. \\ L \leftarrow 0 \text{ if } Nly_{Ls1} \leftarrow 1 \\ \left[L + L1\cdot\left[Ns1 - \left(Nly_{Ls1} - 1\right)\cdot Ntl_{Ls1}\right]\right] \end{array}\right.$$

$$Lcu_{Ls1} = 36.29\,cm$$

$$Rdc_{Ls1} := \rho\cdot\frac{Lcu_{Ls1}}{Wcu_{Ls1}\cdot Nst_{Ls1}} \qquad Rdc_{Ls1} = 9.51\times 10^{-3}\,ohm$$

$$Rac_{Ls1} := \frac{Rdc_{Ls1}\cdot\left(\frac{Dcu_{Ls1}}{2\cdot Sd}\right)^2}{\left(\frac{Dcu_{Ls1}}{2\cdot Sd}\right)^2 - \left(\frac{Dcu_{Ls1}}{2\cdot Sd} - 1\right)^2} \qquad Rac_{Ls1} = 0.02\,ohm$$

$$\frac{Rac_{Ls1}}{Rdc_{Ls1}} = 1.78$$

$$Pcu_{Ls1} := Rdc_{Ls1}\cdot\left(\frac{Io1_{max}}{2}\right)^2 + Rac_{Ls1}\cdot\left(\frac{Is1_{ac}}{2}\right)^2 \qquad Pcu_{Ls1} = 0.08\,watt$$

$$Lcu_{Ls2} := \left|\begin{array}{l} L1 \leftarrow Ldf_{Ls1} \\ L \leftarrow 0\cdot cm \\ \text{for } i \in 1..\left(Nly_{Ls2} - 1\right) \\ \quad \left|\begin{array}{l} L \leftarrow L + L1\cdot Ntl_{Ls2} \\ L1 \leftarrow L1 + 4\cdot Dcu_{Ls2} \end{array}\right. \\ L \leftarrow 0 \text{ if } Nly_{Ls2} \leftarrow 1 \\ \left[L + L1\cdot\left[Ns2 - \left(Nly_{Ls2} - 1\right)\cdot Ntl_{Ls2}\right]\right] \end{array}\right.$$

$$Lcu_{Ls2} = 12.57\,cm$$

$$Wcu_{Ls2} = 5\times 10^{-8}\,m^2 \qquad Nst_{Ls2} = 1$$

$$Rdc_{Ls2} := \rho \cdot \frac{Lcu_{Ls2}}{Wcu_{Ls2} \cdot Nst_{Ls2}}$$ $Rdc_{Ls2} = 0.05\,ohm$

$$Rac_{Ls2} := \frac{Rdc_{Ls2} \cdot \left(\frac{Dcu_{Ls2}}{2 \cdot Sd}\right)^2}{\left(\frac{Dcu_{Ls2}}{2 \cdot Sd}\right)^2 - \left(\frac{Dcu_{Ls2}}{2 \cdot Sd} - 1\right)^2}$$ $Rac_{Ls2} = 0.05\,ohm$

$Pcu_{Ls2} := Rdc_{Ls2} \cdot Io2_{max}^2 + Rac_{Ls2} \cdot Is2_{ac}^2$ $Pcu_{Ls2} = 0.02\,watt$

$Pcu_{tot} := Pcu_{Lp} + Pcu_{Ls1} + Pcu_{Ls2}$ $Pcu_{tot} = 0.4\,watt$

-Total transformer losses:

$Ptrans_{tot} := Pcu_{tot} + Pcore$ $Ptrans_{tot} = 0.75\,watt$

-Transformer efficiency:

$$\eta_{Tra} := \frac{Po_{max}}{Po_{max} + Ptrans_{tot}}$$ $\eta_{Tra} = 98.89\%$

12) Total power supply efficiency

$Ptrans_{tot} = 0.75\,watt$ $Pdiode_{tot} = 4.95\,watt$ $Pmosfet_{tot} = 0.66\,watt$

(each phase)

$Pout := Vo1 \cdot Io1_{max} + Vo2 \cdot Io2_{max}$ $R_{L1} := 0.085\Omega$

-Input Inductor losses:

$Pinput_{inductor} := R_{L1} \cdot Idc^2$ $Pinput_{inductor} = 0.31\,watt$

-Board losses, current sense losses: (Estimated value) $P_{pcb} := 1 \cdot watt$

$$\eta_{tot} := \frac{Pout}{Pout + Ptrans_{tot} + Pdiode_{tot} + Pmosfet_{tot} \cdot 2 + Pinput_{inductor} + P_{pcb}}$$ $\eta_{tot} = 88.13\%$

-Total Power Losses:

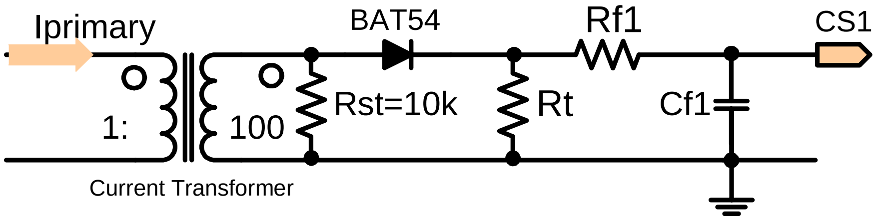
$P_{loss} := Ptrans_{tot} + Pdiode_{tot} + Pmosfet_{tot} \cdot 2 + Pmosfet_{tot} + P_{pcb}$ $P_{loss} = 8.68\,watt$

13) Selecting the proper switching frequency

The operating frequency of the power supply should be selected to obtain the best balance between switching losses, total transformer losses, size and cost of magnetic components and output capacitors.
High switching frequency reduces the output capacitor value and the inductance of the primary and secondary windings, and therefore the total size of the transformer.
In the same manner, higher switching frequency increases the transformer losses and the switching losses of the switching transistor. These high losses reduce the overall efficiency of the power supply, and increase the size of the heat-sink required to dissipate the heat.

14) Current limit

The LM5030 contains two levels of over current protection: cycle by cycle current limit (0.5volt) and hiccup mode (0.6volt)



Current transformer: Pulse P8208Turns ratio: $CT_{tr} := 100$

- Primary peak current:

$$Ip_{peak} := Ip_{ft} + \frac{Vi_{nom} \cdot T_{ch} \cdot Dnom}{2 \cdot Lp2}$$ $Ip_{peak} = 2.92amp$

- Primary current limit set: $I_{limit} := 3.2amp$

-Terminating resistor:

$$Rt := \frac{0.5volt \cdot CT_{tr}}{I_{limit}}$$ $Rt = 15.63ohm$

- Rst = 10K resistor to reset the core

- Rf&Cf: Current sense filter

Notes:

Wire table:

AWG Wire Size	Bare Area cm^2 10^-3	Area cm^2 ^-3	Diameter cm
18	8.23	9.32	0.109
19	6.53	7.54	0.098
20	5.188	6.065	0.0879
21	4.116	4.837	0.0785
22	3.243	3.857	0.0701
23	2.588	3.135	0.0632
24	2.047	2.514	0.0566
25	1.623	2.002	0.0505
26	1.28	1.603	0.0452
27	1.021	1.313	0.0409
28	0.8046	1.0515	0.0366
29	0.647	0.8548	0.033
30	0.5067	0.6785	0.0294
31	0.4013	0.5596	0.0267

32	0.3242	0.4559	0.0241
33	0.2554	0.3662	0.0216
34	0.2011	0.2863	0.0191
35	0.1589	0.2268	0.017
36	0.1266	0.1813	0.0152
37	0.1026	0.1538	0.014
38	0.08107	0.1207	0.0124
39	0.06207	0.0932	0.0109
40	0.04869	0.0723	0.0096

References:

1. Magnetics application notes.
2. Colonel Wm. T. McLyman "Transformer and Inductor Design Handbook"
3. J Riche, High temperature power supply design (*2)
4. Pressman "Switching Power Supply Design" (*1)