Mains frequency generator

H. Nacinovich, Gulgong NSW

This circuit was designed to operate a 240 V/3 W telescope drive motor but it would be suitable for many other low power applications. It could also provide the basis for a high power version, with suitable modification to the output stage.

For its present purpose, the most important requirement is for a highly stable, 50 Hz operating frequency. This is achieved by using a 3.5795 MHz crystal and an MM5369EYRN IC, which were chosen for their low cost and ready availability. The MM5369EYRN IC contains an oscillator and all the divider circuitry necessary to produce a precise 50 Hz square wave output when used in conjunction with the 3.5795 MHz crystal.

One disadvantage of this IC, however, is that its output is not an exact 50/50 duty cycle square wave. For some applications this may not matter but, if used directly to drive an output stage in a high power convertor, for example, the asymmetrical waveform could result in significant unbalanced dc currents sufficient to saturate the output transformer. Also, for high power convertor applications, at least, it is desirable to drive the output transistors (usually in push-pull) with a delay between turn-off of one set of output transistors and turn-on of its complementary set of transistors.

This circuit provides both a symmetrical drive current waveform to the output transistors and the delay referred to above. This is achieved using only two low cost, easily obtainable ICs, a 4046 CMOS phase lock loop and a 4022 octal counter.

The counter is arranged in a feedback loop with the 4046 in such a way that the output is locked precisely to the 50 Hz input derived from the 5369 IC. The 4022 has, in fact, eight outputs which go sequentially high when the counter is clocked. In this case the 4022 is connected as a divide-by-6 counter, with four of its outputs being used to supply input drive to transistors Q1, Q2. The sequential operation of the 4022 outputs is taken advantage of here to obtain the waveforms shown in the diagram without the need for any extra gating. The idealised ac output waveform has a 4:2 on/-off ratio which gives a theoretical peak/rms ratio similar to that for a sine voltage waveform.

The output section is conventional. It comprises a pair of transistors Q1, Q2 in push-pull driving a pair of output transistors Q3, Q4 respectively, which in turn are coupled to an output transformer, T1. The transistors Q1, Q2 are ac coupled to the 4022 outputs, rather than dc coupled, to ensure that all the transistors are turned off in case oscillation ceases for any reason, e.g: in case of a fault.

The output transformer is a commonly available type with a 240 V/15 V centre-tapped winding ratio which, assuming a 12 V battery supplying the circuit, will theoretically give a 384 V peak (256 RMS). In practice an output closer to 360 V peak (240 V RMS) is obtained due to circuit losses.

Maximum continuous output power is around 10 W. If higher output power is required it will be necessary to substitute a suitably rated transformer and output transistors with correspondingly increased current/power ratings. It may also be necessary to use Darlington output pairs to obtain the increased output current.

Diodes D3, D4 and a series RC network across the transformer secondary minimise switching spikes in the ac output. Some experimentation with the values of C_X, R_X may be necessary for optimum suppression depending on transformer type and output loads.