Watchdog circuit protects against loss of battery charger's control signals

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Recharging a mobile phone's internal battery usually occurs under control of a proprietary charging algorithm that resides in the baseband controller. The charger connects to the internal battery through a P-channel-MOSFET switch of low on-resistance (**Figure 1**). A baseband controller supplies a PWM signal that drives the switch. To minimize power dissipation and consequent thermal problems in the phone, the charging supply—usually a plug-in transformer assembly—features internal current limiting and has specifications that correspond to the battery's chemistry and charge-recovery requirements.

However, if the baseband processor stalls for any reason, the nearly direct charger-to-battery connection could damage the battery. To circumvent the problem, another circuit monitors the charger's PWM input and disables the series power switch after a predetermined delay interval (**Figure 2**). The circuit operates independently of the baseband unit's processor and allows charging to resume when the PWM signal returns.

In this circuit, microprocessor supervisor IC_1, a Maxim MAX6321 that includes a watchdog circuit that can monitor software execution, drives IC_2, a normally open SPST analog switch. Components R_4, D_2, and C_1 protect IC_1 and IC_2 by limiting V_{CC} to a maximum of 5.1V. Resistor R_4's value isn't critical because the protection circuit's quiescent current is low at approximately 30 μA. Select R_4 to provide just enough current—for example, 0.5 mA—to bias zener diode D_1 into the "knee" of its characteristic V-I curve.

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The protection circuit consumes no power except when the battery undergoes charging and therefore doesn't burden the battery. Supervisor IC_1 provides a $\overline{RESET}$ output that can serve as a charger-ready interrupt input to the baseband-controller CPU. The $\overline{RESET}$ output's open-drain structure allows its connection to other circuits that operate from different supply voltages. Supplying power to the watchdog and PWM circuits only during charging also prevents reverse current from flowing into the IC_1's $\overline{RESET}$ output and discharging the battery via a sneak path.

The timing diagram illustrates the circuit's operation when an active

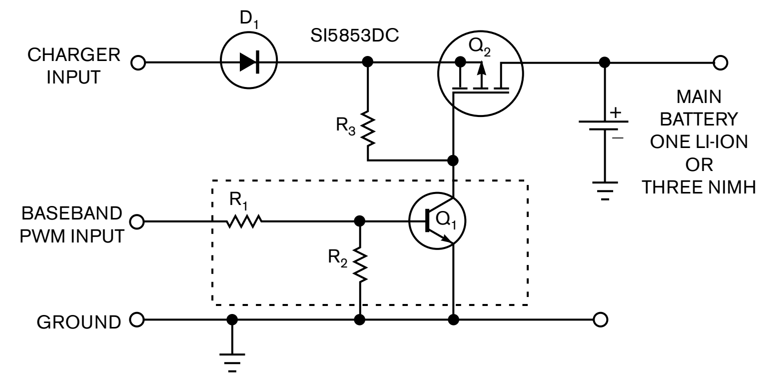


Figure 1 A typical mobile phone's battery-charger input circuit comprises a series switch controlled by a PWM signal.

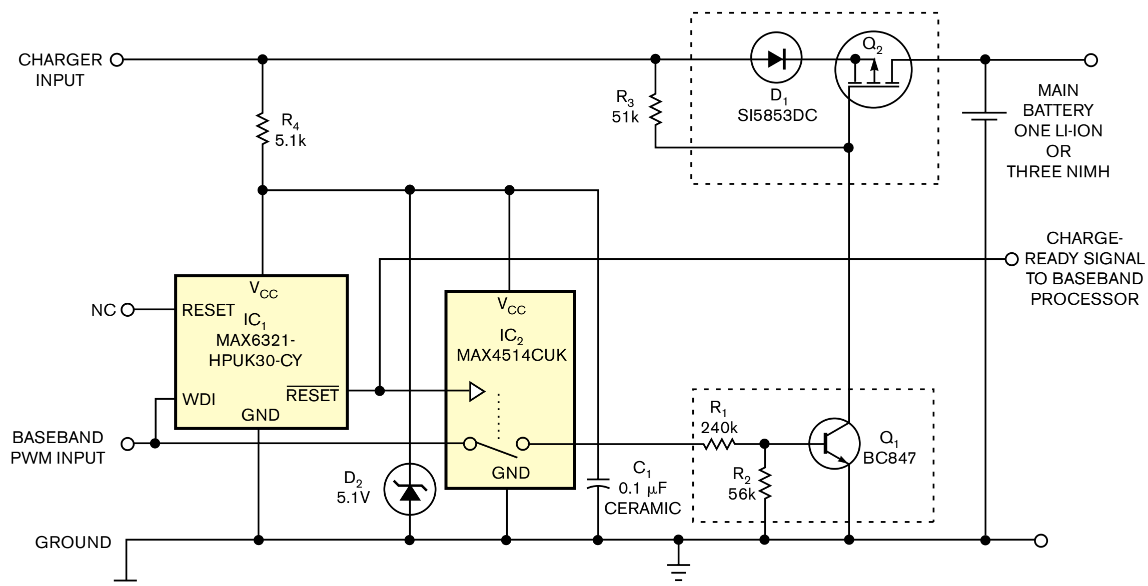
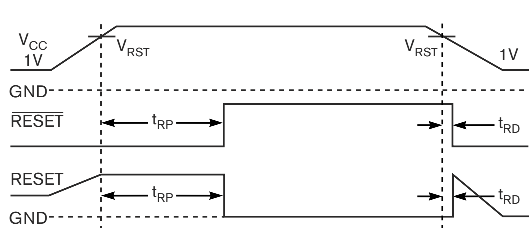
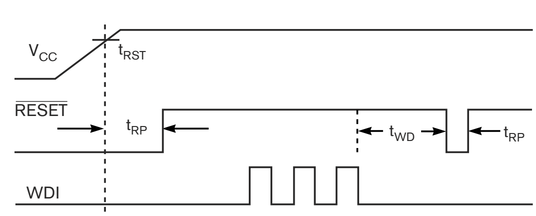


Figure 2 Adding watchdog protection to the circuit of Figure 1 guards against battery damage when the baseband processor stalls or ceases software execution.



NOTES:
t_{RP}=RESET-ACTIVE-TIME-OUT PERIOD (200 mSEC).
t_{RD}=RESET-DELAY TIME FROM V_{CC} (40 µSEC).

Figure 3 Reset-timing relationships for the circuit of Figure 2 illustrates its power-on behavior.



NOTES:
t_{WD}=WATCHDOG-TIME-OUT PERIOD (1.6 SEC).
t_{RP}=RESET-ACTIVE-TIME-OUT PERIOD (200 mSEC).

Figure 4 When PWM pulses cease, the watchdog circuit disables the charger after a 1.6-sec interval.

charger connects to the phone's charger-input socket (**Figure 3**). In this example, the MAX6321-HPUK30-CY that IC_1 uses is factory-trimmed for a 3V reset threshold, and the -CY suffix indicates complementary reset outputs and a 1.6-sec delay interval. The reset interval begins when V_{CC} reaches 3V±45 mV. After 200 msec, RESET goes low, and $\overline{\text{RESET}}$ goes high.

The $\overline{\text{RESET}}$ output releases the SPST analog switch, IC_2, which enables the PWM input. Meanwhile, the active WDI (watchdog input) monitors the PWM input signal. If no signal transitions occur within 1.6 sec, the RESET and $\overline{\text{RESET}}$ outputs become active, disabling the PWM input and pausing the charger algorithm using a CPU interrupt that the charger-ready signal conveys (**Figure 4**). All active and passive components for the circuit are available in surface-mount packages. Pass transistor Q_2, a Siliconix-Vishay SiS5853, includes an integrated Schottky diode, D_1.EDN