Ramp generator

A POSITIVE ramp can be generated by dumping charges on a capacitor. The amount of charge deposited after $t = {}^{n+1}$ pulses will be $Q = It$. After five seconds $5 \times 10^{-4}Q$ will have been dumped on the capacitor which increases its volume from $V_0 = It/C$ to $V_1 = It^{n+1}/C$. This voltage is stored on the capacitor and decreases by an amount V_d which is determined by the internal resistance of the capacitor and the f.e.t. gate leakage current. Without any load to the capacitor the voltage across it will decrease by $9/10^{-n}$V/min.. To obtain an output voltage which has little influence on the charge or discharge of the capacitor, a 741 with a high impedance duel f.e.t. input is used. The circuit shown generates a ramp from 0 to 5.3V.

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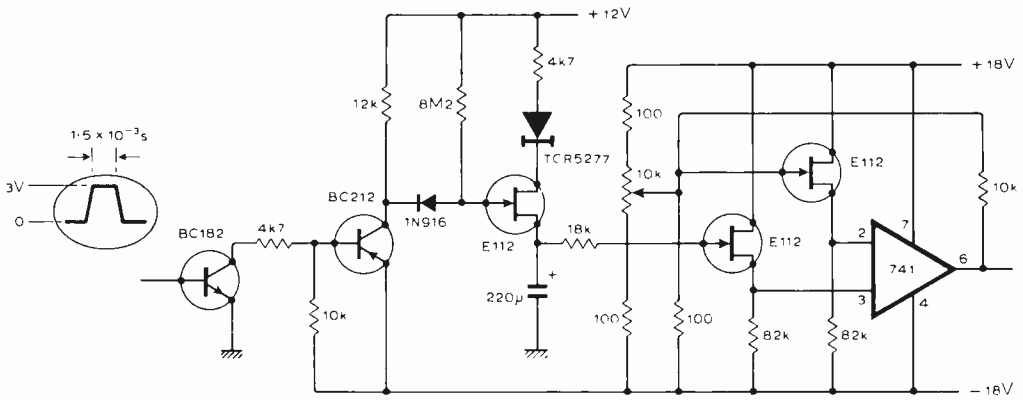

Analogue divider and multiplier

THE only non-linear device in this analogue divider/multiplier is a field effect transistor. The principle of the divider is simple, consider the quotient $Q_1 = A/B$. If the numerator and denominator of the quotient are multiplied by a factor K so that $KB = 1$ or any other constant, then the value of the quotient is equal to KA. In the circuit the numerator and denominator pass through a buffer amplifier before being modulated. The prototype used field-effect transistors driven by two 180° out-of-phase pulse trains with a mark-to-space ratio of slightly less than unity which suppresses unwanted spikes. The modulated numerator and denominator signals are then passed through an adding amplifier before being processed by the variable attenuator, buffer amplifier, and demodulators.

The signal in the denominator channel then passes through a low-pass filter with a built-in d.c. gain, before being compared with the voltage V_c ($\equiv KB$) in the integrator. The resulting signal is then applied to the field-effect transistor in the variable attenuator.

In the prototype, V_c was set to 10V and the d.c. gain in the low-pass filter was 60dB so that the drain-source voltage of the field-effect transistor was always less than or equal to 10mV. This low drain-source voltage is desirable because the f.e.t. operation is restricted to the linear part of its characteristics. A f.e.t. selected for low on-resistance should be used to prevent the use of an unreasonably large series resistor.

Note that the response time of the circuit depends on the size of the capacitors used in the low-pass filter and integrator. Response time can be reduced by raising the modulating frequency. For accurate division, zero offset controls are needed for $IC_{1,2,3}$ and IC_5.

Also, an f.e.t. input op-amp should be used for IC_4 to suppress offsets caused by its variable source impedance. In the prototype the accuracy was limited by the use of optical modulation to within ±0.5%. However, the author feels that this figure could be improved.

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