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Scheme yields frequency-locked triangle waves

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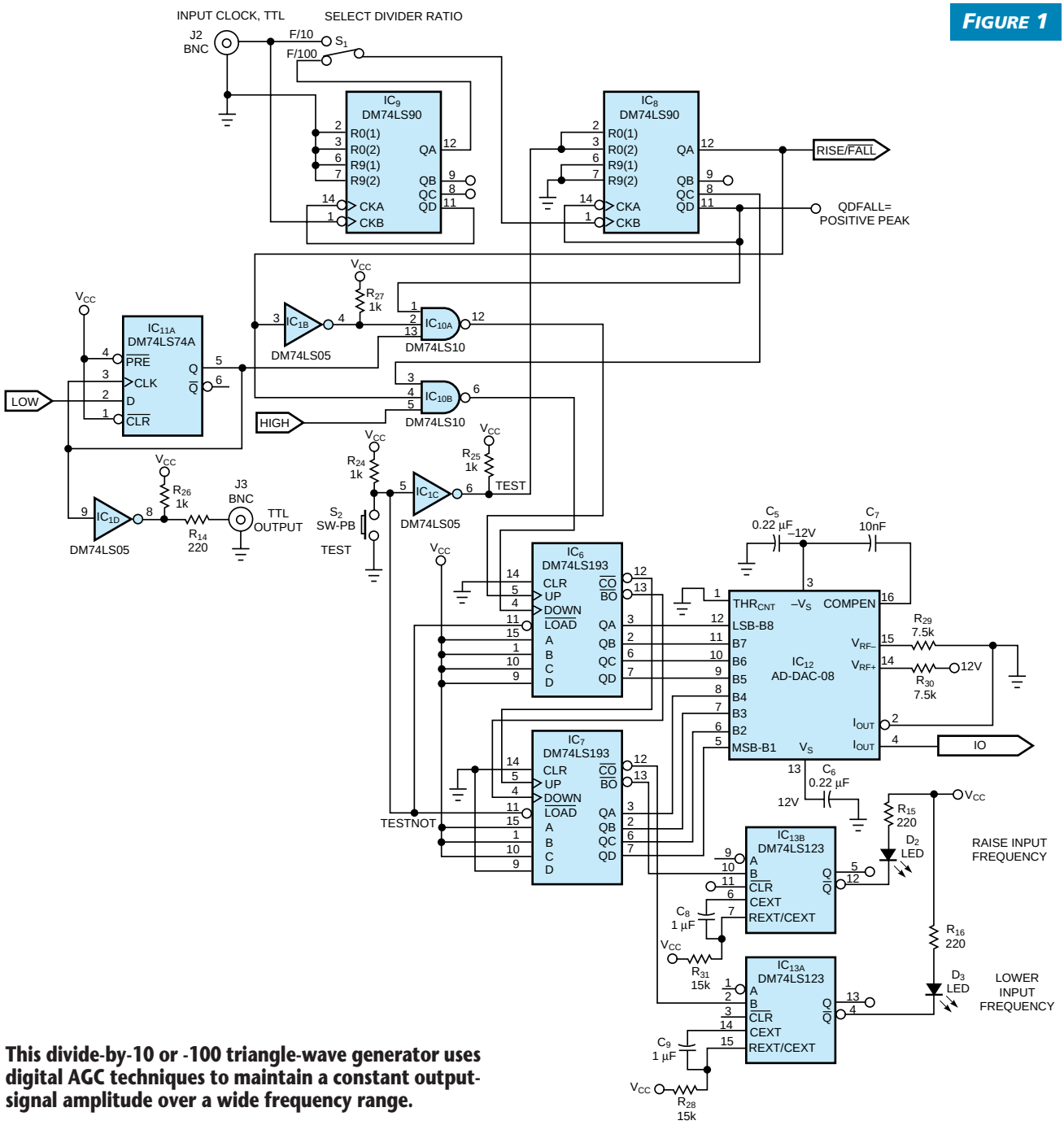
The circuit in **Figures 1** and **2** generates frequency-locked triangle waves of constant amplitude. It uses readily available TTL and other older-technology parts. The circuit portion in **Figure 1** comprises the frequency dividers, counters, and converter. The portion in **Figure 2** contains current sources, output circuits, and comparators. The circuit satisfies a need

FIGURE 1



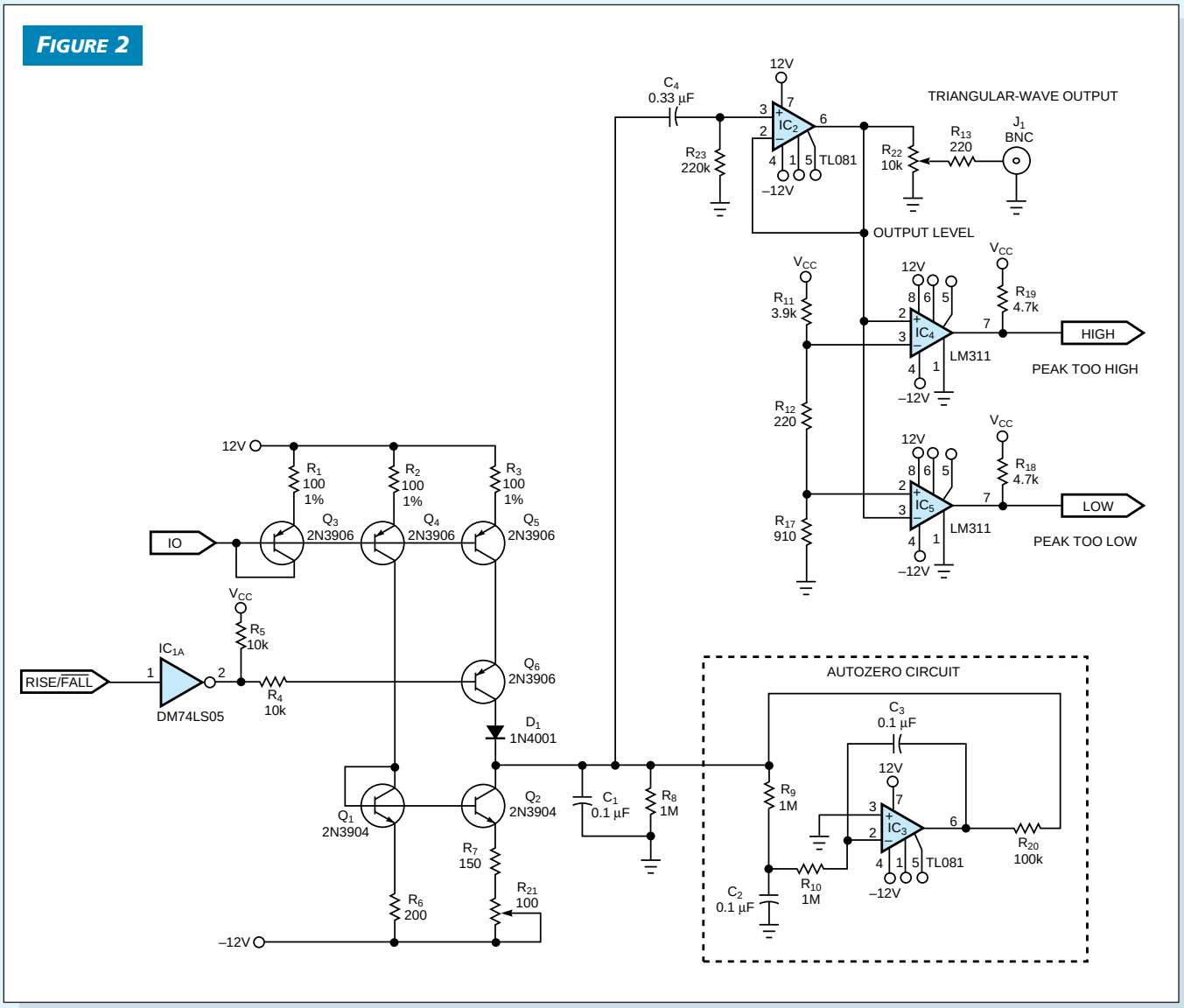
This divide-by-10 or -100 triangle-wave generator uses digital AGC techniques to maintain a constant output-signal amplitude over a wide frequency range.

for a triangle wave of approximately constant amplitude, at a frequency exactly one-tenth or $^1/_{100}$ that of an input TTL clock. The input frequency can vary over a wide range before the circuit loses lock. The triangle-wave output frequency ranges from 250 Hz to 2.5 kHz. Two decade dividers divide the input clock by 10 or 100. Switch S_1 selects the divider ratio. The signal RISE/$\overline{\text{FALL}}$ is a 50%-duty-cycle wave that turns on a 2I current source, comprising transistors Q_3, Q_4, and Q_5; a –I current source comprising Q_1 and Q_2 is always on.

After you initially adjust R_{21}, op amp IC_3 keeps any dc offset (caused by tracking imbalances between the current source and sink) to a minimal value. The output signal from the 8-bit DAC, IC_{12}, controls the current level in both the source and sink. The currents sum on capacitor C_2, thus generating a triangle wave. An op amp buffers the triangular signal; potentiometer R_{22} adjusts the output level. Assuming a fixed input frequency and a fixed capacitor value, you can adjust the current sources for the desired amplitude.

If the frequency decreases, the triangle-wave amplitude increases. To keep the amplitude constant, comparator IC_4 detects that the positive-peak amplitude is too high. The comparator sends input-clock signals to decrement the 8-bit counter IC_6 and IC_7, thus controlling the source- and sink-current value through the DAC. Similarly, if you raise the clock frequency, the triangle-wave amplitude decreases. Comparator IC_5 detects that the positive-peak amplitude at the end of the triangle wave's rise is too low. IC_{11a} latches the comparator output and gates clock pulses to increase the count and the source- and sink-current values.

FIGURE 2



A companion to Figure 1's converter, this block contains the supporting current sources, output circuits, and comparators.

If you run out of counts on IC_6 and IC_7, the carry and borrow output signals trigger the monostables, IC_{13A} and IC_{13B}. LED D_2 or D_3 lights to warn you to change the input frequency accordingly. Frequency tracking is asymmetric: As soon as the circuit detects the high limit, pulses decrement the counter. The sooner the high limit occurs, the more decrementing pulses the counter receives. However, you detect that the current is too low only when the RISE/$\overline{\text{FALL}}$ signal falls, and the triangular wave is still below the positive-peak low limit. This occurrence triggers a single pulse.

To adjust the circuit, set the divider to f/10, apply a 10-kHz TTL signal to the clock input, short-circuit C_2, push the TEST button, and adjust R_{22} for a zero-centered triangular wave. Release the TEST button, and remove the short circuit. You can increase the frequency range by using a bigger counter and a higher resolution DAC or by band-switching the current-summing capacitor, C_1, with some added logic that the borrow and carry outputs of IC_7 trigger. (DI #2127) EDN

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