Input Clock Adjusts Frequency Of Digital Ramp Generator

NICK IERFINO | IGS Technologies, Montreal, Quebec, Canada
NickI@IGSTechnologies.com

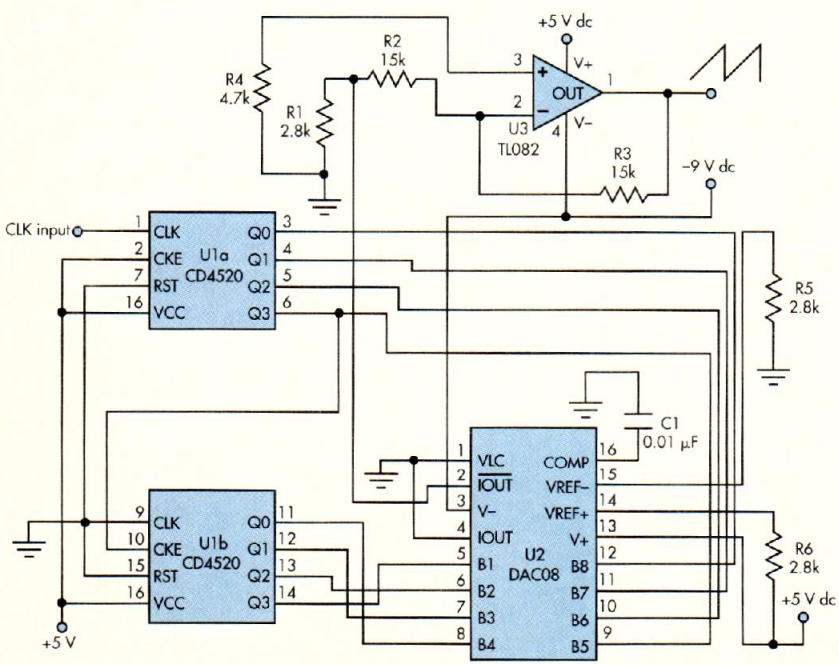
It's not always easy to design a ramp generator whose ramping frequency can be changed without manipulation of capacitors or inductors. Many ramp circuit designs are available, but they may not be flexible when it comes to varying the rise time. The digital ramp generator circuit in the figure, however, can vary the ramp frequency from less than 1 Hz to about 30 kHz just by varying the input clock from 100 Hz to about 6 MHz.

The output was measured at a voltage of 5 V peak, but it can be adjusted as well, by varying R1 and R6. Make sure the negative voltage driving the DAC08 8-bit high-speed multiplying digital-to-analog converter is greater than −8.5 V dc. If not, the rail-to-rail ramp doesn't go from 0 to 5 V.

This circuit can be modified to start at 0 and ramp up to any given voltage by adjusting the reset of the CD4520 dual up-counter. This can be useful in voltage-controlled-oscillator tracking circuits, where the rise time and input voltage are critical in the locking performance of a phase-locked loop.

NICK IERFINO, *senior engineer, holds a BSc Eng., telecommunications, from Concordia University, Montreal, Quebec, Canada, and a DEC in electrotechnology from Dawson College, Montreal.*

ED ONLINE 17663



To ensure that the rail-to-rail ramp goes from 0 to 5 V, the negative voltage driving the DAC08 must be greater than −8.5 V.