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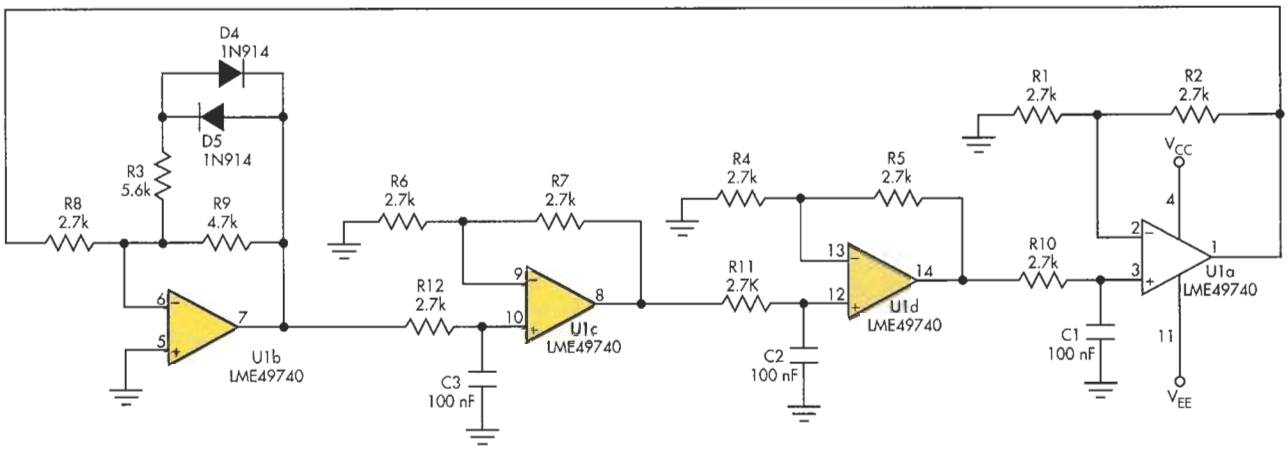
Oscillator Delivers Four Multi-Phased, Equal-Amplitude Sine Waves



1. This oscillator delivers four sine waves of equal amplitude with phase differences of 60° between each.

One application I recently dealt with needed multiple phases of sine waves, all of equal amplitude. I considered 45°, 60°, and 90° differences, but decided 60° was the best solution. I scoured the Internet for a circuit. Unfortunately, while multiple phases exist, and the topologies are legion, no topology offered sine waves of equal amplitude with a 60° phase shift.

I thought the solution would look like a common three-op-amp phase-shift oscillator, so that was my starting point. Three RC stages, all equal and running at a 60° phase delay, would sum to the 180° phase shift required for oscillation. For symmetry's sake, I used the fourth op amp in a quad device to buffer the final RC stage prior to feeding back to the summing amplifier. This way the feedback impedance doesn't load the RC oscillator and affect the phase shift of the last stage.

The first stab at the circuit had unity-gain buffers at each RC stage, similar to what I found as prior art. This is fine if you need a single sine wave. Unfortunately, using unity-gain buffers means that the amplitude of the sine wave is attenuated at every stage. I did a quick simulation of just a single RC low-pass filter and measured the amplitude response when the phase shift was 60°. I was surprised that it was −6 dB, a very convenient value. I changed each of the buffers to have a gain of 2 so that all of the sine waves were the same amplitude *(Fig. 1)*.

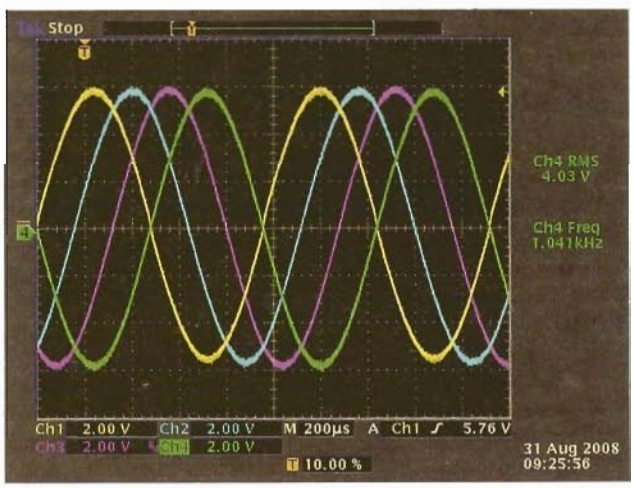
I did have to adjust the summing amplifier (U1b) to work best near unity gain. A nice benefit of this topology is that three op amps operate at 6 dB gain, and the summing amplifier operates at unity gain. The original circuit operated the summing amplifier near 18 dB, eroding its gain margin. The summing amplifier circuit works best when the two feedback resistances in parallel (R3 and R9) are slightly less than the source impedance (R8).

The amplitude of the oscillation is regulated by a pair of silicon diodes in the feedback of the summing amplifier. The diodes do add to the harmonic distortion, since they're nonlinear. However, each of the RC stages should attenuate these harmonics. Furthermore, my application didn't require low THD+N.

A simple equation determines the oscillation frequency:

$$f_{OSC} = \frac{1}{3.655 \times R \times C}$$

where f_{OSC} is the desired oscillation frequency, R is the value of resistors R10, R11, and R12, and C is the value of capacitors C1, C2, and



2. An oscilloscope measurement shows each phase 60° apart. Also, measurements confirmed that THD+N was reduced at each stage.

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C3. For the values shown in the circuit—2.7-kΩ resistors and 100-nF capacitors—the oscillation frequency is about 1 kHz. Keeping the resistor values low minimizes their thermal noise contribution.

The prototype used 5% resistors and capacitors of unknown tolerance (I assume about 10%). The oscillation frequency was exactly as predicted, as was the output amplitude, about 4.0 V rms. I chose a quad op amp, the LME49740, for its very low distortion, wide bandwidth, and excellent drive characteristics.

Figure 2 shows the circuit's time-domain response. Channel 1 (yellow trace) is from pin 7, channel 2 (blue) from pin 8, channel 3 (magenta) from pin 14, and channel 4 (green) from pin 1. Although the crossover of channel 1 is obscured by the other phases, it does have a slightly visible crossover distortion due to the diode level control. Indeed, the THD+N measured at this point was 2.1%. If your application requires lower distortion, a more complicated level-control circuit should be used. Examples of these circuits can be found in the application note at *www.national.com/an/AN/AN-263.pdf#page=2*.

The hypothesis that the THD+N would decrease from one amplifier to the next was verified. Measured at pin 7, it was 2.1%; at pin 8, 0.67%; at pin 14, 0.242%; and at pin 1, 0.090%. This was measured with a bandwidth of 22 Hz to 20 kHz. The reduction in THD+N from the summing amplifier to the final buffered RC stage was 27 dB.