Pulse Selector

064

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The circuit presented here can be useful in triggering, test and measurement applications. It converts a rising edge into a square pulse whose length is equal to the period of an input pulse train.

In the quiescent state, flip-flop IC1B is clear, holding flip-flop IC1A set.

A TTL-level rising edge at the SELECT input causes a brief spike to appear at the output of gate IC2D. The spike is only a few nanoseconds long, and depends on the propagation delay through NAND gates IC2A, IC2B and IC2C, which are connected as inverters.

The spike sets flip-flop IC1B. Its output (pin 9) goes high,

releasing the set input on flip-flop IC1A. This state is stable and persists after the trailing edge of the spike, IC1A remaining set.

However, the inverting output of IC1A is connected to its D input, and so the next positive edge arriving at the trigger input ('INPUT') clears it. The inverting output goes high and the non-inverting output goes low. On the next rising edge of INPUT IC1A is set again. The inverting output, connected to OUTPUT, goes low again, and the non-inverting output goes high. This rising edge on its clock in turn clears IC1B, since its D input is tied to ground. With IC1B cleared, IC1A is again held in the set state, and this situation will persist, independently of TRIGGER pulses, until the next SELECT edge arrives.

The result is that the output is high for one period of the input following the spike. The circuit works equally well with CMOS gates, although it should be observed that the spike must be short compared to the period of the input.

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