Bipolar and V-MOS hybrid delivers fast power pulses

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The major advantages afforded by the up-and-coming V-groove MOS transistor—low cost, moderate power capability, high-frequency operation, and immunity to mismatch—are utilized in this relatively inexpensive, compact pulser that, with the aid of two bipolar power transistors, will deliver a peak power of 5 kilowatts at widths as narrow as 20 nanoseconds. In terms of voltage and current, the unit can supply an output pulse of as much as 250 volts or 30 amperes.

This pulser overcomes the size, weight, and standby power limitations of vacuum tubes, the bulkiness and limited frequency response of charged delay lines, and the exponential fall rate and lack of constant output impedance that occur with silicon controlled rectifiers. Bipolar transistors that are fast enough cannot handle the current or voltage. The drawbacks are overcome by combining the bipolar transistors and V-MOS devices, which are fast but cannot deliver great amounts of power.

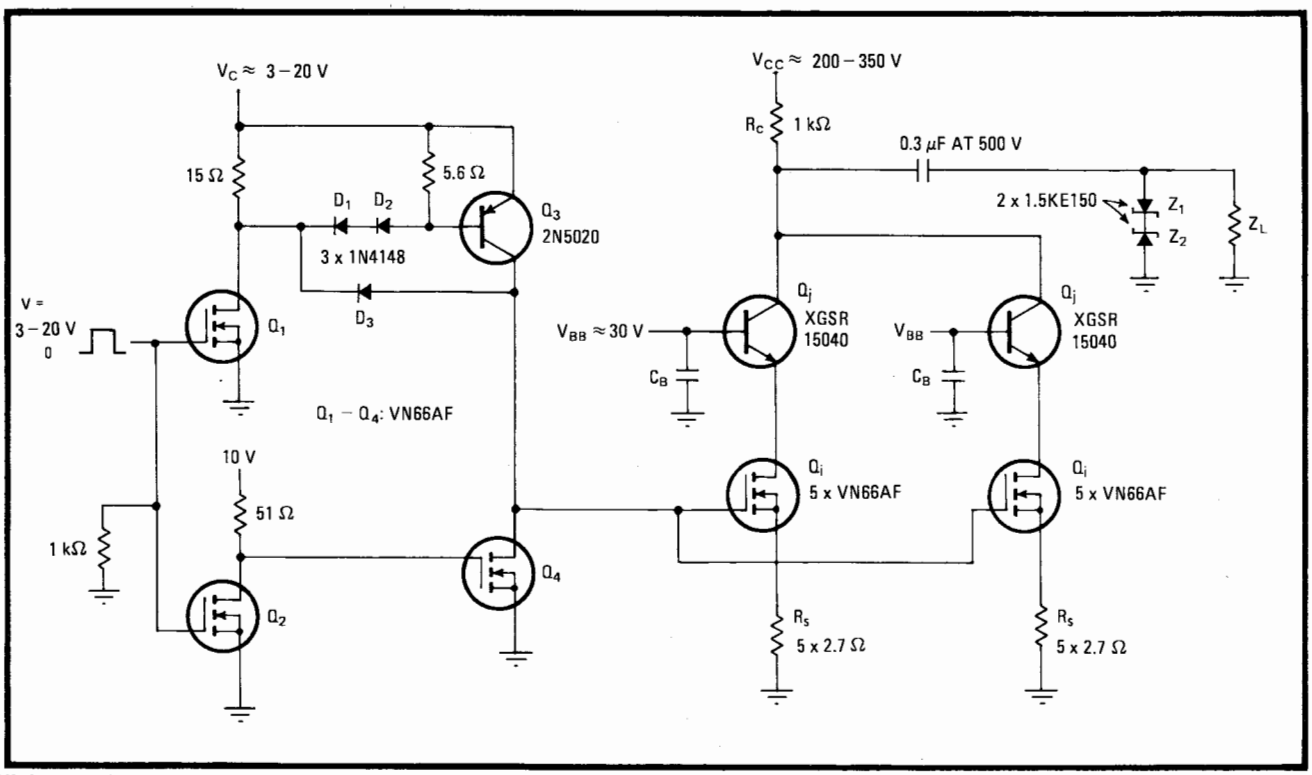
Transistors Q_1–Q_4 comprise the driver circuit for the pulser. The energizing waveform is provided by an external low-power pulse source applied at Q_1 and Q_2. Q_1 and Q_2 are directly coupled to Q_3 and Q_4. The base current to Q_3 is set at about 1.5 A, a necessary condition for achieving rise times of 10 ns across the V-MOS input capacitance of 500 picofarads.

D_1–D_3 serve as clamping diodes to prevent Q_3 from saturating on the rising edge of the pulse, and the 5.6-ohm resistor helps turn off Q_3 quickly. The amplitude of the output pulse is determined by the control voltage, which is applied to Q_3's emitter. The circuit could be further simplified if a p-channel V-MOS device were to replace Q_3, but unfortunately the p-channel units are not yet readily available.

In general, the basic output circuit is in a cascode arrangement using 10 V-MOS transistors Q_i and two bipolar transistors Q_j, with the gates of Q_i driven by the pulse. The base of Q_j is at ac ground. In this way, the current delivered to the load Z_L is approximately proportional to the voltage applied to Q_i.

The cascode circuit helps minimize the effect of the gate-to-source and gate-to-drain (input) capacitances of the V-MOS transistors, thereby enhancing the response time or speed of the circuit. Note that the output voltage of Q_i overcomes the drop across Q_j's (internal) emitter inductance (10 to 20 nH) when the stage is made active, and that Q_i is selected to withstand the inductive kick (10 to 20 V) that occurs when the stage is switched at slew rates as fast as 2 A/ns. In addition, Q_j is never driven into saturation, and as a consequence, fast response times are maintained.

The usual precautions for protecting V-MOS gates have been observed. The input-pulse amplitude is within the gate-voltage ratings. The source-to-drain voltage is not exceeded when the device is off. No attempt to bias the gate near its turn-off point to improve device linearity has been made, either, as a small misadjustment may



High-stepping quickly. Advantages of bipolar and V-MOS transistors are combined in circuit that delivers pulses to 5 kilowatts at a nominal width of 20 ns, if load is resistive. Output pulse width is limited by the 0.3-μF coupling capacitor.

cause excessive dissipation and device failures.

The bipolar transistor is a current source and so short circuits at the output of the pulser cause no trouble. Protecting the output transistors from voltage spikes is important, however, and fast transient suppressors Z_1 and Z_2 have been added to avoid transistor damage. Z_1 and Z_2 work well for low-impedance loads (10 Ω or less) but their high capacitance may otherwise serve to slow circuit speed.

The circuit has been built on a brass plate, to avoid parasitic oscillation problems in V-MOS that would be manifest if the circuit were constructed on a printed-circuit board. Very low-impedance bypass capacitors (monolithic ceramic) are connected between the base of the bipolar transistors and ground. Note that the gates of each V-MOS device are connected directly in parallel without a resistor or ferrite bead. This arrangement is equally effective in improving the suppression of parasitic oscillations. □

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