Deglitcher–delay circuit serves also as pulse generator

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Sustaining its input pulse for a number of clock cycles before translating it into an output pulse, this circuit provides an effective means of discriminating between valid data and spurious pulses or glitches. The designer who uses the circuit has numerous options for adjusting the delay between the input and output transitions, as well as controlling the duration of the output pulse. Furthermore, it triggers on either a rising or a falling edge and generates complementary outputs.

Data entering serial shift register A_1 is sampled at the clock rate and shifted along from output Q_A to Q_H. Meanwhile, for the complement of the input at the output of A_2, the same process occurs at the shift register A_3. Since all 1s are required at gates A_4 or A_5 to toggle cross-coupled NAND gates A_6 and A_7, there is a delay in the leading edge of the output, as well as in the pulse duration. The delay and the pulse duration depend on how many and which taps are connected from the shift registers to the eight-input NAND gates.

It is apparent that noise—in fact, any changes in input level—will be subject to successive samples, whose number is equal to the tap count, before it results in a change in output. By employing different numbers of taps on registers A_1 and A_3, the criterion will be different for different polarity edges—A_1 controls the positive edges and A_3 controls the negative ones—and therefore the circuit is highly noise-resistant. Further, by starting with a tap other than Q_A, initial edge delays can be built in, again selectively for either positive or negative edges.

A version of the circuit allows it to modify the input pulse width. Feeding selected output taps of A_1 into A_5 (eliminating inverter A_2 and serial register A_3) controls the time at which the trailing edge of the output pulse occurs. By judiciously choosing which taps go to A_4 and which go to A_5, the designer can exercise control over the width of the output pulse.

The circuits' applications are enhanced by expanding on the basic concepts. Thus, smaller NAND gates may be used with fewer samples, and expanded gates may be used with more shift registers in tandem. Finally, additional timing signals may be generated by connecting additional sets of gates to the shift registers. □

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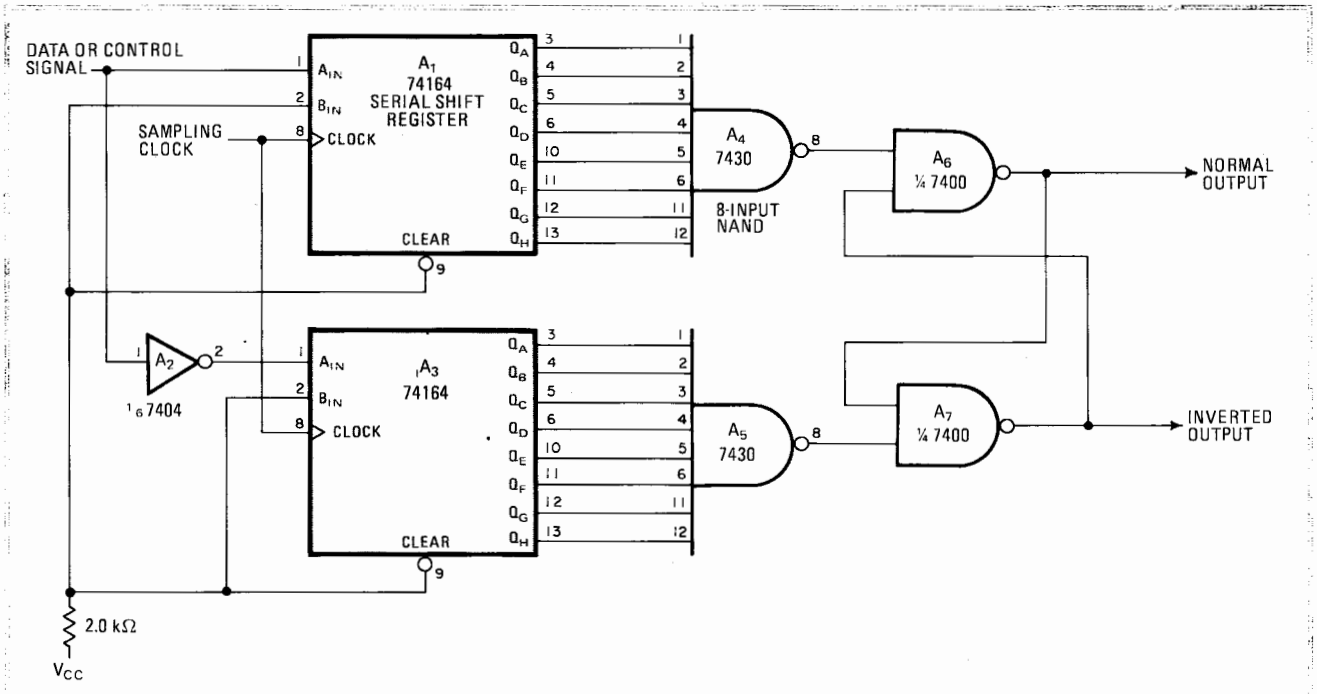

Tap dance. By changing the quantity and position of the shift register outputs into which the multiple-input NAND gates tap, a designer can mask unwanted spikes, as well as exercise a wide range of control over the output pulse width and rising and falling pulse edges.