Digital logic multiplies pulse widths

by N. Bhaskara Rao U.V.C.E., Department of Electrical Engineering, Bangalore, India

Using logic elements to multiply the width of incoming pulses by a value selected by the user, this circuit is simple to build and provides a higher accuracy-to-cost ratio than its analog counterpart. It should therefore find numerous uses in synchronous systems, and although its prime function is to provide a multiplication factor of greater than unity, it can generate smaller values as well.

The figure will help make circuit operation clear. The multiplication factor is selected by presetting two 74S192 down counters, A_1 and A_2 . Initially, counter A_1 is set to a value, M; A_2 is preset to a second value, N; A_3 is zero; and the Q output of flip-flop A_4 is high.

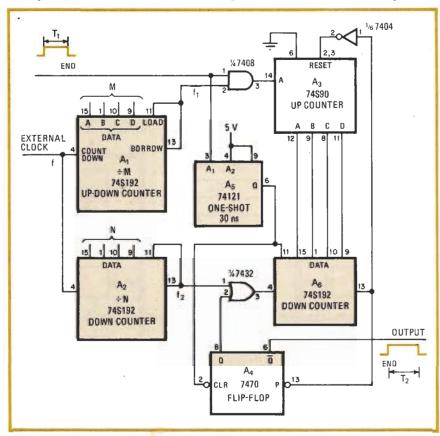
An incoming pulse of width T₁ (the signal to be multiplied) switches on the 7408 AND gate and enables

 A_3 to count to a number determined by f_1 , which is derived from an external clock having input frequency f. Thus, at the end of the pulse, the counter contains the number f_1T_1 . Note that $f_1 = f/M$.

When the trailing edge of the pulse arrives, A_5 is triggered and presets A_6 with the number contained in A_3 . Meanwhile, A_4 is cleared (Q=0) by A_5 , and the OR gate is thereby activated so that counter A_6 can initiate counting from its preset value. Note that A_6 is driven by A_2 , the divide-by-N down counter, and that $f_2 = f/N$.

The time taken for A_6 to reach zero from its preset value is thus $T_2 = (f_1/f_2)T_1 = (N/M)T_1$. At this time, the output from A_6 's borrow port clears A_3 and presets the flip-flop. Therefore the time between the flip-flop's move to logic 0 (at the trailing edge of the input pulse) and the time its Q output moves high again is T_2 .

The output signal is not derived until the input pulse's trailing edge arrives. The multiplication factor, N/M, can thus be set to any value greater or less than unity because the conversion is carried out after a delay. Needless to say, f should be much greater than T_1 for accurate pulse-width multiplication.



Width multiplier. Circuit has no analog elements. Multiplication factor is determined by ratio of N to M, set by user. A_6 is preset to f_1T_1 ; stepped to zero at f_2 rate, it signals flip-flop. Time between state changes of flip-flop is $T_2 = (N/M)T_1$.