New Phase-Locked-Loops Have Advantages as Frequency to Voltage Converters (and more)

National Semiconductor
Application Note 210
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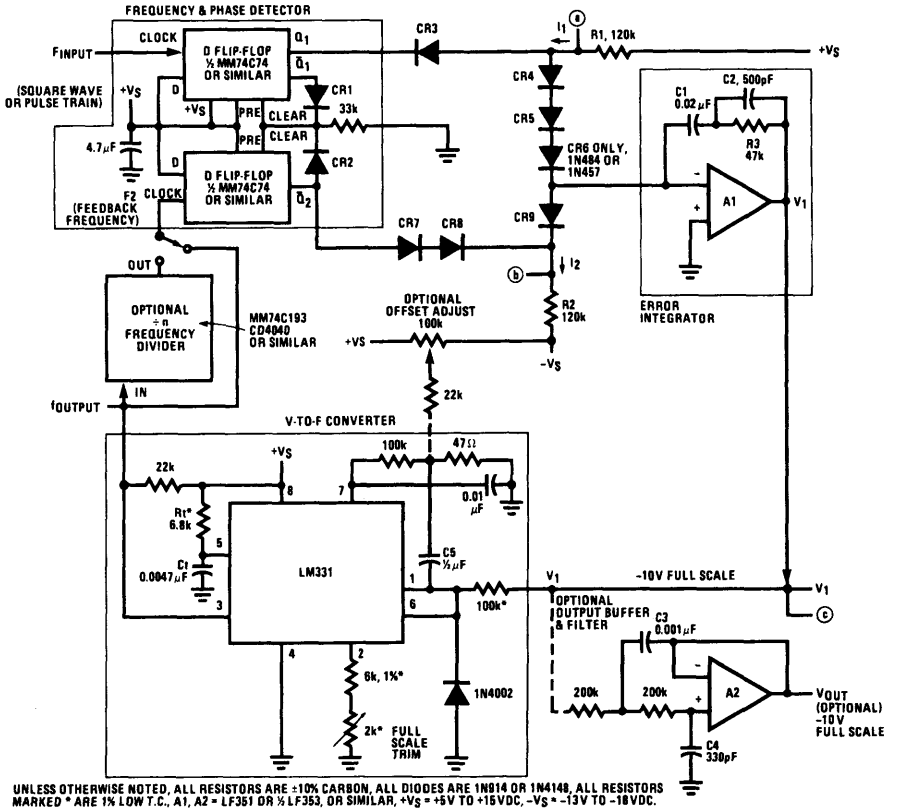
A phase-locked-loop (PLL) is a servo system, or, in other words, a feedback loop that operates with frequencies and phases. PLL's are well known to be quite useful (powerful, in fact) in communications systems, where they can pluck tiny signals out of large noises. Here, however, we will discuss a new kind of PLL which cannot work with low-level signals immersed in noise, but has a new set of advantages, instead. It does require a clean noise-free input frequency such as a square wave or pulse train.

This PLL can operate over a wide frequency range, not just 1 or 2 octaves but over 1 or 2 or 3 decades. It naturally provides a voltage output which responds quickly to frequency changes, yet does not have any inherent ripple. Thus, it can be used as a frequency-to-voltage (F-to-V) converter which does not have any of the classical limitations or compromises of (large ripple) vs (slow response), which most F-to-V converters have.[1] The linearity of this F-to-V converter will be as good as the linearity of the V-to-F converter used, and this linearity can easily be better than 0.01%. Other advantages will be apparent as we study the circuit further.

The basic circuit shown in *Figure 1* has all the functional blocks of a standard PLL. The frequency and phase detection do not consist of a quadrature detector, but of a standard dual-D flip-flop. When the frequency input is larger than F_2, Q1 will be forced high a majority of the time, and provide a positive error signal (via CR3, 4, 5, and 6) to the integrator.



UNLESS OTHERWISE NOTED, ALL RESISTORS ARE ±10% CARBON, ALL DIODES ARE 1N914 OR 1N4148, ALL RESISTORS MARKED * ARE 1% LOW T.C., A1, A2 = LF351 OR ½ LF353, OR SIMILAR, +Vs = +5V TO +15VDC, -Vs = -13V TO -18VDC.

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FIGURE 1. Basic Wide-Range Phase-Locked Loop

1. Appendix C, "V/F Converter ICs Handle Frequency-to-Voltage Needs," National Semiconductor Linear Applications book.

If F input and F_2 are the same, but the rising edges of F input lead the rising edges of F_2, the duty cycle of Q1 = HI will be proportional to the phase error. Thus, the error signal fed to the integrator will decrease to nearly zero, when the loop has achieved phase-lock, and the phase error between F_{IN} and F_2 is zero. Actually, in this condition, Q1 will put out 30 nanosecond positive pulses, at the same time that Q2 puts out 30 nanosecond negative pulses, and the net effect as seen by the integrator is zero net charge. The 30 nanosecond pulses at Q1 and Q2 enable both flip-flops to be CLEARED, and prepared for the next cycle. This phase-detector action is substantially the same as that of an MC4044 Phase-Detector, but the MM74C74 is cheaper and uses less power. It is fast enough for frequencies below 1 MHz. (At higher frequencies, a DM74S74 can be used similarly, with very low delays.)

The error integrator takes in the current from R1 or R2, as gated by the Q1 and $\overline{Q2}$ outputs of the flip-flop. For example, when F_{IN} is higher, and Q1 is HIGH, I_1 will flow through CR4, 5, and 6 and cause the integrator's output to go more negative. This is the direction to make the V-to-F converter run faster, and bring F_2 up to F input. Note that A1 does not merely integrate this current in C1 (a mistake which many amateur PLL designers make). The resistor R3 in series with C1 makes a phase *lead* in the loop response, which is essential to loop stability. The small capacitor C2 across R3 is not essential, but has been observed to offer improved settling at the voltage output.

The output of the integrator, V1, is fed to a voltage-to-frequency (V-to-F) converter. The example shown here utilizes a LM331. This converter runs on a single supply, and responds quickly with nonlinearity better than 0.05% (even though an op-amp is not used nor needed). The output of the VFC is fed back to F_2, as a feedback frequency, either directly or through an (optional) frequency divider. Any number of standard frequency dividers such as MM74C193, CD4029, or CD4018, can be used, subject to reasonable limits. A divider of 2, 3, 10, or 16 is often used. The output voltage of the integrator will be proportional to the F input, as linearly as the V-to-F can make it. Thus, the integrator's output voltage V1 can be used as the output of an ultralinear F-to-V converter. However during the brief pulses when the flip-flop is CLEARing itself, there will be small glitches found on the output of A1. The RMS value of this noise may be very small, typically 0.5 to 5mV, but the peak amplitude, sometimes 10 to 100mV, can be annoying in some systems. And, no additional filtering can be added in the main loop's path, for any further delay in the route to the VFC would cause loop instability. Instead, the output may be obtained from a separate filter and buffer which operates on a branch path. A2 provides a simple 2-pole active filter (as discussed in Reference 1) which cuts the steady-state ripple and noise down below 1mV peak-to-peak an excellent level for such a quick F-to-V (as we shall see).

What is not obvious about A2 is that its output can settle (within a specified error-band such as ±10 millivolts from the final DC value) earlier and more quickly than A1's output. The waveforms in *Figure 2* show F_{IN} stepping up instantly from 5 kHz to 10 kHz; it also shows F_2 stepping up very quickly. The error signal at Q1 is also shown. The critical waveforms are shown in *Figure 3*, the outputs of A1 and A2. While A1 puts out large spikes (caused by I1 flowing through R3), these large spikes cause the V-to-F converter to jump from 5 kHz to 10 KHz without any delay. There is, as shown in Figure 2, a significant phase error between F_{IN} and F_2, but an inspection of these frequencies shows that frequency lock has been substantially instantaneous. Not one cycle has been lost The phase lock and settling takes longer to achieve. Still, we know that if the frequency out of the VFC is 10 kHz, its input voltage must be −10 VDC. If there is noise on it, all we have to do is filter it in A2. Figure 3 shows that A2 settles very quickly — actually, in 2.0 milliseconds, which is just 20 cycles of the new frequency. A2's output has settled (i.e., the frequency has settled). while A1's output error (which is indicative of phase error being servo'ed out) continues to settle out for another 12 ms. Thus, this filter permits its output voltage to settle faster than its input, and it is responsible for the remarkable quickness of this circuit as an F-to-V converter. The waveforms of

Vertical sensitivity = 10 V/DIV (CMOS logic levels)
Horizontal sensitivity = 0.5 ms/DIV

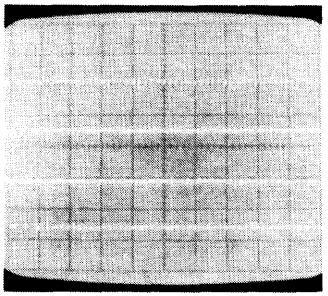

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FIGURE 2a. F output steps up from 5 kHz to 10 kHz as quickly as the input, never missing a beat.
Top Trace = input "F_{IN}" to PLL.
Bottom Trace = output "F_{OUT}" from PLL.

Vert = 10 V/DIV, Horiz = 0.5 ms/DIV

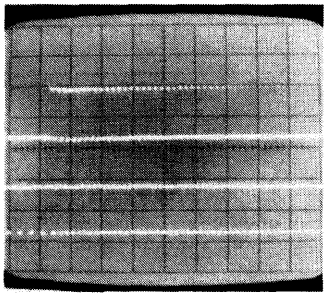

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FIGURE 2b. Error Signal. Top Trace = error signal at Q1. Bottom Trace = output "F_{OUT}" from PLL.

Figure 3 can be compared to the response (shown in *Figure 4)* of a conventional F-to-V converter. The upper trace is the output of a conventional FVC after a 4-pole filter[2], and the lower trace is the output of the circuit of *Figure 1*. The phase-locked-loop F-to-V converter is quicker yet quieter.

2. AN-207, V-to-F and F-to-V Converter Applications.

Vert = 2 V/DIV, Horiz = 2 ms/DIV

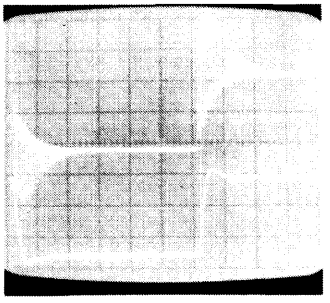

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FIGURE 3a. Settling waveforms, as F_{IN} goes from 5 kHz to 10 kHz and back again, using circuit of *Figure 1*. Top Trace = output of integrator (V1). Bottom Trace = output of filter (V_{OUT}).

Vert = 2 V/DIV, Horiz = 0.5 ms/DIV

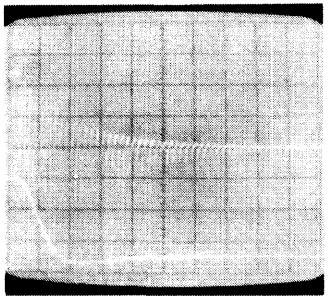

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FIGURE 3b. PLL Settling Waveforms. The same waveform as in *Figure 3a*, but time base is expanded to 0.5 ms/DIV to show fine detail of settling.

Vert = 2 V/DIV, Horiz = 20 ms/DIV

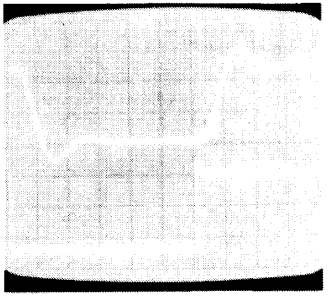

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FIGURE 4a. FVC Response vs PLL Response. The PLL can settle rather more quickly than a conventional F-to-V converter. Top Trace = conventional F-to-V converter with 4-pole active filter, responding to a 5 kHz to 10 kHz step. Bottom Trace = PLL FVC, with the same input, circuit of *Figure 1*.

Vert = 2 V/DIV, Horiz = 20 ms/DIV

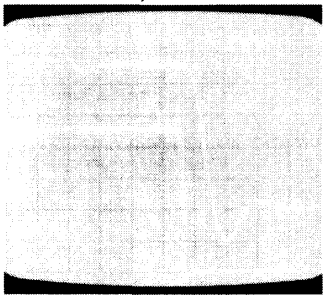

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FIGURE 4b. FVC Step Response.
FIGURE 4b. This waveform is similar to that in *Figure 4a* but the frequency change covers a 10:1 ratio, from 10 kHz to 1 kHz and back to 10 kHz. For this waveform, the adaptive current sources of *Figure 5* connect to *Figure 1* (whereas for *Figure 4a* R1 = R2 = 120k).

Vert = 2 V/DIV, Horiz = 5 ms/DIV

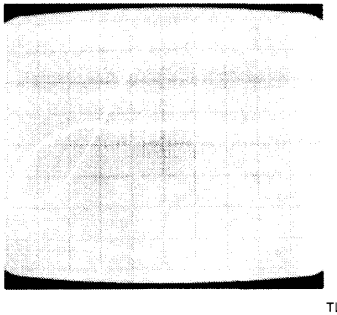

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FIGURE 4c. FVC Response. The same as *Figure 4b*, but time base expanded to 5 ms/DIV, to show detail of rise time. Top Trace = conventional FVC. Bottom Trace = PLL FVC.

Vert = 2 V/DIV, Horiz = 5 ms/DIV

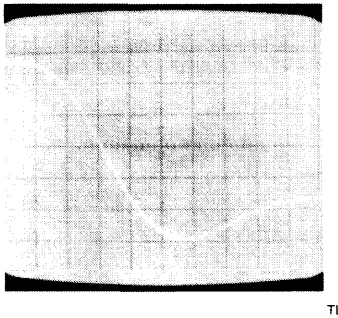

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FIGURE 4d. FVC Response The same as *Figure 4b*, but expanded to 5 ms/DIV to show details of fall time. Top Trace = conventional FVC. Bottom Trace = PLL FVC.

Vert = 0.2 V/DIV/, Horiz = 50 ms/DIV

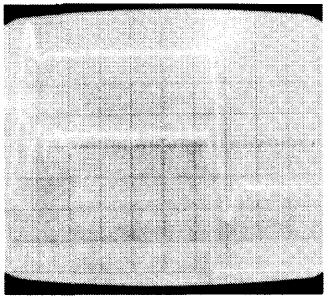

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FIGURE 4e. PLL Settling Waveforms at Low Frequencies. The same idea as in *Figure 4b*, but 10 × slower, from 1.0 kHz to 100 Hz (and back). The settling to 1 kHz is still distinctly faster for the PLL, but at 100 Hz, it is a bit slower. Still, the PLL is faster than the FVC at all speeds from 200 Hz to 10 kHz.

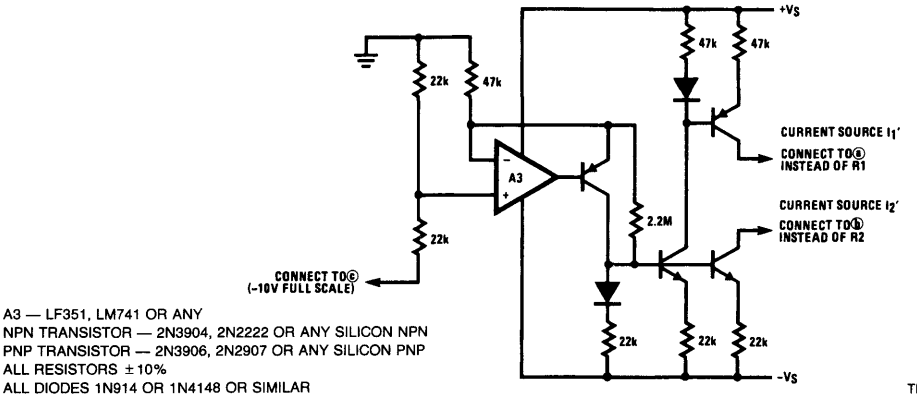
So far we have shown a PLL which operates nicely over a frequency range of about 3:1. If the frequency is decreased below 3 kHz, the loop gain becomes excessive, and the currents I1 and I2 are large enough to cause loop instability. The loop gain increases at lower frequencies, because a given initial phase error will cause the fixed current from R1 or R2 to be integrated for a *longer* time, causing a *larger* output change at the integrator's output, and a *larger* change of frequency. When the frequency is thus corrected, and the period of one cycle is changed, at a low frequency it may be *over-corrected,* and the phase error on the next cycle may be as large as (or larger than) the initial phase error, but with reversed sign.[3] To avoid this and to maintain loop stability at lower frequencies, e.g. 0.5 to 1 kHz, R1 and R2 can be simply raised to 1.5 MΩ. However, response to a step will be proportionally slower. To achieve a wide frequency range (20:1), and optimum quickness at all frequencies, it is necessary to servo I1 and I2 to be *proportional to the frequency.* Fortunately, as V1 is normally proportional to F, it is easy to generate current sources I1' and I2' which are proportional to F. The circuit of *Figure 5* can be connected to the basic PLL, instead of R1 and R2, and provides good, quick loop stability over a 30:1 frequency range, from 330 Hz to 10 kHz. For best results over a 30:1 frequency range, change R3, the damping resistor in Figure 1, from 47k to 100k. However, if the frequency range is smaller (such as 2:1 or 3:1), constant resistors for R1 and R2 or very simple current sources may give adequate response in many systems. (To cover wider frequency ranges than 30.1 with optimum response, the circuits in the precision phase-locked-loop, below, are much more suitable.)

Often a frequency multiplier is needed, to provide an output frequency 2 or 3 or 10 or n times higher than the input. By inserting a ÷n frequency divider in the feedback loop, this is easily accomplished. [Of course, a ÷m frequency divider can be inserted ahead of the frequency input, to provide correct scaling, and the output frequency then will be $F_{IN}(n/m)$.]

To obtain good loop stability in a frequency multiplier with n = 2, remember that a 20 kHz V-to-F converter followed by a ÷2 circuit has exactly the same loop response and stability needs as a 10 kHz V-to-F converter, because it *is* a 10 kHz V-to-F converter, even though it provides a useful 20 kHz output. Thus, the frequency of the F_2 (minimum and maximum) will determine what loop gains and loop damping components are needed.

To accommodate a 1 kHz V-to-F loop, simply make C1 and C2 10 times bigger than the values of *Figure 1*; treat C3, C4, C5 and Ct similarly is used. To accommodate a 100 Hz V-to-F, increase them by another factor of 10.

If the PLL is to be used primarily as a frequency multiplier, it may be necessary to use stable, low-temperature-coefficient components, because the accuracy of V_{OUT} will not be important. The parts cost can be cut considerably. (Make sure that the VFC does not run out of range to handle all frequencies of interest.) On the other hand, the damping components will be chosen quite a bit differently if slow, stable jitter-free response is needed or if quick response is required. The circuits shown are just a starting place, to start optimizing your own circuit.



A3 — LF351, LM741 OR ANY
NPN TRANSISTOR — 2N3904, 2N2222 OR ANY SILICON NPN
PNP TRANSISTOR — 2N3906, 2N2907 OR ANY SILICON PNP
ALL RESISTORS ±10%
ALL DIODES 1N914 OR 1N4148 OR SIMILAR

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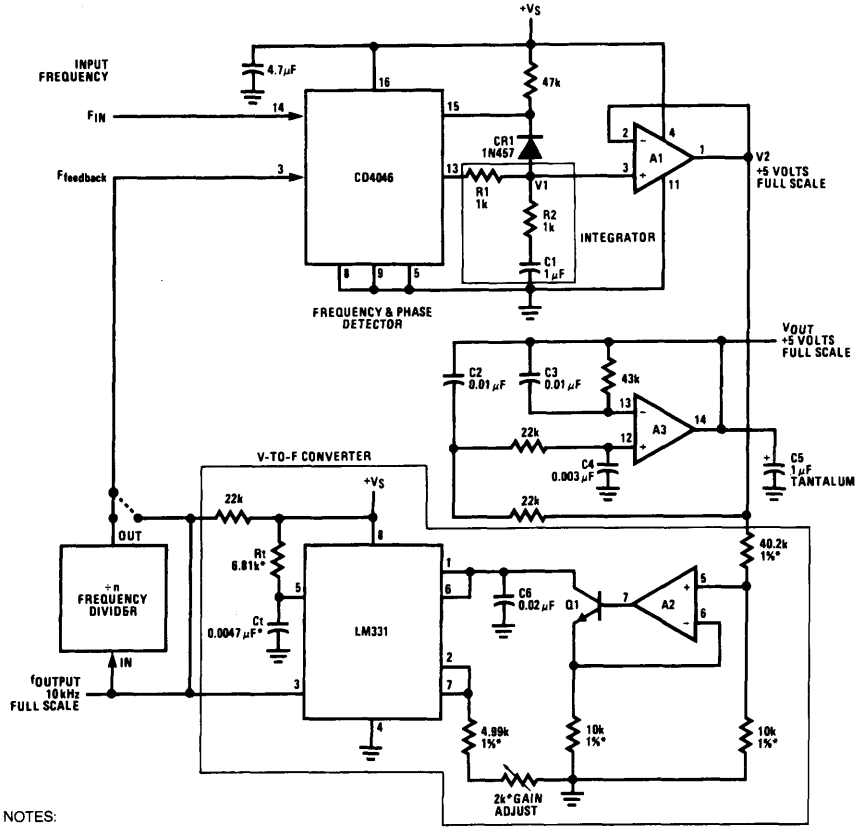
FIGURE 5. Proportional Current Source for Basic PLL

3. Optimize phase-lock loops to meet your needs or determine why you can't. Andrzej B. Przedpelski, *Electronic Design,* September 13, 1978.

A Single-Supply PLL

The single-supply PLL is shown in *Figure 6* as an example of a simple circuit which is effective when battery operation or single-supply operation is necessary. This circuit will function accurately over a 10:1 frequency range from 1 kHz to 10 kHz, but will not respond as quickly as the basic PLL of *Figure 1*. The reason is the use of the CD4046 frequency detector. When an F_{IN} edge occurs ahead of a F feedback pulse, pin 13 of the CD4046 pulls up on C1 via R1 = 1 kΩ. This current cannot be controlled or manipulated over as wide a range as "I1" in *Figure 1*. As a consequence, the response of this PLL is never as smooth nor fast-settling as the basic PLL, but it is still better behaved than most F-to-V converters. As with the basic PLL, the detector feeds a current to be integrated in C1 (and R2 provides the necessary "lead"). A1 acts simply as a buffer for the R1, C1 integrator. A3, optional, can provide a nicely filtered output. And A2 servos Q1, drawing a current out of C6 which is proportional to V2. Here the LM331 acts as a current-to-frequency converter, and F output is precisely proportional to the collector current of Q1. As with the basic circuit, this PLL can be used as a quick and/or quiet F-to-V converter, or as a frequency multiplier. One of the most important uses of an F-to-V is to demodulate the frequency of a V-to-F converter, which may be situated at a high common-mode voltage, isolated by photoisolators, or to recover a telemetered signal. An F-to-V converter of this sort can provide good bandwidth for demodulating such a signal.



NOTES:

— Q1 = 2N3565 OR 2N3904 HIGH BETA NPN

— A1, A2, A3 = ¼ LM324

— ON CD4046, PINS 1, 2, 4, 6, 7, 10, 11, 12 ARE NO CONNECTION

— USE STABLE, LOW-T.C. PARTS FOR COMPONENTS MARKED*

—+V_S = +7 TO +15 VDC

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FIGURE 6. Single Supply Phase Locked Loop

The precision PLL in *Figure 7* acts very much the same as the basic PLL, with refinements in various places.

- The flip-flops in the detector have a gate G1 to CLEAR them, for quicker response.
- The currents which A1 integrates are steered through Q1, Q2 and Q3, Q4 because transistors are quicker then diodes, yet have much lower leakage.
- The V-to-F converter uses A2 as an op-amp integrator, to get better than 0.01% nonlinearity (max).
- G2 is recommended as an inverter, to invert the signal on the LM331's pin 3, avoid a delay, and improve loop stability. (However, we never found any *real* improvement in loop stability, despite theories that insist it must be there. Comments are invited.)

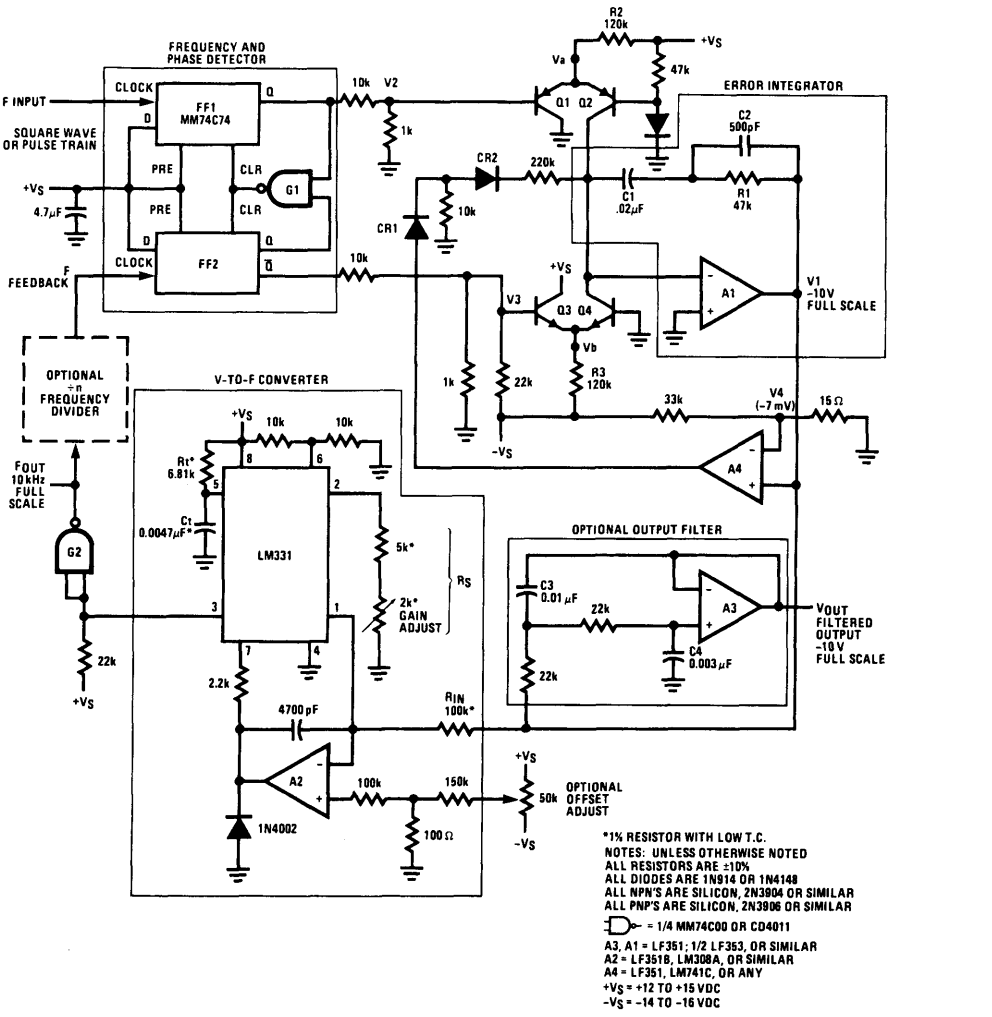

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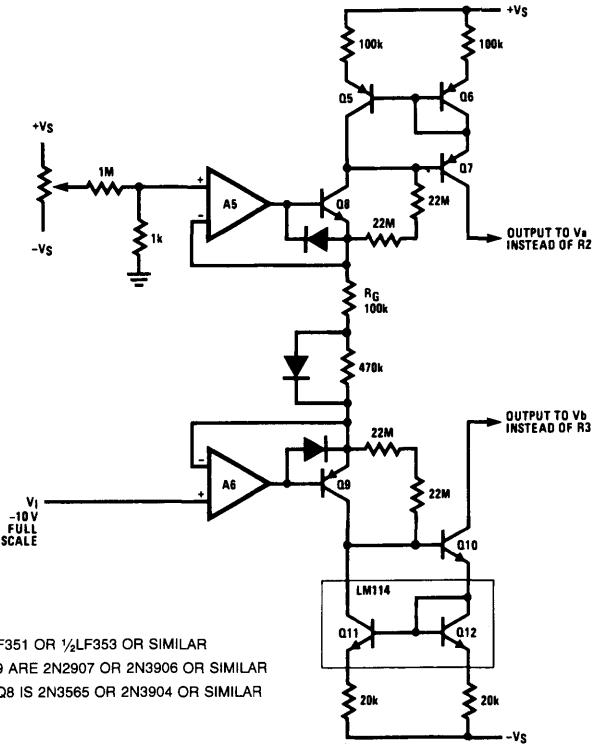
FIGURE 7. Precision PLL

- A4 is included as an (optional) limiter, to prevent V1 from ever going positive. This will facilitate quick startup and recovery from overdrive conditions.

Also, in *Figure 8*, the wide-range current pump for the precision PLL is a "semiprecision" circuit, and provides an output current proportional to −V1, give or take 10 or 15%, over a 3-decade range. The 22 MΩ resistors prevent the current from shutting off in case −V becomes positive (probably unnecessary if A4 is used). For best results over a full 3-decade range (11 kHz to 9 Hz), do use A4, delete the four 22 MΩ resistors, and insert the (diode parallel to the 470 kΩ) in series with the R_G as shown. This will give good stability at all frequencies (although stability cannot be extended below 1/1500 of full scale without extra efforts).

This PLL has been widely used in testing of VFCs, as it can force the LM331 to run at a crystal-controlled frequency (established as the F input), and the output voltage at V_{OUT} is promptly measured by a 6-digit (1 ppm nonlinearity, max) digital voltmeter, with much greater speed and precision than can be obtained by forcing a voltage and trying to read a frequency. While at 10 kHz, the advantages are clearcut; at 50 Hz it is even more obvious. Measuring a 50 Hz signal with ±0.01 Hz resolution cannot be done (even with the most powerful computing counter-timer) as accurately, quickly, and conveniently as the PLL's voltage output settles.



A5, A6, ARE LF351 OR ½LF353 OR SIMILAR
Q5, Q6, Q7, Q9 ARE 2N2907 OR 2N3906 OR SIMILAR
Q8, Q10 ARE Q8 IS 2N3565 OR 2N3904 OR SIMILAR

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FIGURE 8. Wide Range Current Pumps for Precision PLL of *Figure 7*

One final application of this PLL is as a wide-range sine generator. The VFC in *Figure 9* puts out an adequate sine-shaped output, but does not have good V-to-F linearity, and its frequency stability is not much better than 0.2%. An LM331 makes an excellent linear stable V-to-F converter, with a pulse output; but it can not make sines. But it can command, via a PLL, to force the sine VFC to run at the correct frequency. Simply connect the sine VFC of *Figure 9* into one of the PLLs, instead of the LM331 VFC circuit. Then use a precise linear low-drift VFC based on the LM331 to establish the F_{IN} to the PLL. If the voltage needed by the sine VFC to put out a given frequency drifts a little, that is okay, as the integrator will servo and make up the error. The use of a controlled sine-wave generator in a test system was the first of many applications for a wide-range phase-locked-loop.

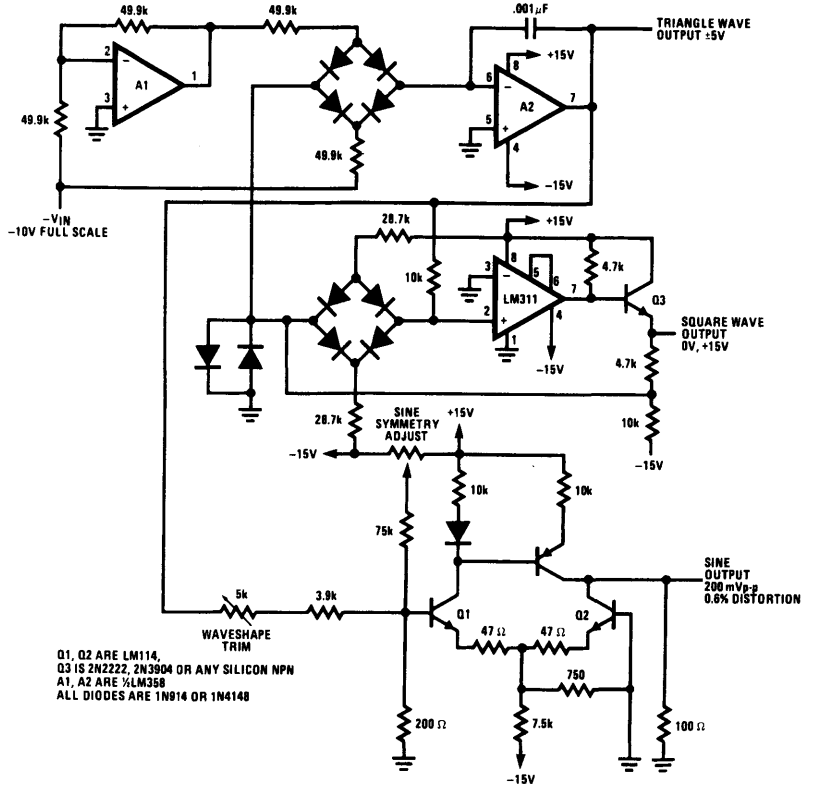

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FIGURE 9. Sine-Wave VFC to Use with PLL