The RCA COS/MOS Phase-Locked-Loop A Versatile Building Block for Micro-Power Digital and Analog Applications

INTRODUCTION

Phase-locked-loops (PLL's), especially in monolithic form, are finding significantly increased usage in signal-processing and digital systems. FM demodulation, FSK demodulation, tone decoding, frequency multiplication, signal conditioning, clock synchronization, and frequency synthesis are some of the many applications of a PLL. The PLL described in this Note is the COS/MOS CD4046A, which consumes only 600 microwatts of power at 10 kHz, a reduction in power consumption of 160 times when compared to the 100 milliwatts required by similar monolithic bipolar PLL's. This power reduction has particular significance for portable battery-operated equipment. This Note discusses the basic fundamentals of phase-locked-loops, and presents a detailed technical description of the COS/MOS PLL as well as some of its applications.

REVIEW OF PLL FUNDAMENTALS

The basic phase-locked-loop system is shown in Fig. 1; it consists of three parts: phase comparator, low-pass filter, and voltage-controlled oscillator (VCO); all are connected to form a closed-loop frequency-feedback system.

With no signal input applied to the PLL system, the error voltage at the output of the phase comparator is zero. The voltage, Vd(t), from the low-pass filter is also zero, which causes the VCO to operate at a set frequency, fo, called the center frequency. When an input signal is applied to the PLL, the phase comparator compares the phase and frequency of the signal input with the VCO frequency and generates an error voltage proportional to the phase and frequency

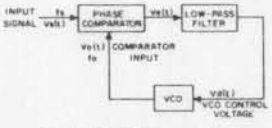


Fig. 1– Block diagram of PLL.

difference of the input signal and the VCO. The error voltage, Ve(t), is filtered and applied to the control input of the VCO; Vd(t) varies in a direction that reduces the frequency difference between the VCO and signal-input frequency. When the input frequency is sufficiently close to the VCO frequency, the closed-loop nature of the PLL forces the VCO to *lock* in frequency with the signal input; i.e., when the PLL is in lock, the VCO frequency is identical to the signal input except for a finite phase difference. The range of frequencies over which the PLL can maintain this locked condition is defined as the *lock range* of the system. The lock range is always larger than the band of frequencies over which the PLL can acquire a locked condition with the signal input. This latter band of frequencies is defined as the *capture range* of the PLL system.

TECHNICAL DESCRIPTION OF COS/MOS PLL

Fig. 2 shows a block diagram of the COS/MOS CD4046A, which has been implemented on a single monolithic integrated circuit. The PLL structure consists of a low-power, linear, voltage-controlled oscillator (VCO), and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-volt zener is provided for supply regulation if necessary. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The low-pass filter is implemented through external parts because of the radical configuration changes from application to application and because some of the components are non-integrable. The CD4046A is supplied in a 16-lead, dual-in-line, ceramic package (CD4046AD); a 16-lead, dual-in-line, plastic package (CD4046AE); or a 16-lead flat-pack (CD4046AK). It is also available in chip form (CD4046AH).

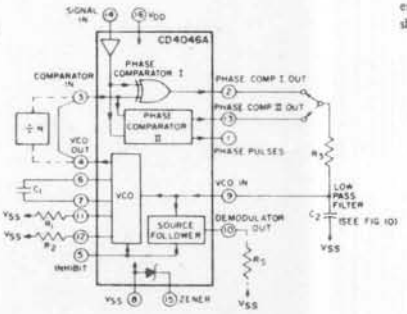


Fig. 2– COS/MOS PLL block diagram.

Phase Comparators

Most PLL systems utilize a balanced mixer composed of well-controlled analog amplifiers for the phase-comparator section. Analog amplifiers with well-controlled gain characteristics cannot easily be realized using COS/MOS technology. Hence, the COS/MOS design shown in Fig. 3 employs digital-type phase comparators. Both phase comparators are driven by a common-input amplifier configuration composed of a bias stage and four inverting-amplifier stages. The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic 0 ≤ 30% (VDD-VSS), logic 1 ≥ 70% (VDD-VSS)]. For smaller input signal swings, the signal must be capacitively coupled to the self-biasing amplifier at the signal input to insure an over-driven digital signal into the phase comparators.

Phase-comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal and comparator input frequencies must have 50-percent duty cycle. With no signal or noise on the signal input, this phase comparator has

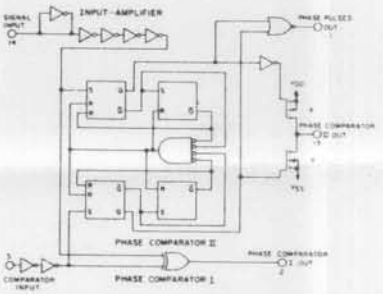


Fig. 3– Schematic of COS/MOS PLL phase-comparator section.

an average output voltage equal to VDD/2. The low-pass filter connected to the output of phase-comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o). With phase-comparator I, the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 4 shows the typical, triangular, phase-to-output, response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase-comparator I in locked condition of f_o is shown in Fig. 5.

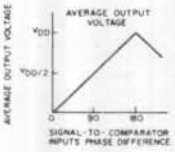


Fig. 4– Phase-comparator I characteristics at low-pass filter output.

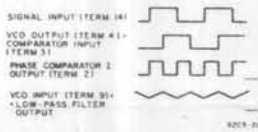


Fig. 5– Typical waveforms for COS/MOS phase-locked loop employing phase-comparator I in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p and n drivers having a common output node as shown in Fig. 3. When the p-MOS or n-MOS drivers are ON, they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal- and comparator-input signals. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-MOS output driver is maintained ON continuously. If the signal-input frequency is lower than the comparator-input frequency, the n-MOS output driver is maintained ON continuously. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-MOS output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the signal input leads the comparator input in phase, the p-MOS output driver is maintained ON for time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this type of phase comparator is adjusted until the signal and comparator input are equal in both phase and frequency. At this stable operating point, both p- and n-MOS output drivers remain OFF, and thus the phase-comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover, the signal at the "phase pulses" output is at a high level, and can be used for indicating a locked condition. Thus, for phase-comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-MOS output drivers are OFF for most of the signal-input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase-comparator II. Fig. 6 shows typical waveforms for a COS/MOS PLL employing phase-comparator II in a locked condition.

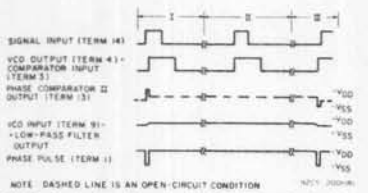


Fig. 6 – Typical waveforms for COS/MOS phase-locked loop employing phase-comparator II in locked condition.

Fig. 7 shows the state diagram for phase-comparator II; each circle represents a state of the comparator. The number at the top inside each circle represents the state of the comparator, while the logic state of the signal and comparator inputs, represented by a 0 or a 1, are given by the left and right numbers, respectively, at the bottom of each circle. The transitions from one state to another result from either a logic change on the signal input (I) or the comparator input (C). A positive transition and a negative transition are shown by an arrow pointing up or down, respectively. The state diagram assumes that only one transition on either the signal input or the comparator input occurs at any instant. States 3, 5, 9, and 11 represent the condition at the output of phase-comparator II when the p-MOS driver is ON, while states 2, 4, 10, and 12 determine the condition when the n-MOS driver is ON. States 1, 6, 7, and 8 represent the condition when the output of phase-comparator II is in its high impedance state; i.e., both p- and n-devices are OFF, and the phase-pulses output (terminal 1) is high. The condition at the phase-pulses output for all other states is low.

As an example of how one may use the state diagram shown in Fig. 7, consider the operation of phase-comparator II in the locked condition shown in Fig. 6. The waveforms shown in Fig. 6 are broken up into three sections: section I corresponds to the condition in which the signal input leads the comparator input in phase, while section II corresponds to a finite phase difference. Section III depicts the condition when the comparator input leads the signal input in phase. These three sections all correspond to a locked condition for the COS/MOS PLL; i.e., both signal- and comparator-input signals are of the same frequency but differ slightly in phase. Assume that both the signal inputs begin in the 0 state, and that phase-comparator II is initially in its high-impedance output condition (state 1), as shown in Figs. 7 and 6, respectively. The signal input makes a positive transition

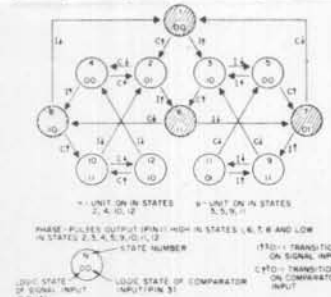


Fig. 7– State diagram of phase-comparator II.

first, which brings phase-comparator II to state 3. State 3 corresponds to the condition of the comparator in which the signal input is a 1, the comparator input is a 0, and the output p-device is ON. The comparator input goes high next, while the signal input is high, thus bringing the comparator to state 6, a high-impedance output condition. The signal input goes to zero next, while the comparator input is high, which corresponds to state 7. The comparator input goes low next, bringing phase-comparator II back to state 1. As shown for section I, the p-device stays on for a time corresponding to the phase difference between the signal input and the comparator input. Starting in state 1 at the beginning of section III, the comparator input goes high first, while the signal input is low, bringing the comparator to state 2. Following the example given for section I, the comparator proceeds from state 2 to states 6 and 8 and then back to 1. The output of phase-comparator II for section III corresponds to the n-device being on for a time corresponding to the phase difference between the signal and comparator inputs.

The state diagram of phase-comparator II completely describes all modes of operation of the comparator for any input condition in a phase-locked-loop.

Voltage-Controlled Oscillator

Fig. 8 shows the schematic diagram of the voltage-controlled oscillator (VCO). To assure low system-power dissipation, it is desirable that the low-pass filter consume little power. For example, in an RC filter, this requirement dictates that a high-value R and a low-value C be utilized. The VCO input must not, however, load down or modify the characteristics of the low-pass filter. Since the VCO design shown utilizes an n-MOS input configuration having practically infinite input resistance, a great degree of freedom is allowed in selection of the low-pass filter components.

The VCO circuit shown in Fig. 8 operates as follows: when the inhibit input is low, P_3 is turned full ON, effectively connecting the sources of P_1 and P_2 to V_{DD}; and gates 1 and 2 are permitted to function as NOR-gate flip-flops. N1 together with external-resistor R1 form a source-follower configuration. As long as the resistance of R1 is at least an order of magnitude greater than ON resistance of N_1 (greater than 10 kilohms), the current through R1 is linearly dependent on the VCO input voltage. This current flows through P_1, which, together with P2, forms a current-mirror network. External resistor R2 adds an additional constant current through P1; this current offsets the VCO operating frequency for VCO input signals of 0 volts. In the current-mirror network, the current of P2 is effectively equal to the current through P1 independent of the drain voltage at P2. (This condition is true provided P2 is maintained in saturation; in the circuit shown, P2 is saturated under all possible operating conditions and modes). The set/reset flip-flop composed of gates 1 and 2 turns ON either P4 and N3, or P5 and N2. One side of the external capacitor C1 is, therefore, held at ground, while the other side is charged by the constant current supplied by P2. As soon as C1 charges to the point at which the transfer point of inverters 1 or 5 is reached, the flip-flop changes state. The

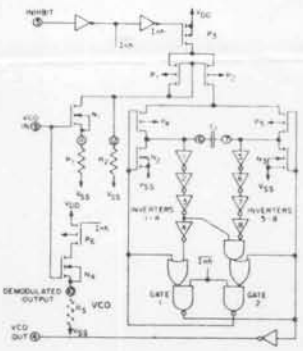


Fig. 8– Schematic of COS/MOS VCO section.

charged side of the capacitor is now pulled to ground. The other side of the capacitor goes negative, and discharges rapidly through the drain diode of the OFF n-device. Subsequently, a new half-cycle starts. Since inverters 1 and 5 have the same transfer points, the VCO has a 50-percent duty-cycle. Inverters 1 through 4 and 5 through 8 serve several purposes: (1) they shape the slow-input ramp from capacitor C1 to a fast waveform at the flip-flop input stage, (2) they maintain low power dissipation through the use of high-impedance devices at inverters 1 and 5 (slow-input wave-forms), and (3) they provide four inverter delays before removal of the set/reset flip-flop triggering pulse to assure proper toggling action.

In order not to load the low-pass filter, a source-follower ouput of the VCO input voltage is provided (demodulated output). If this output is used, a load resistor (Rs) of 10 kilohms or more should be connected from this terminal to ground. If unused, this terminal should be left open. A logic 0 on the inhibit input enables the VCO and the source follower, while a logic 1 turns off both to minimize stand-by power consumption.

Performance Summary of COS/MOS PLL

The maximum ratings for the CD4046A COS/MOS PLL, as well as its general operating-performance characteristics are outlined in Table I. The VCO and comparator characteristics are shown in Tables II and III, respectively. Table IV summarizes some useful formulas as a guide for approximating the values of external components for the CD4046A in a phase-locked-loop system. When using Table IV, one should keep in mind that frequency values are in kilohertz, resistance values are in kilohms, and capacitance values are in microfarads. The selected external components must be within the following ranges:

$$10\ K\Omega \leq R_1, R_2, R_S \leq 1\ M\Omega$$
$$C_1 \geq 100\ pF \text{ at } V_{DD} \geq 5\ V$$
$$C_1 \geq 50\ pF \text{ at } V_{DD} \geq 10\ V$$

In addition to the given design information, refer to Fig. 9 for R_1, R_2, and C_1 component selections. The use of Table IV in designing a COS/MOS PLL system for some familiar applications is discussed below.

APPLICATIONS OF THE COS/MOS PLL

The COS/MOS phase-locked-loop is a versatile building block suitable for a wide variety of applications, such as FM demodulators, frequency synthesizers, split-phase data synchronization and decoding, and phase-locked-loop lock detection.

FM Demodulation

When a phase-locked-loop is locked on an FM signal, the voltage-controlled oscillator (VCO) tracks the instantaneous frequency of that signal. The VCO input voltage, which is the filtered error voltage from the phase detector, corresponds to the demodulated output. Fig. 11 shows the connections for the COS/MOS CD4046A PLL as an FM demodulator. For this example, an FM signal consisting of a 10-kilohertz carrier frequency was modulated by a 400-Hz audio signal. The total FM signal amplitude is 500 millivolts, therefore the signal must be ac coupled to the signal input (terminal 14).

Table I– Maximum ratings and general operating characteristics

MAXIMUM RATINGS, *Absolute-Maximum Values*

Storage Temperature Range	65°C to +150	°C
Operating Temperature Range		
Ceramic Package Types	55°C to +125	°C
Plastic Package Types	40°C to +85	°C
DC Supply Voltage Range (V_{DD} – V_{SS})	−0.5 V to +15	V
Device Dissipation (Per Pkg.)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply Voltage (V_{DD} – V_{SS})	5 to 15	V
Recommended Input Voltage Swing	V_{DD} to V_{SS}	

General Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Operating Supply Voltage ($V_{DD} - V_{SS}$)			5 to 15 V
Operating Supply Current			
Inhibit = "0" @ C_1 = 0.0001 μF R_1 = 1 MΩ	f_0 = 10 kHz	V_{DD} = 5 V	70 μW
	f_0 = 10 kHz	V_{DD} = 10 V	600 μW
Inhibit = "1"			25 μA

Table II– VCO electrical characteristics

VCO Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Maximum Frequency	1.2 MHz
Temperature Stability	600 ppm/°C
Linearity ($V_{VCO\ in}$ = 5 V ± 2.5 V)	1%
Center Frequency	Programmable with R_1 and C_1
Frequency Range	Programmable with R_1, R_2, and C_1
Input Resistance	$10^{12}\ \Omega$
Output Voltage	10 V_{p-p}
Duty Cycle	50%
Rise & Fall Times	50 ns
Output Current Capability	
"1" Drive @ V_O = 9.5 V	−1.8 mA
"0" Sink @ V_O = 0.5 V	2.6 mA
Demodulated Output	
Offset Voltage	
$\lvert V_{VCO\ in} - V_{DEMOD\ out}\rvert$ @ 1 mA	1.5 V

Table III – Comparator electrical characteristics

Comparator Characteristics (Typical Values at $V_{DD} - V_{SS}$ = 10 V and T_A = 25°C)

Signal Input	
Input Impedance	400 KΩ
Input Sensitivity	
ac coupled	400 mV
dc coupled	"0" ≤ 30% ($V_{DD} - V_{SS}$) "1" ≥ 70% ($V_{DD} - V_{SS}$)
Comparator Input Levels (term. 3)	"0" ≤ 30% ($V_{DD} - V_{SS}$) "1" ≥ 70% ($V_{DD} - V_{SS}$)
Output Current Capability	
Comparator I (term. 2) and Comparator II (term. 13):	
"1" Drive @ V_O = 9.5 V	−1.8 mA
"0" Sink @ V_O = 0.5 V	2.6 mA
Comparator II Phase Pulses (term. 1)	
"1" Drive @ V_O = 9.5 V	−0.5 mA
"0" Sink @ V_O = 0.5 V	1.4 mA

Phase-comparator I is used for this application because a PLL system with a center frequency equal to the FM carrier frequency is needed. Phase comparator I lends itself to this application also because of its high signal-input-noise-rejection characteristics.

The formulas shown in Table IV for phase-comparator I with $R_2 = \infty$ are used in the following considerations. The center frequency of the VCO is designed to be equal to the carrier frequency, 10 kHz. The value of capacitor C_1, 500 pF, was found by assuming an R_1 = 100 KΩ for a supply voltage V_{DD} = 5 volts.

These values determined the center frequency:

$$f_o = 10\ \text{kHz}$$

The PLL was set for a capture-range of

$$f_c \approx \pm \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{R_3 C_2}} \approx \pm 0.4\ \text{kHz}$$

to allow for the deviation of the carrier frequency due to the audio signal. The components shown in Fig. 10 for the low-pass filter (R_3 = 100 kΩ, C_2 = 0.1 μF) determine the above capture frequency.

The total current drain at a supply voltage of 5 volts for this FM-demodulator application is 132 microamperes for a 4 dB S/N-ratio on the signal input, and 90 microamperes for a 10dB S/N ratio. The power consumption decreases because the signal-input amplifier goes into saturation at higher input levels.

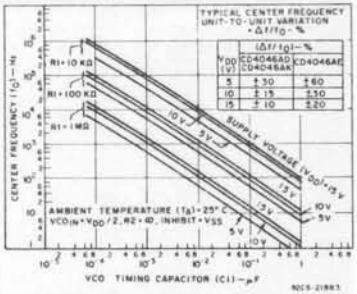


Fig. 9(a)– Typical center frequency vs. C_1 for R_1 = 10 KΩ, 100 KΩ, and 1 MΩ.

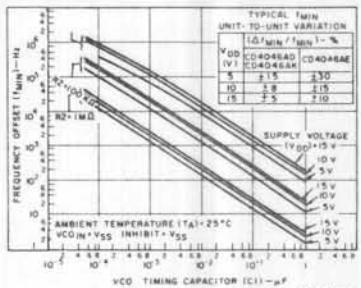


Fig. 9(b)– Typical frequency offset vs. C_1 for R_2 = 10 KΩ, 100 KΩ, and 1 MΩ.

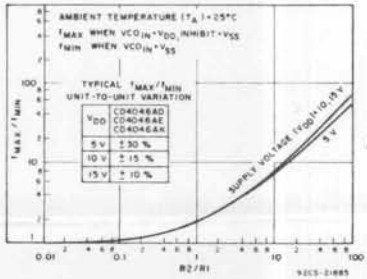
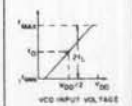
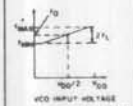
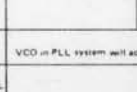
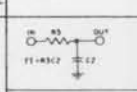


Fig. 9(c)– Typical f_{max}/f_{min} vs. R_2/R_1.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET, $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET, $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L$ = full VCO frequency range		$2f_L = f_{max} - f_{min}$	
Frequency Capture Range, $2f_C$			$f_C = f_L$	
Loop Filter Component Selection	 For $2f_C$, see Ref. (2)			
Phase Angle between Signal and Comparator	90° at center frequency (f_o), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	– Given f_o – Use f_o with Fig.9a to determine R1 and C1	– Given f_o and f_L – Calculate f_{min} from the equation $f_{min} = f_o - f_L$ – Use f_{min} with Fig.9b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.9c to determine ratio R2/R1 to obtain R1	– Given f_{max} – Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ – Use f_o with Fig.9a to determine R1 and C1	– Given f_{min} & f_{max} – Use f_{min} with Fig.9b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.9c to determine ratio R2/R1 to obtain R1

For further information, see
(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966.
(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

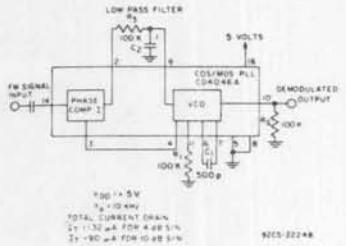


Fig. 10– FM demodulator.

Fig. 11 shows the performance of the FM/demodulator circuit of Fig. 10 at a 4 dB S/N-ratio. The demodulated output is taken off the VCO-input source follower using a resistor Rs (R_S = 100 kΩ).The demodulation gain for this circuit is 250 mV/kHz.

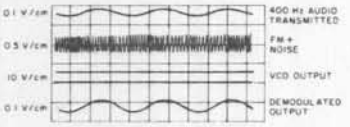


Fig. 11– Voltage waveforms of FM demodulator.

Frequency Synthesizer

The PLL system can function as a frequency-selective frequency multiplier by inserting a frequency divider into the feedback loop between the VCO output and the comparator input. Fig. 12 shows a COS/MOS low-frequency synthesizer with a programmable divider consisting of three decades. N, the frequency-divider modulus, can vary from 3 to 999 in steps of 1. When the PLL system is in lock, the signal and comparator inputs are at the same frequency and

$$f = N \times 1\ \text{kHz}$$

Therefore, the frequency range of this synthesizer is 3 to 999 kHz in 1-kHz increments, which is programmable by the switch position of the Divide-by-N counter.

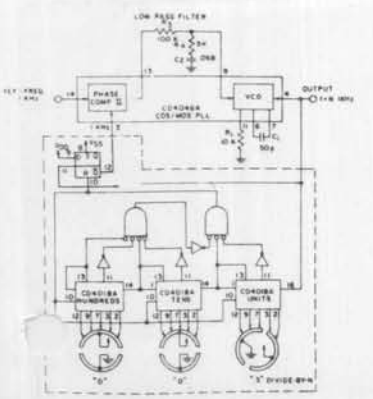


Fig. 12– Low-frequency synthesizer with three-decade programmable divider.

Phase-comparator II is used for this application because it will not lock on harmonics of the signal-input reference frequency (phase-comparator I does lock on harmonics). Since the duty cycle of the output of the Divide-by-N frequency divider is not 50 percent, phase-comparator II lends itself directly to this application.

Using the formulas for phase-comparator II shown in Table IV, the VCO is set up to cover a range of 0 to 1.1 MHz. The low-pass filter for this application is a two-pole, lag-lead filter which enables faster locking for step changes in frequency. Fig. 13 shows the waveforms during switching between output frequencies of 3 and 903 kHz. The figure shows that the transient going towards 3 kHz on the VCO control voltage is overdamped, while the transient to 903 kHz is underdamped. This condition could be improved by changing the value of R3 in the low-pass filter by means of adjustment of the switch-position hundreds in the Divide-by-N counter.

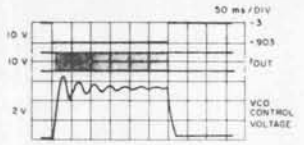


Fig. 13– Frequency-synthesizer waveforms.

Split-Phase Data Synchronization and Decoding

Fig. 14 shows another application of COS/MOS PLL, split-phase data synchronization and decoding. A split-phase data signal consists of a series of binary digits that occur at a periodic rate, as shown in waveform A in Fig. 14. The weight of each bit, 0 or 1, is random, but the duration of each bit, and therefore the periodic bit-rate, is essentially constant. To detect and process the incoming signal, it is necessary to have a clock that is synchronous with the data-bit rate. This clock signal must be derived from the incoming data signal. Phase-lock techniques can be utilized to recover the clock and the data. Timing information is contained in the data transitions, which can be positive or negative in direction, but both polarities have the same meaning for timing recovery. The phase of the signal determines the binary bit weight. A binary 0 or 1 is a positive or negative transition, respectively, during a bit interval in split-phase data signals.

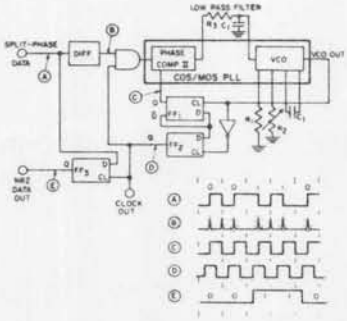


Fig. 14– Split-phase data synchronization and decoding.

As shown in Fig. 14, the split-phase data-input (A) is first differentiated to mark the locations of the data transitions. The differentiated signal, (B), which is twice the bit rate, is gated into the COS/MOS PLL. Phase-comparator II in the PLL is used because of its insensitivity to duty cycle on both the signal and comparator inputs. The VCO output is fed into the clock input of FF1 which divides the VCO frequency by two. During the ON intervals, the PLL tracks the differentiated signal (B); during the OFF intervals the PLL remembers the last frequency present and still provides a clock output. The VCO output is inverted and fed into the clock input of FF2 whose data input is the inverted output of FF1. FF2 provides the necessary phase shift in signal (C) to obtain signal (D), the recovered clock signal from the split-phase data transmission. The output of FF3, (E), is the recovered binary information from the phase information contained in the split-phase data. Initial synchronization of this PLL system is accomplished by a string of alternating 0's and 1's that precede the data transmission.

Phase-Locked-Loop Lock Detection

In some applications that utilize a PLL, it is sometimes necessary to have an output indication of when the PLL is in lock. One of the simplest forms of lock-condition indicator is a binary signal. For example, a 1 or a 0 output from a lock-detection circuit would correspond to a locked or unlocked condition, respectively. This signal could, in turn, activate circuitry utilizing a locked PLL signal. This detection could also be used in frequency-shift-keyed (FSK) data transmissions in which digital information is transmitted by switching the input frequency between either of two discrete input frequencies, one corresponding to a digital 1 and the other to a digital 0.

Fig. 15 shows a lock-detection scheme for the COS/MOS PLL. The signal input is switched between two discrete frequencies of 20 kHz and 10 kHz. The PLL system uses

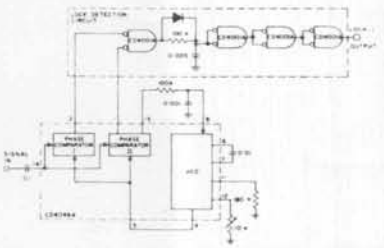


Fig. 15– Lock-detection circuit.

phase-comparator II; the VCO bandwidth is set up for an f_{min} of 9.5 kHz and an f_{max} of 10.5 kHz. Therefore, the PLL locks and unlocks on the 10-kHz and 20-kHz signals, respectively. When the PLL is in lock, the output of phase-comparator I is low except for some very short pulses that result from the inherent phase difference between the signal and comparator inputs; the phase-pulses output (terminal 1) is high except for some very small pulses resulting from the same phase difference. This low condition of phase comparator I is detected by the lock-detection circuit shown in Fig. 15. Fig. 16 shows the performance of this circuit when the input signal is switched between 20 and 10 kHz. It can be seen that after about five input cycles the lock detection signal goes high.

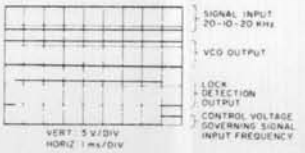


Fig. 16– Lock-detection-circuit waveforms.