Reducing a PLL's even-order harmonics

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In contrast to the clean output they produce when operated in their fundamental mode, phase-locked loops generate even-order harmonics of the input frequency and excessive sideband noise when used in frequency-divider or frequency-multiplier circuits. The spurious responses may be reduced, however, by adding an extra break or corner frequency to the PLL's low-pass filter response, in order to reduce the modulation index at the input to the loop's voltage-controlled oscillator.

A block diagram of a typical PLL frequency multiplier is shown in (a). Detector A_1 compares the phase of the input signal, f_1, with the phase of the divided-down VCO signal. Thus A_1 generates a voltage proportional to the phase difference between its inputs. After passing through low-pass filter A_2, the signal is applied to the VCO, A_3, so altering its output frequency f_2 that the phase difference between f_2 and f_1 is minimized. The loop is in the so-called locked state when f_1 equals f_2 in frequency and phase.

As a result of placing divider N in the loop to make the PLL operate as a frequency multiplier, the output of the phase detector and thus the loop, which is picked off at A_3, also contains unwanted harmonics of f_1. The amount of sideband noise on each carrier signal, which is an indication of the modulation index (a relation too cumbersome to derive for most waveforms), is given by:

$$\theta_0(s) = NK_0F(s)V_d/s$$

where F(s) is the transfer function of the loop's low-pass filter, V_d is A_1's output voltage, and K_0 is the voltage-to-frequency control constant of A_3. So, by reducing the numerical value of F(s), $\theta(s)$ and the modulation index fall and harmonics are also reduced.

The transfer function of the active loop filter typically used in PLL circuits (b) is $F_2(s) = (s\tau_2+1)/s\tau_1$, where $\tau_1 = R_1C$ and $\tau_2 = R_2C$. By adding capacitor C′ across R_2 as shown in (c), the second-order filter previously shown is made a third-order network, whose transfer function is given by $F_3(s) = (s\tau+s\tau_3+1)/(s^2\tau_1\tau_3+s\tau_1)$, where $\tau_3 = R_2C'$.

Note the corresponding curves of the filter's open-loop response. If the unwanted harmonics in question are all above the added pole frequency, $1/2\pi\tau_3$, they will be attenuated because the magnitude of $F_3(s)$ will be less than that of $F_2(s)$. At ω_{2f} in (b), there is no additional suppression beyond that which exists as a result of the integrating effects of the VCO and its low-pass filter. The attenuation is increased with the addition of C′ as shown in (c).

Adding C′ creates a network that, under some conditions, can be unstable. However, as long as the open-loop gain of the originally stable second-order loop is unchanged after C′ is added, and the slope at which the loop's log-magnitude plot crosses the unity-gain axis does not exceed −40 decibels per decade, there will be no problem. Both of these conditions are normally found in practice.

Adding the additional break point affects the network's damping factor, δ, and the system bandwidth, B, two of the most important parameters of interest in designing a loop filter. The effects of damping start to become noticeable when τ_3 starts to move down from infinity to $\tau_2/30$. It should be understood that with a reduction in harmonic output also comes a decrease in the range over which the PLL will operate.

As an example of how to design a filter network, consider the case where a PLL multiplier is to be scaled to generate a frequency f_{out} equal to $(108/109)f_{in}$, having a damping factor of 1.2 and a bandwidth of 100 hertz. Thus the VCO is made to multiply f_{in} by 108, and a divider is used to provide N = 109. Along with the initial considerations, an additional requirement is to suppress the sidebands at the divider output by 50 dB. This corresponds to a phase jitter of 0.4°.

A standard second-order filter design can meet the damping and bandwidth criteria, but a third-order filter is required to meet the sideband suppression and phase jitter requirements.

It will be realized that it is necessary to reduce the

first-order sidebands at least 10 dB, if the sidebands at the output of the divide-by-109 unit are to be at least 50 dB below the peak output voltage. By using the well-known two-pole RC filter equations (this discussion assumes familiarity with the design procedures of basic PLL filters), and setting δ to 2.2 and B to 100 Hz to get V_0 = 10 dB below V_d, it is found that $\tau_1 = 6.7(10^{-2})$ and $\tau_2 = 5.09(10^{-2})$. R_1, R_2, and C can then be appropriately selected.

From (d), an experimental curve generated for use in designing the three-pole filter, it is found that an *equivalent* second-order damping factor of 1.1 is obtained for such a loop when N = 21.2 and $\tau_3 = \tau_2/N = 2.5(10^{-3})$. Thus $C' = \tau_3/R_2 = 0.5$ microfarad if R_2 = 50 kilohms, a typical value of resistance. □

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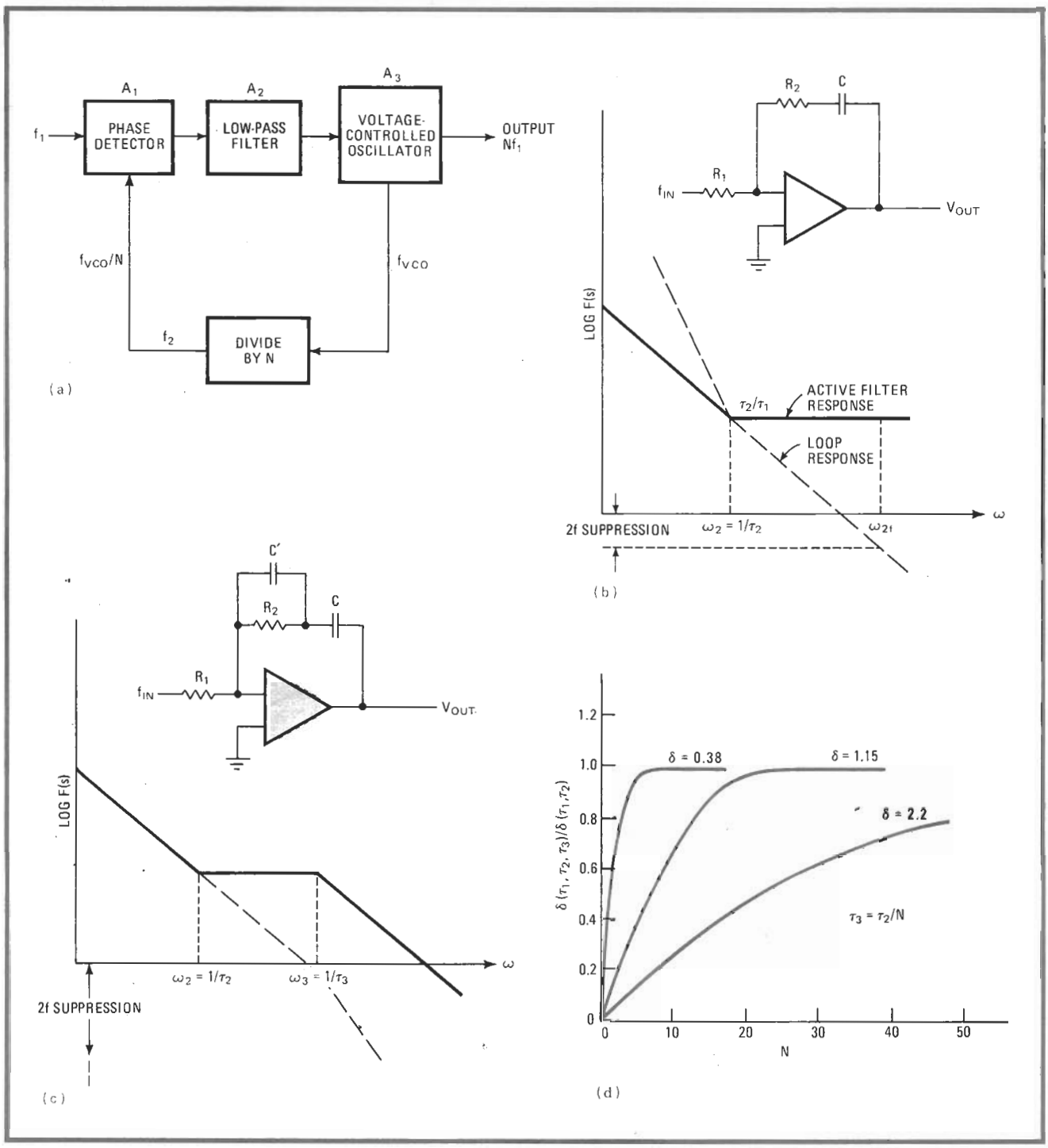

Break point. Phase-locked loop (a) generates spurious energy when used in frequency-multiplying circuits. Low-pass filter (b) cannot provide sufficient input frequency harmonic suppression. Capacitor C′ (c) adds break or corner frequency to filter response, enables increased rejection of even-order harmonics. Effects of τ_3 on equivalent second-order damping are plotted (d) to aid in design example discussed in text.