Phase-Locked Loops for High-Frequency Receivers and Transmitters—Part 1

by Mark Curtin and Paul O'Brien

This 3-part series of articles is intended to give a comprehensive overview of the use of PLLs (phase-locked loops) in both wired and wireless communication systems.

In this first part, the emphasis is on the introductory concepts of PLLs. The basic PLL architecture and principle of operation is described. We will also give an example of where PLLs are used in communication systems. We will finish the first installment by showing a practical PLL circuit using the ADF4111 Frequency Synthesizer and the VCO190-902T Voltage-Controlled Oscillator.

In the second part, we will examine in detail the critical specifications associated with PLLs: phase noise, reference spurs and output leakage current. What causes these and how can they be minimized? What effect do they have on system performance?

The final installment will contain a detailed description of the blocks that go to make up a PLL synthesizer and the architecture of an Analog Devices synthesizer. There will also be a summary of synthesizers and VCOs currently available on the market, with a list of ADI's current offerings.

PLL BASICS

A phase-locked loop is a feedback system combining a voltage-controlled oscillator and a phase comparator so connected that the oscillator maintains a constant phase angle relative to a reference signal. Phase-locked loops can be used, for example, to generate stable output frequency signals from a fixed low-frequency signal. The first phase-locked loops were implemented in the early 1930s by a French engineer, de Bellescize. However, they only found broad acceptance in the marketplace when integrated PLLs became available as relatively low-cost components in the mid-1960s.

The phase locked loop can be analyzed in general as a negative-feedback system with a forward gain term and a feedback term.

A simple block diagram of a voltage-based negative-feedback system is shown in Figure 1.

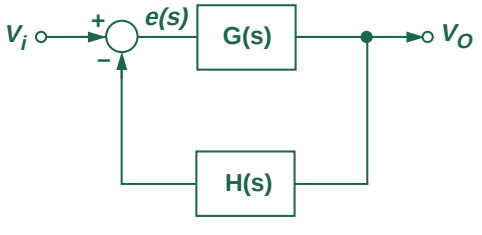

Figure 1. Standard negative-feedback control system model.

In a phase-locked loop, the error signal from the phase comparator is proportional to the relative phase of the input and feedback signals. The average output of the phase detector will be constant when the input and feedback signals are the same frequency. The usual equations for a negative-feedback system apply.

$$Forward\ Gain = G(s),\ [s = j\omega = j2\pi f]$$

$$Loop\ Gain = G(s) \times H(s)$$

$$Closed\text{-}Loop\ Gain = \frac{G(s)}{1 + G(s)H(s)}$$

Because of the integration in the loop, at low frequencies the steady state gain, $G(s)$, is high and

$$V_O/V_I,\ Closed\text{-}Loop\ Gain = \frac{1}{H}$$

The components of a PLL that contribute to the loop gain include:

1. The *phase detector* (PD) and *charge pump* (CP).
2. The *loop filter*, with a transfer function of $Z(s)$
3. The *voltage-controlled oscillator* (VCO), with a sensitivity of K_V/s
4. The *feedback divider*, $1/N$

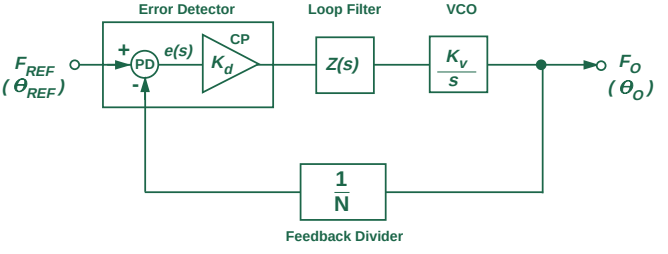

Figure 2. Basic phase-locked-loop model.

If a linear element like a four-quadrant multiplier is used as the phase detector, and the loop filter and VCO are also analog elements, this is called an analog, or *linear PLL* (LPLL).

If a *digital* phase detector (EXOR gate or J-K flip flop) is used, and everything else stays the same, the system is called *a digital PLL* (DPLL).

If the PLL is built exclusively from digital blocks, without any passive components or linear elements, it becomes an *all-digital PLL* (ADPLL).

Finally, with information in digital form, and the availability of sufficiently fast processing, it is also possible to develop PLLs in the software domain. The PLL function is performed by software and runs on a DSP. This is called a *software PLL* (SPLL).

Referring to Figure 2, a system for using a PLL to generate higher frequencies than the input, the VCO oscillates at an angular frequency of ω_O. A portion of this signal is fed back to the error detector, via a frequency divider with a ratio 1/N. This divided-down frequency is fed to one input of the error detector. The other input in this example is a fixed reference signal. The error detector compares the signals at both inputs. When the two signal inputs are equal in frequency, the error will be constant and the loop is said to be in a "locked" condition. If we simply look at the error signal, the following equations may be developed.

$$e(s) = \Phi_{REF} - \frac{\Phi_O}{N}$$

$$\frac{de(s)}{dt} = F_{REF} - \frac{F_O}{N}$$

When

$$e(s) = constant, \frac{F_O}{N} = F_{REF}$$

Thus

$$F_O = N\ F_{REF}$$

In commercial PLLs, the phase detector and charge pump together form the error detector block. When $F_O \neq N F_{REF}$, the error detector will output source/sink current pulses to the low-pass loop filter. This smooths the current pulses into a voltage which in turn drives the VCO. The VCO frequency will then increase or decrease as necessary, by K_V DV, where K_V is the VCO sensitivity in MHz/Volt and DV is the change in VCO input voltage. This will continue until $e(s)$ is zero and the loop is locked. The charge pump and VCO thus serves as an integrator, seeking to increase or decrease its output frequency to the value required so as to restore its input (from the phase detector) to zero.

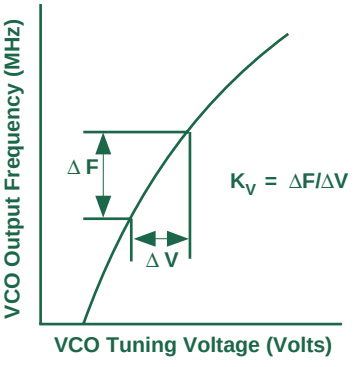

Figure 3. VCO transfer function.

The overall transfer function (CLG or Closed-Loop Gain) of the PLL can be expressed simply by using the CLG expression for a negative feedback system as given above.

$$\frac{F_O}{F_{REF}} = \frac{Forward\ Gain}{1 + Loop\ Gain}$$

$$Forward\ Gain, G = \frac{K_D\ K_V\ Z(s)}{s}$$

$$Loop\ Gain, GH = \frac{K_D\ K_V\ Z(s)}{Ns}$$

When GH is much greater than 1, we can say that the closed loop transfer function for the PLL system is N and so

$$F_{OUT} = N \times F_{REF}$$

The loop filter is a low-pass type, typically with one pole and one zero. The transient response of the loop depends on:

1. the magnitude of the pole/zero,
2. the charge pump magnitude,
3. the VCO sensitivity,
4. the feedback factor, N.

All of the above must be taken into account when designing the loop filter. In addition, the filter must be designed to be stable (usually a phase margin of $\pi/4$ is recommended). The 3-dB cutoff frequency of the response is usually called the loop bandwidth, B_W. Large loop bandwidths result in very fast transient response. However, this is not always advantageous, as we shall see in Part 2, since there is a tradeoff between fast transient response and reference spur attenuation.

PLL APPLICATIONS TO FREQUENCY UPSCALING

The phase-locked loop allows stable high frequencies to be generated from a low-frequency reference. Any system that requires stable high frequency tuning can benefit from the PLL technique. Examples of these applications include wireless base stations, wireless handsets, pagers, CATV systems, clock-recovery and -generation systems. A good example of a PLL application is a GSM handset or base station. Figure 4 shows the receive section of a GSM base station.

In the GSM system, there are 124 channels (8 users per channel) of 200-kHz width in the RF band. The total bandwidth occupied is 24.8 MHz, which must be scanned for activity. The handset has a transmit (Tx) range of 880 MHz to 915 MHz and a receive (Rx) range of 925 MHz to 960 MHz. Conversely, the base station has a Tx range of 925 MHz to 960 MHz and an Rx range of 880 MHz to 915 MHz. For this example, we will consider just the base station transmit and receive sections. The frequency bands for GSM900 and DCS1800 Base Station Systems are shown in Table 1. Table 2 shows the channel numbers for the carrier frequencies (RF channels) within the frequency bands of Table 1. $Fl(n)$ is the center frequency of the RF channel in the lower band (Rx) and $Fu(n)$ is the corresponding frequency in the upper band (Tx).

Table 1. Frequency Bands for GSM900 and DCS1800 Base Station Systems

	Tx	Rx
P-GSM900	935 to 960 MHz	890 to 915 MHz
DCS1800	1805 to 1880 MHz	1710 to 1785 MHz
E-GSM900	925 to 960 MHz	880 to 915 MHz

Table 2. Channel Numbering for GSM900 and DCS1800 Base Station Systems

	Rx		Tx
PGSM900	Fl(n) = 890 + 0.2 × (n)	1 ≤ n ≤ 124	Fu(n) = Fl(n) + 45
EGSM900	Fl(n) = 890 + 0.2 × (n) Fl(n) = 890 + 0.2 × (n – 1024)	0 ≤ n ≤ 124 975 ≤ n ≤ 1023	Fu(n) = Fl(n) + 45
DCS1800	Fl(n) = 1710.2 + 0.2 × (n – 512)	512 ≤ n ≤ 885	Fu(n) = Fl(n) + 95

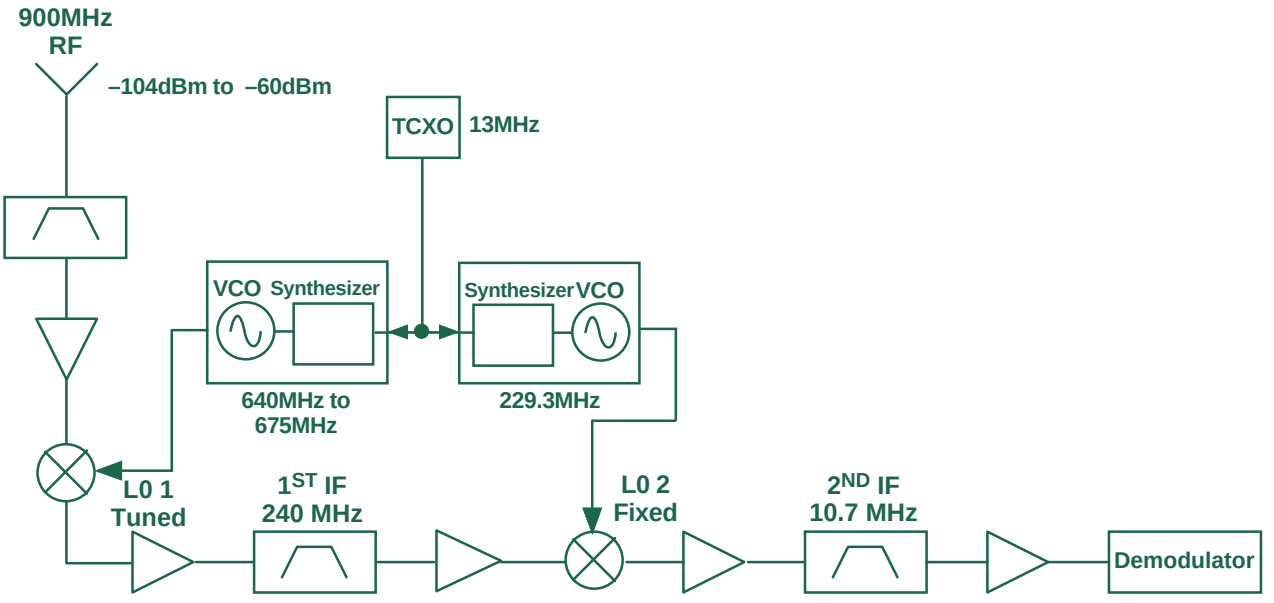

Figure 4. Signal chain for GMS base-station receiver.

The 900-MHz RF input is filtered, amplified and applied to the first stage mixer. The other mixer input is driven from a tuned local oscillator (LO). This must scan the input frequency range to search for activity on any of the channels. The actual implementation of the LO is by means of the PLL technique already described. If the 1st intermediate-frequency (IF) stage is centered at 240 MHz, then the LO must have a range of 640 MHz to 675 MHz in order to cover the RF input band. When a 200-kHz reference frequency is chosen, it will be possible to sequence the VCO output through the full frequency range in steps of 200 kHz. For example, when an output frequency of 650 MHz is desired, N will have a value of 3250. This 650-MHz LO will effectively check the 890-MHz RF channel ($F_{RF} - F_{LO} = F_{IF}$ or $F_{RF} = F_{LO} + F_{IF}$). When N is incremented to 3251, the LO frequency will now be 650.2 MHz and the RF channel checked will be 890.2 MHz. This is shown graphically in Figure 5.

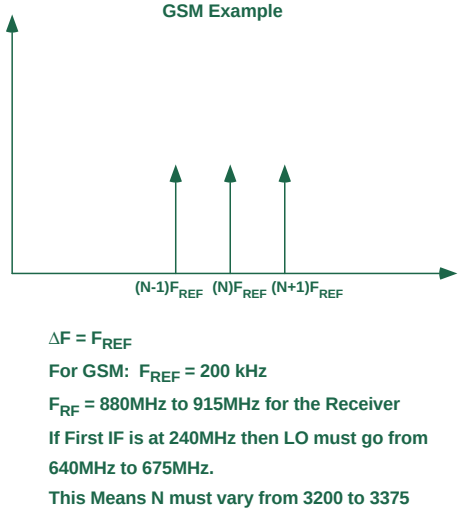

Figure 5. Testing frequencies for GSM base-station receiver.

It is worth noting that, in addition to the tunable RF LO, the receiver section also uses a fixed IF (in the example shown this is 240 MHz). Even though frequency tuning is not needed on this IF, the PLL technique is still used. The reason for this is that it is an affordable way of using the stable system reference frequency to produce the high frequency IF signal. Several synthesizer manufacturers recognize this fact by offering dual versions of the devices: one operating at the high RF frequency (>800 MHz) and one operating at the lower IF frequency (500 MHz or less).

On the transmit side of the GSM system, similar requirements exist. However, it is more common to go directly from baseband to the final RF in the Transmit section; this means that the typical T_X VCO for a base station has a range of 925 MHz to 960 MHz (RF band for the Transmit section).

CIRCUIT EXAMPLE

Figure 6 shows an actual implementation of the local oscillator for the transmit section of a GSM handset. We are assuming direct baseband to RF up-conversion. This circuit uses the new ADF4111 PLL Frequency Synthesizer from ADI and the VCO190-902T Voltage Controlled Oscillator from Vari-L Corporation (http://www.vari-L.com/).

The reference input signal is applied to the circuit at $FREF_{IN}$ and is terminated in 50 Ω. This reference input frequency is typically 13 MHz in a GSM system. In order to have a channel spacing of 200 kHz (the GSM standard), the reference input must be divided by 65, using the on-chip reference divider of the ADF4111.

The ADF4111 is an integer-N PLL frequency synthesizer, capable of operating up to an RF frequency of 1.2 GHz. In this integer-N type of synthesizer, N can be programmed from 96 to 262,000 in discrete integer steps. In the case of the handset transmitter, where an output range of 880 MHz to 915 MHz is needed, and where the internal reference frequency is 200 kHz, the desired N values will range from 4400 to 4575.

The charge pump output of the ADF4111 (Pin 2) drives the loop filter. This filter ($Z(s)$ in Figure 2) is basically a 1st-order lag-lead type. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system would be 45 degrees. Other PLL system specifications are given below:

K_D = 5 mA
K_V = 8.66 MHz/V
Loop Bandwidth = 12 kHz
F_{REF} = 200 kHz
N = 4500
Extra Reference Spur Attenuation = 10 dB

All of these specifications are needed and used to come up with the loop filter components values shown in Figure 6.

The loop filter output drives the VCO, which, in turn, is fed back to the RF input of the PLL synthesizer and also drives the RF Output terminal. A T-circuit configuration with 18-ohm resistors is used to provide 50-ohm matching between the VCO output, the RF output and the RF_{IN} terminal of the ADF4111.

In a PLL system, it is important to know when the system is in lock. In Figure 6, this is accomplished by using the MUXOUT signal from the ADF4111. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or *lock-detect* signal. When MUXOUT is chosen to select lock detect, it can be used in the system to trigger the output power amplifier, for example.

The ADF4111 uses a simple 4-wire serial interface to communicate with the system controller. The reference counter, the N counter and various other on-chip functions are programmed via this interface.

CONCLUSION

In this first part of the series, we have introduced the basic concepts of PLLs with simple block diagrams and equations. We have shown a typical example of where the PLL structure is used and given a detailed description of a practical implementation.

In the next installment, we will delve deeper into the specifications which are critical to PLLs and discuss their system implications.

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1. Mini-Circuits Corporation, "VCO Designers Handbook."
2. L.W. Couch, "Digital and Analog Communications Systems" Macmillan Publishing Company, New York.
3. P. Vizmuller, "RF Design Guide," Artech House.
4. R.L. Best, "Phase Locked Loops: Design, Simulation and Applications," 3rd Edition, McGraw Hill.

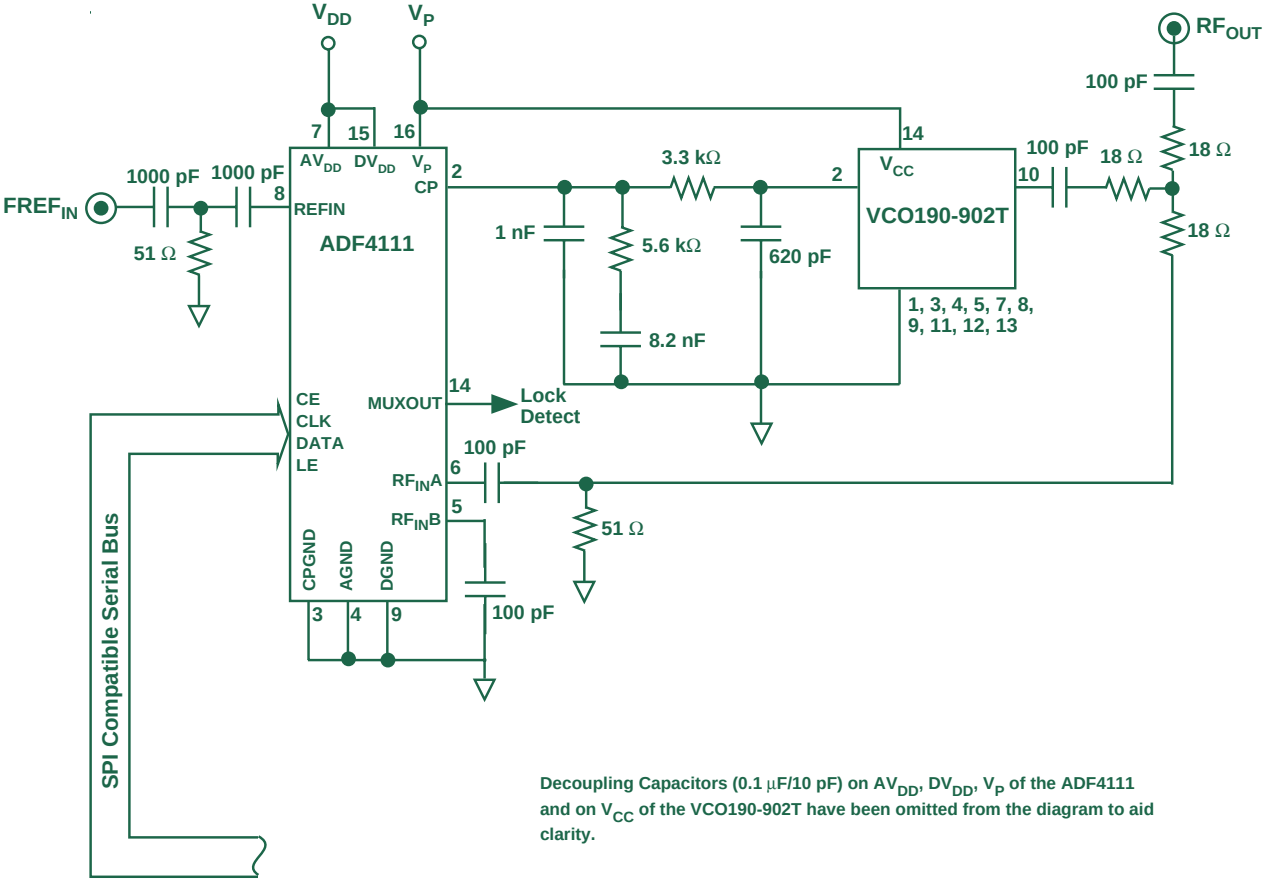

Figure 6. Transmitter local oscillator for GSM handset.

Phase-Locked Loops for High-Frequency Receivers and Transmitters—Part 2

by Mike Curtin and Paul O'Brien

The *first part* of this series of articles introduced the basic concepts of *phase-locked loops* (PLLs). The PLL architecture and principle of operation was described and accompanied by an example of where a PLL might be used in a communication system.

In this second part, we will focus on a detailed examination of two critical specifications associated with PLLs: *phase noise* and *reference spurs*. What causes them and how can they be minimized? The discussion will include measurement techniques and the effect of these errors on system performance. We will also consider *output leakage current*, with an example showing its significance in open-loop modulation schemes.

Noise in Oscillator Systems

In any oscillator design, frequency stability is of critical importance. We are interested in both long-term and short-term stability. *Long-term* frequency stability is concerned with how the output signal varies over a long period of time (hours, days or months). It is usually specified as the ratio, $\Delta f/f$ for a given period of time, expressed as a percentage or in dB.

Short-term stability, on the other hand, is concerned with variations that occur over a period of seconds or less. These variations can be random or periodic. A spectrum analyzer can be used to examine the short-term stability of a signal. Figure 1 shows a typical spectrum, with random and discrete frequency components causing a broad skirt and spurious peaks.

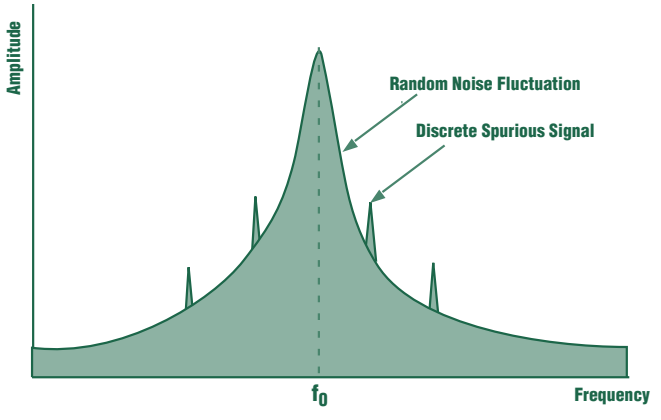

Figure 1. Short-term stability in oscillators.

The discrete spurious components could be caused by known clock frequencies in the signal source, power line interference, and mixer products. The broadening caused by random noise fluctuation is due to *phase noise*. It can be the result of thermal noise, shot noise and/or flicker noise in active and passive devices.

Phase Noise in Voltage-Controlled Oscillators

Before we look at phase noise in a PLL system, it is worth considering the phase noise in a *voltage-controlled oscillator* (VCO). An ideal VCO would have no phase noise. Its output as seen on a spectrum analyzer would be a single spectral line. In practice, of course, this is not the case. There will be jitter on the output, and a spectrum analyzer would show phase noise. To help understand phase noise, consider a phasor representation, such as that shown in Figure 2.

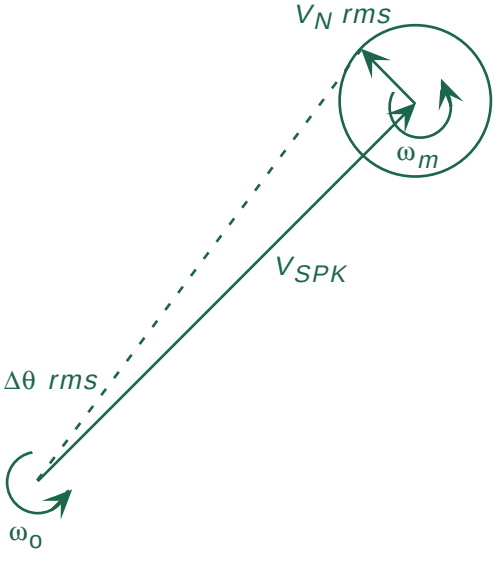

Figure 2. Phasor representation of phase noise.

A signal of angular velocity ω_O and peak amplitude V_{SPK} is shown. Superimposed on this is an error signal of angular velocity ω_m. $\Delta\theta$rms represents the rms value of the phase fluctuations and is expressed in rms degrees.

In many radio systems, an overall integrated phase error specification must be met. This overall phase error is made up of the PLL phase error, the modulator phase error and the phase error due to base band components. In GSM, for example, the total allowed is 5 degrees rms.

Leeson's Equation

Leeson (see Reference 6) developed an equation to describe the different noise components in a VCO.

$$L_{PM} \approx 10\log\left[\frac{FkT}{A}\frac{1}{8Q_L^2}\left(\frac{f_O}{f_m}\right)^2\right] \quad (1)$$

where:

L_{PM} is single-sideband phase noise density (dBc/Hz)
F is the device noise factor at operating power level A (linear)
k is Boltzmann's constant, 1.38×10^{-23} J/K
T is temperature (K)
A is oscillator output power (W)
Q_L is loaded Q (dimensionless)
f_O is the oscillator carrier frequency
f_m is the frequency offset from the carrier

For Leeson's equation to be valid, the following must be true:

- f_m, the offset frequency from the carrier, is greater than the 1/f flicker corner frequency;
- the noise factor at the operating power level is known;
- the device operation is linear;
- Q includes the effects of component losses, device loading and buffer loading;
- a single resonator is used in the oscillator.

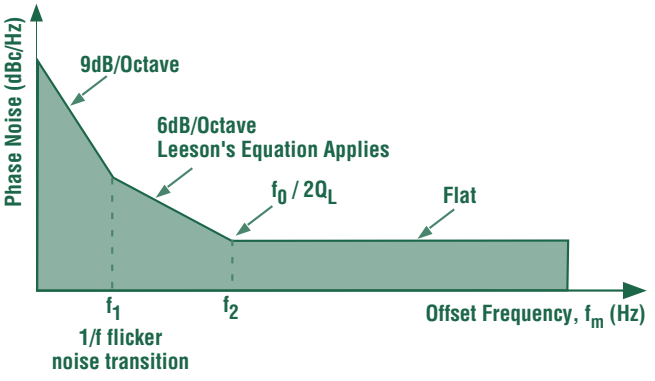

Figure 3. Phase noise in a VCO vs. frequency offset.

Leeson's equation only applies in the knee region between the break (f_1) to the transition from the "1/f" (more generally 1/f$^\gamma$) flicker noise frequency to a frequency beyond which amplified white noise dominates (f_2). This is shown in Figure 3 [$\gamma = 3$]. f_1 should be as low as possible; typically, it is less than 1 kHz, while f_2 is in the region of a few MHz. High-performance oscillators require devices specially selected for low 1/f transition frequency. Some guidelines to minimizing the phase noise in VCOs are:

1. Keep the tuning voltage of the varactor sufficiently high (typically between 3 and 3.8 V)
2. Use filtering on the dc voltage supply.
3. Keep the inductor Q as high as possible. Typical off-the-shelf coils provide a Q of between 50 and 60.
4. Choose an active device that has minimal noise figure as well as low flicker frequency. The flicker noise can be reduced by the use of feedback elements.
5. Most active device exhibit a broad U-shaped noise-figure-vs.-bias-current curve. Use this information to choose the optimal operating bias current for the device.
6. Maximize the average power at the tank circuit output.
7. When buffering the VCO, use devices with the lowest possible noise figure.

Closing The Loop

Having looked at phase noise in a free-running VCO and considered how it can be minimized, we will now consider the effect of closing the loop (see *Part 1* of the series) on phase noise.

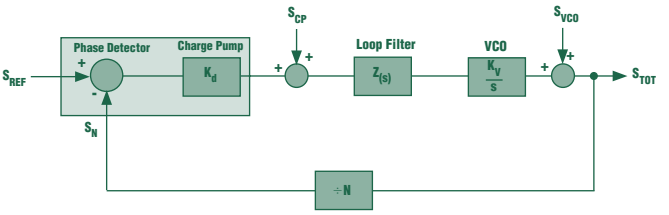

Figure 4. PLL-phase-noise contributors.

Figure 4 shows the main phase noise contributors in a PLL. The system transfer function may be described by the following equations.

$$Closed\ Loop\ Gain = \frac{G}{1 + GH} \tag{2}$$

$$G = \frac{K_d \times K_v \times Z(s)}{s} \tag{3}$$

$$H = \frac{1}{N} \tag{4}$$

$$Closed\ Loop\ Gain = \frac{\frac{K_d \times K_v \times Z(s)}{s}}{\frac{K_d \times K_v \times Z(s)}{N \times s}} \tag{5}$$

For the discussion that follows, we will define S_{REF} as the noise that appears on the reference input to the phase detector. It is dependent on the reference divider circuitry and the spectral purity of the main reference signal. S_N is the noise due to the feedback divider appearing at the frequency input to the phase detector. S_{CP} is the noise due to the phase detector (depending on its implementation). And S_{VCO} is the phase noise of the VCO as described by equations developed earlier.

The overall phase noise performance at the output depends on the terms described above. All the effects at the output are added in an rms fashion to give the total noise of the system. Thus:

$$S_{TOT}{}^2 = X^2 + Y^2 + Z^2 \tag{6}$$

where:

$S_{TOT}{}^2$ is the total phase noise power at the output

X^2 is the noise power at the output due to S_N and S_{REF}.

Y^2 is the noise power at the output due to S_{CP}.

Z^2 is the noise power at the output due to S_{VCO}.

The noise terms at the PD inputs, S_{REF} and S_N, will be operated on in the same fashion as F_{REF} and will be multiplied by the closed loop gain of the system.

$$X^2 = \left(S_{REF}{}^2 + S_N{}^2\right) \times \left(\frac{G}{1 + GH}\right)^2 \tag{7}$$

At low frequencies, inside the loop bandwidth,

$$GH >> 1\ and\ X^2 = \left(S_{REF}{}^2 + S_N{}^2\right) \times N^2 \tag{8}$$

At high frequencies, outside the loop bandwidth,

$$G << 1 \; and \; X^2 \Rightarrow 0 \tag{9}$$

The overall output noise contribution due to the phase detector noise, S_{CP}, can be calculated by referencing S_{CP} back to the input of the PFD. The equivalent noise at the PD input is S_{CP}/K_d. This is then multiplied by the closed-loop gain:

$$Y^2 = {S_{CP}}^2 \times \left(\frac{1}{K_d}\right)^2 \times \left(\frac{G}{1+GH}\right)^2 \tag{10}$$

Finally, the contribution of the VCO noise, S_{VCO}, to the output phase noise is calculated in a similar manner. The forward gain this time is simply 1. Therefore its contribution to the output noise is:

$$Z^2 = {S_{VCO}}^2 \times \left(\frac{1}{1+GH}\right)^2 \tag{11}$$

G, the forward loop gain of the closed loop response, is usually a low pass function; it is very large at low frequencies and small at high frequencies. H is a constant, 1/N. The denominator of the above expression is therefore low pass, so S_{VCO} is actually high-pass filtered by the closed loop.

A similar description of the noise contributors in a PLL/VCO can be found in Reference 1. Recall that the closed-loop response is a low-pass filter with a 3-dB cutoff frequency, B_W, denoted the *loop bandwidth*. For frequency offsets at the output less than B_W, the dominant terms in the output phase noise response are X and Y, the noise terms due to reference noise, N (counter noise), and charge pump noise. Keeping S_N and S_{REF} to a minimum, keeping K_d large and keeping N small will thus minimize the phase noise inside the loop bandwidth, B_W. Because N programs the output frequency, it is not generally available as a factor in noise reduction.

For frequency offsets much greater than B_W, the dominant noise term is that due to the VCO, S_{VCO}. This is due to the high pass filtering of the VCO phase noise by the loop. A small value of B_W would be desirable as it would minimize the total integrated output noise (phase error). However a small B_W results in a slow transient response and increased contribution from the VCO phase noise inside the loop bandwidth. The loop bandwidth calculation therefore must trade off transient response and total output integrated phase noise.

To show the effect of closing the loop on a PLL, Figure 5 shows an overlay of the output of a free-running VCO and the output of a VCO as part of a PLL. Note that the in-band noise of the PLL has been attenuated compared to that of the free-running VCO.

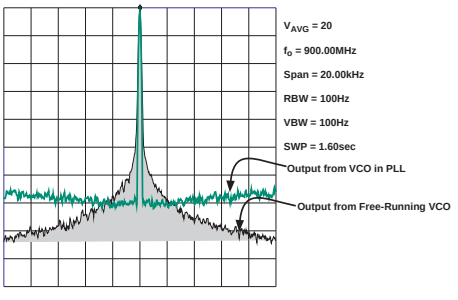

Figure 5. Phase noise on a free-running VCO and a PLL-connected VCO.

Phase Noise Measurement

One of the most common ways of measuring phase noise is with a high frequency spectrum analyzer. Figure 6 is a typical example of what would be seen.

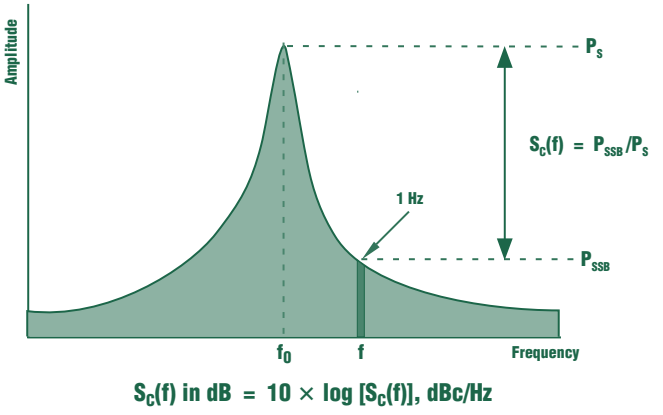

Figure 6. Phase noise definition.

With the spectrum analyzer we can measure the spectral density of phase fluctuations per unit bandwidth. VCO phase noise is best described in the frequency domain where the spectral density is characterized by measuring the noise sidebands on either side of the output signal center frequency. Phase noise power is specified in decibels relative to the carrier (dBc/Hz) at a given frequency offset from the carrier. The following equation describes this SSB phase noise (dBc/Hz).

$$S_C(f) = 10 \log \frac{P_S}{P_{SSB}} \tag{12}$$

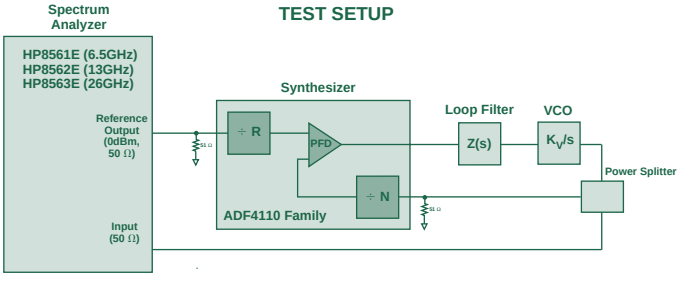

Figure 7. Measuring phase noise with a spectrum analyzer.

The 10-MHz, 0-dBm reference oscillator, available on the spectrum analyzer's rear-panel connector, has excellent phase noise performance. The R divider, N divider, and the phase detector are part of ADF4112 frequency synthesizer. These dividers are programmed serially under the control of a PC. The frequency and phase noise performance are observed on the spectrum analyzer.

Figure 8 illustrates a typical phase noise plot of a PLL synthesizer using an ADF4112 PLL with a Murata VCO, MQE520-1880. The frequency and phase noise were measured in a 5-kHz span. The reference frequency used was f_{REF} = 200 kHz (R = 50) and the output frequency was 1880 MHz (N = 9400). If this were an ideal-world PLL synthesizer, a single discrete tone would be displayed rising up above the spectrum analyzer's noise floor. What is displayed here is the tone, with the phase noise due to the loop components. The loop filter values were chosen to give a loop

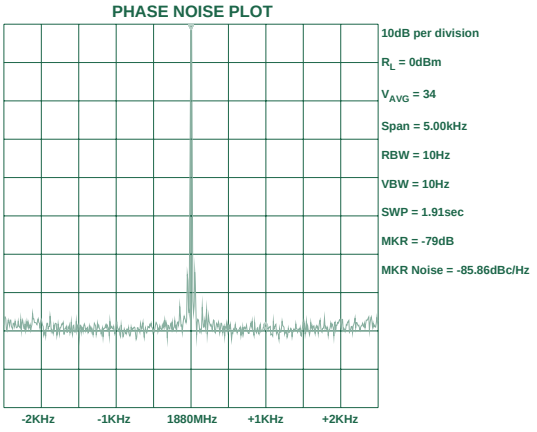

Figure 8. Typical spectrum-analyzer output.

bandwidth of approximately 20 kHz. The flat part of the phase noise for frequency offsets less than the loop bandwidth is actually the phase noise as described by X^2 and Y^2 in the section "closing the loop" for cases where f is inside the loop bandwidth. It is specified at a 1-kHz offset. The value measured, the phase-noise power in a 1-Hz bandwidth, was –85.86 dBc/Hz. It is made up of the following:

1. Relative power in dBc between the carrier and the sideband noise at 1-kHz offset.
2. The spectrum analyzer displays the power for a certain resolution bandwidth (RBW). In the plot, a 10-Hz RBW is used. To represent this power in a 1-Hz bandwidth, 10log(RBW) must be subtracted from the value obtained from (1).
3. A correction factor, which takes into account the implementation of the RBW, the log display mode and detector characteristic, must be added to the result obtained in (2).
4. Phase noise measurement with the HP 8561E can be made quickly by using the marker noise function, MKR NOISE. This function takes into account the above three factors and displays the phase noise in dBc/Hz.

The phase noise measurement above is the total output phase noise at the VCO output. If we want to estimate the contribution of the PLL device (noise due to phase detector, R&N dividers and the phase detector gain constant), the result must be divided by N^2 (or $20 \times \log N$ be subtracted from the above result). This gives a phase-noise floor of $[-85.86 - 20 \times \log(9400)] = -165.3$ dBc/Hz.

Reference Spurs

In an integer-N PLL (where the output frequency is an integer multiple of the reference input), reference spurs are caused by the fact that the charge pump output is being continuously updated at the reference frequency rate. Consider

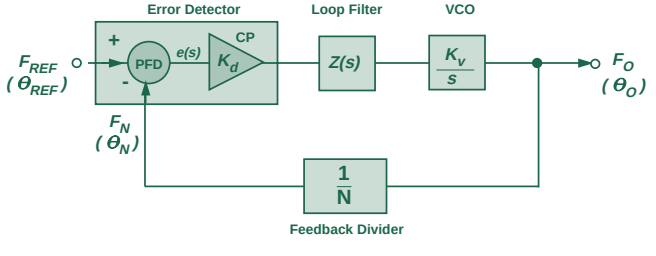

Figure 9. Basic PLL model.

again the basic model for the PLL which was discussed in Part 1 of this series. This is shown again in Figure 9.

When the PLL is in lock, the phase and frequency inputs to the PFD (f_{REF} and f_N) are essentially equal, and, in theory, one would expect that there to be no output from the PFD. However, this can create problems (to be discussed in Part 3 of this series), so the PFD is designed such that, in the locked condition, the current pulses from the charge pump will typically be as shown in Figure 10.

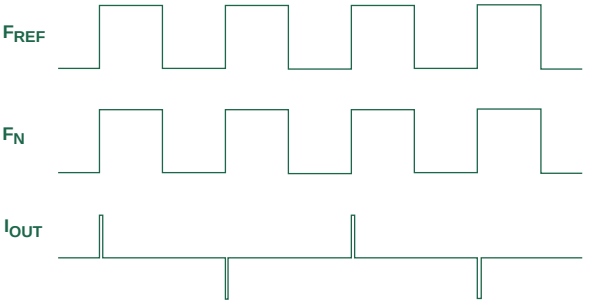

Figure 10. Output current pulses from the PFD charge pump.

Although these pulses have a very narrow width, the fact that they exist means that the dc voltage driving the VCO is modulated by a signal of frequency f_{REF}. This produces *reference spurs* in the RF output occurring at offset frequencies that are integer multiples of f_{REF}. A spectrum analyzer can be used to detect reference spurs. Simply increase the span to greater than twice the reference frequency. A typical plot is shown in Figure 11. In this case the reference frequency is 200 kHz and the diagram clearly shows reference spurs at ±200 kHz from the RF output of 1880 MHz. The level of these spurs is –90 dB. If the span were increased to more than four times the reference frequency, we would also see the spurs at $(2 \times f_{REF})$.

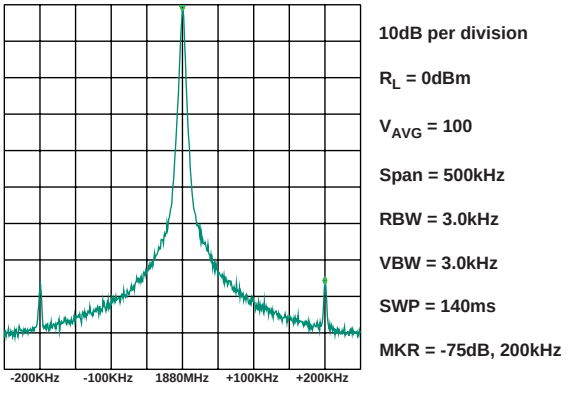

Figure 11. Output spectrum showing reference spurs.

Charge Pump Leakage Current

When the CP output from the synthesizer is programmed to the high impedance state, there should, in theory, be no leakage current flowing. In practice, in some applications the level of leakage current will have an impact on overall system performance. For example, consider an application where a PLL is used in open-loop mode for frequency modulation—a simple and inexpensive way of implementing FM that also allows higher data rates than modulating in closed-loop mode. For FM, a closed-loop method works fine but the data rate is limited by the loop bandwidth.

A system that uses open-loop modulation is the European cordless telephone system, DECT. The output carrier frequencies are in a range of 1.77 GHz to 1.90 GHz and the data rate is high; 1.152 Mbps.

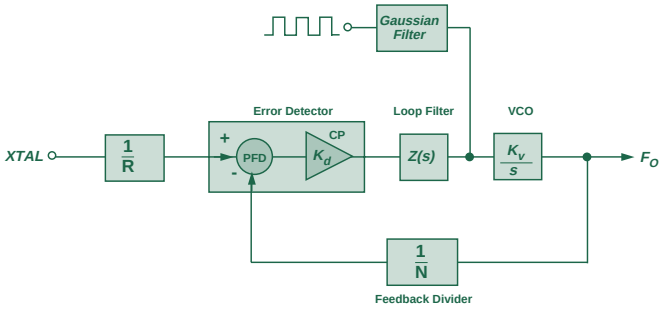

Figure 12. Block diagram of open-loop modulation.

A block diagram of open-loop modulation is shown in Figure 12. The principle of operation is as follows: The loop is initially closed to lock the RF output, $f_{OUT} = N f_{REF}$. The modulating signal is turned on and at first the modulation signal is simply the dc mean of the modulation. The loop is then opened, by putting the CP output of the synthesizer into high-impedance mode, and the modulation data is fed to the Gaussian filter. The modulating voltage then appears at the VCO where it is multiplied by K_V. When the data burst finishes, the loop is returned to the closed loop mode of operation.

As the VCO usually has a high sensitivity (typical figures are between 20 and 80 MHz/volt), any small voltage drift before the VCO will cause the output carrier frequency to drift. This voltage drift, and hence the system frequency drift, is directly dependent on the leakage current of the charge pump, CP, when in the high impedance state. This leakage will cause the loop capacitor to charge or discharge depending on the polarity of the leakage current. For example, a leakage current of 1 nA would cause the voltage on the loop capacitor (1000 pF for example) to charge or discharge by dV/dt = I/C (1 V/s in this case). This, in turn, would cause the VCO to drift. So, if the loop is open for 1 ms and the K_V of the VCO is 50 MHz/Volt, the frequency drift caused by 1-nA leakage into a 1000-pF loop capacitor would be 50 kHz. In fact, the DECT bursts are generally shorter (0.5 ms), so the drift will be even less in practice for the loop capacitance and leakage current used in the example. However, it does serve to illustrate the importance of charge-pump leakage in this type of application.

Receiver Sensitivity

Receiver sensitivity specifies the ability of the receiver to respond to a weak signal. Digital receivers use maximum bit-error rate (BER) at a certain rf level to specify performance. In general, device gains, noise figures, image noise, and local-oscillator (LO) wideband noise all combine to produce an equivalent noise figure. This is then used to calculate the overall receiver sensitivity.

Wideband noise in the LO can elevate the IF noise level and thus degrade the overall noise factor. For example, wideband phase noise at $F_{LO} + F_{IF}$ will produce noise products at F_{IF}. This directly impacts the receiver sensitivity. This wideband phase noise is primarily dependent on the VCO phase noise.

Close-in phase noise in the LO will also impact sensitivity. Obviously, any noise close to F_{LO} will produce noise products close to F_{IF} and impact sensitivity directly.

Receiver Selectivity

Receiver selectivity specifies the tendency of a receiver to respond to channels adjacent to the desired reception channel. *Adjacent-channel interference* (ACI), a commonly used term in wireless systems, is also used to describe this phenomenon. When considering the LO section, the reference spurs are of particular importance with regard to selectivity. Figure 13 is an attempt to illustrate how a spurious signal at the LO, having the same spacing as the channel-spacing frequency, can translate energy from an adjacent radio channel directly onto the IF. This is of particular concern if the desired received signal is distant and weak and the unwanted adjacent channel is nearby and strong, which can often be the case. So, the lower the reference spurs in the PLL, the better it will be for system selectivity.

Conclusion

In Part 2 of this series we have discussed some of the critical specifications associated with PLL synthesizers, described measurement techniques, and shown examples of results. In addition, there has been a brief discussion of the system implications of phase noise, reference spurs and leakage current.

In the final part of this series, we will examine the building blocks that go to make up a PLL synthesizer. In addition, there will be a comparison between integer-N and fractional-N architectures for PLL.

Acknowledgment

The authors would like to acknowledge Brendan Daly of the Analog Devices GP RF Applications Group in Limerick for the plots of phase noise and reference spurs.

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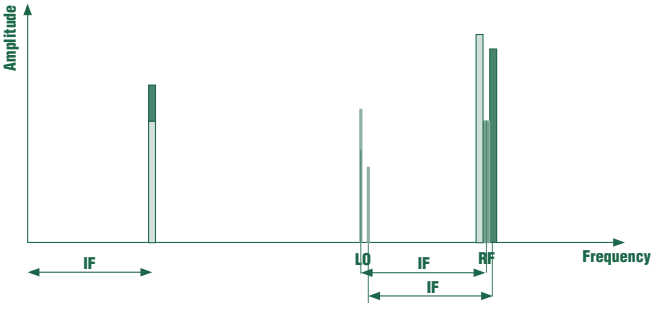

Figure 13. Adjacent Channel Interference.

Phase Locked Loops for High-Frequency Receivers and Transmitters—Part 3

Mike Curtin and Paul O'Brien

The first part of this series introduced phase-locked loops (PLLs), described basic architectures and principles of operation. It also included an example of where a PLL is used in communications systems. In the second part of the series, critical performance specifications, like phase noise, reference spurs, and output leakage, were examined in detail, and their effects on system performance were considered. In this, the last part of the series, we will deal with some of the main building blocks that go to make up the PLL synthesizer. We will also compare integer-N and fractional-N architectures. The series will end with a summary of VCOs currently available on the market and a listing of the Analog Devices family of synthesizers.

PLL Synthesizer Basic Building Blocks

A PLL synthesizer can be considered in terms of several basic building blocks. Already touched upon, they will now be dealt with in greater detail:

Phase-Frequency Detector (PFD)
Reference Counter (R)
Feedback Counter (N)

The Phase-Frequency Detector (PFD)

The heart of a synthesizer is the phase detector—or phase-frequency detector. This is where the reference frequency signal is compared with the signal fed back from the VCO output, and the resulting error signal is used to drive the loop filter and VCO. In a digital PLL (DPLL) the phase detector or phase-frequency detector is a logical element. The three most common implementations are :

Exclusive-or (EXOR) Gate
J-K Flip-Flop
Digital Phase-Frequency Detector

Here we will consider only the PFD, the element used in the ADF4110 and ADF4210 synthesizer families, because—unlike the EXOR gate and the J-K flip flop—its output is a function of both the frequency difference and the phase difference between the two inputs when it is in the unlocked state.

Figure 1 shows one implementation of a PFD, basically consisting of two D-type flip flops. One Q output enables a positive current source; and the other Q output enables a negative current source. Assuming that, in this design, the D-type flip flop is positive-edge triggered, the states are these (Q1, Q2):

11—both outputs high, is disabled by the AND gate (U3) back to the CLR pins on the flip flops.

00—both P1 and N1 are turned off and the output, OUT, is essentially in a high impedance state.

10—P1 is turned on, N1 is turned off, and the output is at V+.

01—P1 is turned off, N1 is turned on, and the output is at V–.

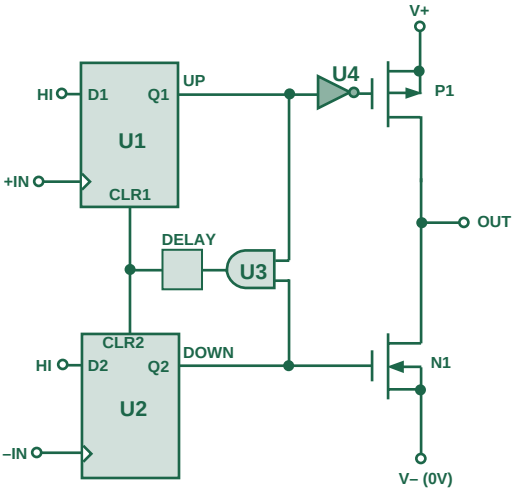

Figure 1. Typical PFD using D-type flip flops.

Consider now how the circuit behaves if the system is out of lock and the frequency at +IN is much higher than the frequency at –IN, as exemplified in Figure 2.

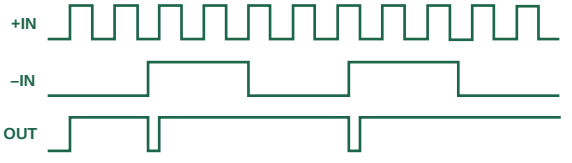

Figure 2. PFD waveforms, out of frequency and phase lock.

Since the frequency at +IN is much higher than that at –IN, the output spends most of its time in the high state. The first rising edge on +IN sends the output high and this is maintained until the first rising edge occurs on –IN. In a practical system this means that the output, and thus the input to the VCO, is driven higher, resulting in an increase in frequency at –IN. This is exactly what is desired.

If the frequency on +IN were much lower than on –IN, the opposite effect would occur. The output at OUT would spend most of its time in the low condition. This would have the effect of driving the VCO in the negative direction and again bring the frequency at –IN much closer to that at +IN, to approach the locked condition. Figure 3 shows the waveforms when the inputs are frequency-locked and close to phase-lock.

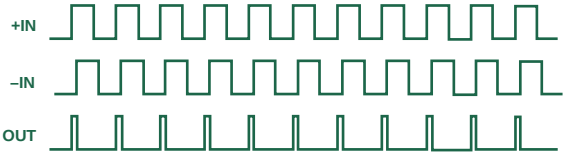

Figure 3. PFD waveforms, in frequency lock but out of phase lock.

Since +IN is leading –IN, the output is a series of positive current pulses. These pulses will tend to drive the VCO so that the –IN signal become phase-aligned with that on +IN.

When this occurs, if there were no delay element between U3 and the CLR inputs of U1 and U2, it would be possible for the output to be in high-impedance mode, producing neither positive nor

negative current pulses. This would not be a good situation. The VCO would drift until a significant phase error developed and started producing either positive or negative current pulses once again. Over a relatively long period of time, the effect of this cycling would be for the output of the charge pump to be modulated by a signal that is a subharmonic of the PFD input reference frequency. Since this could be a low frequency signal, it would not be attenuated by the loop filter and would result in very significant spurs in the VCO output spectrum, a phenomenon known as the *backlash* effect. The delay element between the output of U3 and the CLR inputs of U1 and U2 ensures that it does not happen. With the delay element, even when the +IN and –IN are perfectly phase-aligned, there will still be a current pulse generated at the charge pump output. The duration of this delay is equal to the delay inserted at the output of U3 and is known as the *anti-backlash pulse width*.

The Reference Counter

In the classical Integer-N synthesizer, the resolution of the output frequency is determined by the reference frequency applied to the phase detector. So, for example, if 200-kHz spacing is required (as in GSM phones), then the reference frequency must be 200 kHz. However, getting a stable 200-kHz frequency source is not easy. A sensible approach is to take a good crystal-based high frequency source and divide it down. For example, the desired frequency spacing could be achieved by starting with a 10-MHz frequency reference and dividing it down by 50. This approach is shown in the diagram in Figure 4.

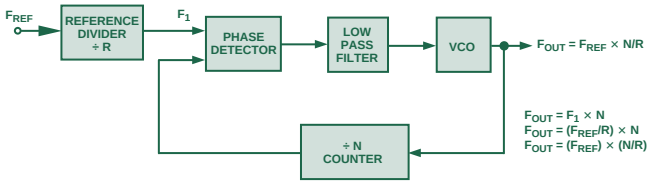

Figure 4. Using a reference counter in a PLL synthesizer.

The Feedback Counter, N

The N counter, also known as the N divider, is the programmable element that sets the relationship between the input and output frequencies in the PLL. The complexity of the N counter has grown over the years. In addition to a straightforward N counter, it has evolved to include a prescaler, which can have a dual modulus.

This structure has grown as a solution to the problems inherent in using the basic divide-by-N structure to feed back to the phase detector when very high-frequency outputs are required. For example, let's assume that a 900-MHz output is required with 10-kHz spacing. A 10-MHz reference frequency might be used, with the R-Divider set at 1000. Then, the N-value in the feedback would need to be of the order of 90,000. This would mean at least a 17-bit counter capable of dealing with an input frequency of 900 MHz.

To handle this range, it makes sense to precede the programmable counter with a fixed counter element to bring the very high input frequency down to a range at which standard CMOS will operate. This counter, called a *prescaler*, is shown in Figure 5.

However, using a standard prescaler introduces other complications. The system resolution is now degraded ($F_1 \times P$). This issue can be addressed by using a dual-modulus prescaler (Figure 6). It has the advantages of the standard prescaler but without any loss in system resolution. A dual-modulus prescaler is a counter whose

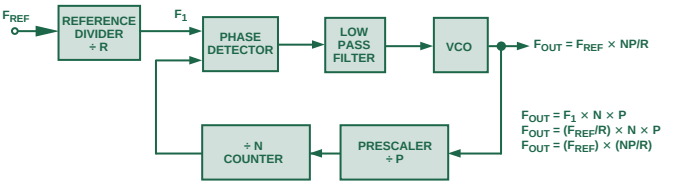

Figure 5. Basic prescaler.

division ratio can be switched from one value to another by an external control signal. By using the dual-modulus prescaler with an A and B counter one can still maintain output resolution of F_1. However, the following conditions must be met:

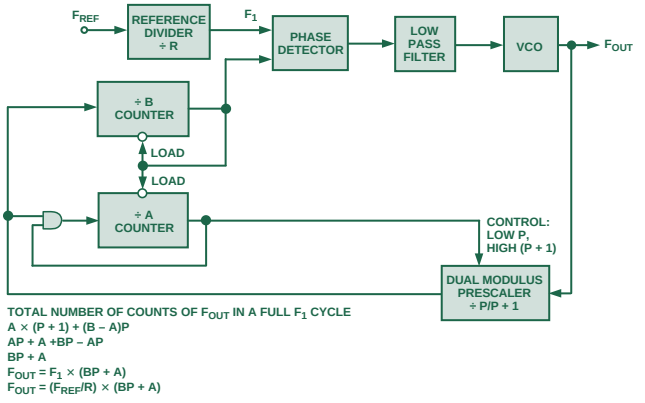

Figure 6. Dual-modulus prescaler.

1. The output signals of both counters are High if the counters have not timed out.
2. When the B counter times out, its output goes Low, and it immediately loads both counters to their preset values.
3. The value loaded to the B counter must always be greater than that loaded to the A counter.

Assume that the B counter has just timed out and both counters have been reloaded with the values A and B. Let's find the number of VCO cycles necessary to get to the same state again.

As long as the A counter has not timed out, the prescaler is dividing down by P + 1. So, both the A and B counters will count down by 1 every time the prescaler counts (P + 1) VCO cycles. This means the A counter will time out after $((P + 1) \times A)$ VCO cycles. At this point the prescaler is switched to divide-by-P. It is also possible to say that at this time the B counter still has $(B - A)$ cycles to go before it times out. How long will it take to do this: $((B - A) \times P)$. The system is now back to the initial condition where we started.

The total number of VCO cycles needed for this to happen is :

$$N = (A \times (P + 1)) + ((B - A) \times P)$$

$$= AP + A + BP - AP$$

$$= A + BP$$

When using a dual-modulus prescaler, it is important to consider the lowest and highest values of N. What we really want here is the range over which it is possible to change N in discrete integer steps. Consider the expression N = A + BP. To ensure a continuous integer spacing for N, A must be in the range 0 to (P – 1). Then, every time B is incremented there is enough resolution to fill in all the integer values between BP and $(B + 1)P$. As was already noted for the dual-modulus prescaler, B must be greater than or equal to A for the dual modulus prescaler to work. From these we can

say that the smallest division ratio possible while being able to increment in discrete integer steps is:

$$N_{MIN} = (B_{min} \times P) + A_{min}$$
$$= ((P - 1) \times P) + 0$$
$$= P^2 - P$$

The highest value of N is given by

$$N_{MAX} = (B_{max} \times P) + A_{max}$$

In this case A_{max} and B_{max} are simply determined by the size of the A and B counters.

Now for a practical example with the ADF4111.
Let's assume that the prescaler is programmed to 32/33.
A counter: 6 bits means A can be $2^6 - 1 = 63$
B counter: 13 bits means B can be $2^{13} - 1 = 8191$

$$N_{MIN} = P^2 - P = 992$$
$$N_{MAX} = (B_{max} \times P) + A_{max}$$
$$= (8191 \times 32) + 63$$
$$= 262175$$

ADF4110 Family

The building blocks discussed in the previous sections are all used in the new families of integer-N synthesizers from ADI. The ADF4110 family of synthesizers consists of single devices and the ADF4210 family consists of dual versions. The block diagram for the ADF4110 is shown below. It contains the reference counter, the dual-modulus prescaler, the N counter and the PFD blocks described above.

Fractional-N Synthesizers*

Many of the emerging wireless communication systems have a need for faster switching and lower phase noise in the local oscillator (LO). Integer N synthesizers require a reference frequency that is equal to the channel spacing. This can be quite low and thus necessitates a high N. This high N produces a phase noise that is proportionally high. The low reference frequency limits the PLL lock time. Fractional-N synthesis is a means of achieving both low phase noise and fast lock time in PLLs.

The technique was originally developed in the early 1970s. This early work was done mainly by Hewlett Packard and Racal. The technique originally went by the name of "digiphase" but it later became popularly named fractional-N.

In the standard synthesizer, it is possible to divide the RF signal by an integer only. This necessitates the use of a relatively low reference frequency (determined by the system channel spacing) and results in a high value of N in the feedback. Both of these facts have a major influence on the system settling time and the system phase noise. The low reference frequency means a long settling time, and the high value of N means larger phase noise.

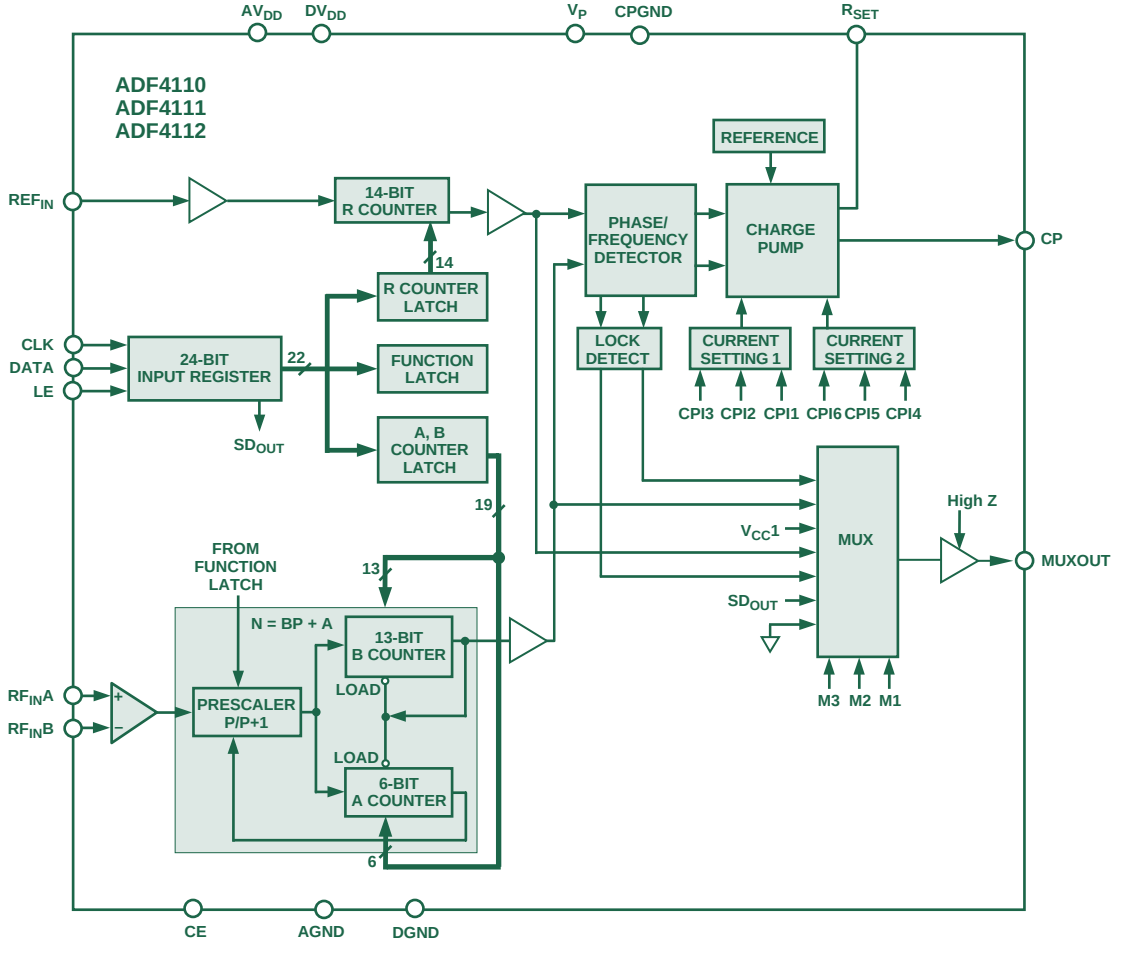

Figure 7. Block diagram for the ADF4110 family.

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If division by a fraction could occur in the feedback, it would be possible to use a higher reference frequency and still achieve the channel spacing. This lower fractional number would also mean lower phase noise.

In fact it is possible to implement division by a fraction over a long period of time by alternately dividing by two integers (divide by 2.5 can be achieved by dividing successively by 2 and 3).

So, how does one divide by X or (X + 1) (assuming that the fractional number is between these two values)? Well, the fractional part of the number can be allowed to accumulate at the reference frequency rate.

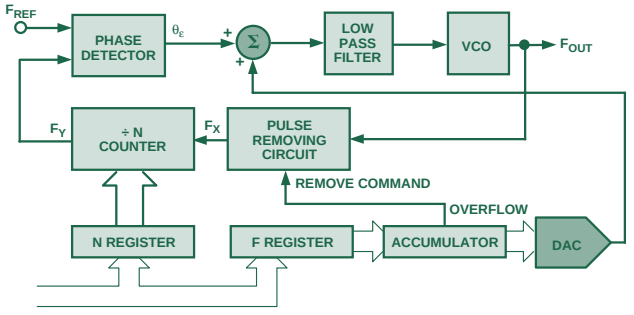

Figure 8. Fractional-N synthesizer.

Then every time the accumulator overflows, this signal can be used to change the N divide ratio. This is done in Figure 8 by removing one pulse being fed to the N counter. This effectively increases the divide ratio by one every time the accumulator overflows. Also, the bigger the number in the F register, the more often the accumulator overflows and the more often division by the larger number occurs. This is exactly what is desired from the circuit. There are some added complications however. The signal being fed to the phase detector from the divide-by-N circuit is not uniform in real time. Instead it is being modulated at a rate determined by the reference frequency and the programmed fraction. This is turn modulates the phase detector output and goes to the VCO input. The end result is a high spurious content at the output of the VCO. Major efforts are currently under way to minimize these spurs. One method uses the DAC shown in Figure 8.

Up to now, monolithic Fractional-N synthesizers have failed to live up to expectations but the eventual benefits that may be realized mean that development is continuing at a rapid pace.

Summary of VCO Manufacturers

With the explosive growth in wireless communications, the demand for products like synthesizers and VCOs has increased dramatically over the past five years. Interestingly, until now, the markets have been served by two distinct sets of manufacturers. Below is listed a selection of players in the VCO field. This list is not meant to be all-inclusive, but rather gives the reader a feel for some of the main players.

VCOs

Murata	Murata has both 3-V and 5-V devices available. The VCOs are mainly narrowband for wireless handsets and base stations. Frequencies are determined by the wireless frequency standards.
Vari-L	Vari-L addresses the same market as Murata. 3-V and 5-V devices are available.
Alps	Alps makes VCOs for wireless handsets and base stations.
Mini-Circuits	Mini-Circuits offers both narrowband and wideband VCOs.
Z-Comm	Z-Communications has both wideband and narrowband VCOs. The wideband VCOs typically have an octave tuning range (1 GHz to 2 GHz, for example) and operate from a supply voltage of up to 20 V. They offer surface-mount packaging.
Micronetics	Micronetics offers both narrowband and wideband VCOs. Their strength lies more in the wideband products where they can go from an octave range at anything up to 1200 MHz. Above these output frequencies, the range is somewhat reduced.

The Analog Devices Synthesizer Family

The table on the next page lists current and future members of the ADF4xxx synthesizer family. It includes single and dual, and integer-N and fractional-N devices.

Acknowledgements

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ADF4xxx Frequency Synthesizer Family

Device	Integer-N Frequency Range	Fractional-N Frequency Range	Single/ Dual	Pin Count	Second Source
ADF4110	≤550 MHz		Single	16	
ADF4111	≤1.2 GHz		Single	16	
ADF4112	≤3.0 GHz		Single	16	
ADF4113	≤3.8 GHz		Single	16	
ADF4116	≤550 MHz		Single	16	LMX2306
ADF4117	≤1.2 GHz		Single	16	LMX2316
ADF4118	≤3.0 GHz		Single	16	LMX2326
ADF4210	≤510 MHz/≤1.2 GHz		Dual	20	
ADF4211	≤510 MHz/≤2.0 GHz		Dual	20	
ADF4212	≤510 MHz/≤3.0 GHz		Dual	20	
ADF4213	≤1.0 GHz/≤2.5 GHz		Dual	20	
ADF4216	≤510 MHz/≤1.2 GHz		Dual	20	LMX2332L
ADF4217	≤510 MHz/≤2.0 GHz		Dual	20	LMX2331L
ADF4218	≤510 MHz/≤2.5 GHz		Dual	20	LMX2330L
ADF4206	≤500 MHz/≤500 MHz		Dual	16	LMX2337
ADF4207	≤1.1 GHz/≤1.1 GHz		Dual	16	LMX2335
ADF4208	≤1.1 GHz/≤2.0 GHz		Dual	20	LMX2336
ADF4150		≤550 MHz	Single	16	
ADF4151		≤1.2 GHz	Single	16	
ADF4152		≤3.0 GHz	Single	16	
ADF4156		≤550 MHz	Single	20	
ADF4157		≤1.2 GHz	Single	20	
ADF4158		≤3.0 GHz	Single	20	
ADF4250	≤550 MHz	≤1.2 GHz	Dual	20	
ADF4251	≤550 MHz	≤2.0 GHz	Dual	20	
ADF4252	≤1.0 GHz	≤3.0 GHz	Dual	20	
ADF4256		≤550 MHz/≤1.2 GHz	Dual	20	
ADF4257		≤550 MHz/≤2.0 GHz	Dual	20	
ADF4258		≤1.0 GHz/≤3.0 GHz	Dual	20	

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