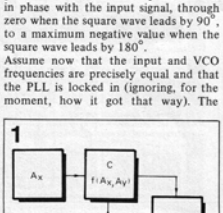
pll systems

It is the intention of this article to give an introduction to Phase-Locked-Loop (PLL) systems, without assuming any advanced mathematical knowledge on behalf of the reader, nor any familiarity with the subject.

The need for such an introduction stems from the ever-increasing use of PLL circuits in consumer electronics and from the increasing complexity of these circuits, which is threatening to make new developments in this field incomprehensible to many electronics enthusiasts. The article also deals with Feedback PLL systems, which are in many ways superior to conventional PLL circuits.
A simple receiver using the Feedback PLL principle will be described in a future issue.

A phase-locked-loop is a control system in which an electrical quantity is controlled by the phase difference between two signals. Figure 1 shows a block diagram of an arbitrary servo control system.
Ax and Ay are quantities of the same form such as A.C. or D.C. potentials. These quantities are compared with one another in block C by, for example, multiplication or subtraction. The result of the comparison is processed in block C in such a way that quantity Ay is adjusted. The form of processing determines a number of the control characteristics such as the control time constant. Quantity Ay is readjusted in such a way that a state of equilibrium is reached at the output of C.
Figure 2 is a block diagram of a PLL. In this case control is based on the phase difference between the input signal (1) and the signal (2) from a Voltage-Controlled Oscillator (VCO) so the contents of block ϕ must be able to recognize this difference.
The VCO is controlled in such a way that a specific phase difference is maintained between the output from the VCO and the input signal. The speed with which the PLL adjusts the VCO to follow any change in the input signal depends, in the first instance, on the characteristics of the low-pass filter LPF.
When two signals are multiplied together, the product includes a component that is proportional to their phase difference and that can be filtered out from the other components. Block ϕ performs this multiplication. In practical circuits the input signal is multiplied by a square-wave output from the VCO, which means in effect that alternate half cycles of the VCO square wave multiply the input signal by +1 and −1. The waveforms in figure 3 should make it easier to understand the mode of operation.
In figure 3a the input (represented as a sinusoid) is shown and below it a VCO square wave of the same frequency is repeated with phase relationships varying progressively from in-phase to 180° leading (figures 3b, 3d, 3f, 3h and 3j). During the positive half-cycles of the VCO square wave (in any particular phase) the associated 'product' waveform (figures 3c, 3e, 3g, 3i and 3k) is the same as the input sine wave of 3a. During the negative half-cycles of the square wave the sine wave of 3a is polarity-changed in the product waveform. This is equivalent to multiplying the two waveforms together.
In the first product waveform (3c), which is associated with the in-phase square wave 3b, it will be seen that the product never becomes negative, in fact it is a full-wave rectified version of the sine wave. Its filtered D.C. value is thus unmistakably positive. When the square wave is leading by 45°, as in 3d, the product 3e clearly has a greater area above the line than below. Its mean D.C. level is therefore also positive, but less than 3c. When the square wave leads by 90°, as in 3f, the product 3g has equal areas above and below the line, so its D.C. value is zero. With leads greater than 90° the D.C. value of the product becomes negative, reaching a maximum (negative) value at +180° (3h to 3k). Summarising; the D.C. value of the product waveform varies from a maximum positive value when the square wave is in phase with the input signal, through zero when the square wave leads by 90°, to a maximum negative value when the square wave leads by 180°.
Assume now that the input and VCO frequencies are precisely equal and that the PLL is locked in (ignoring, for the moment, how it got that way). The VCO square wave will be leading the input signal by 90° and the D.C. output of the phase comparator (multiplier) will be zero. Suppose now that the VCO frequency tends to increase. The phase lead will become greater than 90° and the D.C. output of the phase comparator will become negative. This will tend to reduce the VCO frequency and lock will be maintained with a slight increase in the phase lead. Conversely, if the VCO frequency tends to decrease, the output of the phase comparator will become positive, which will tend to increase the VCO frequency.
It can be shown that the input signal can also lock to harmonics of the VCO frequency, or the VCO to harmonics of the input signal (if the input signal is not sinusoidal as previously assumed). It is also possible to insert a frequency divider between the VCO and the phase comparator and by a combination of frequency divider and harmonic locking the ratio of VCO frequency to input frequency can be made to assume peculiar values such as 16/3 for example. This opens up intriguing possibilities for frequency synthesis.



The capture process

Until now it has been assumed that the PLL is locked in. It is now necessary to consider what happens when the circuit is switched on and the VCO is out of lock, as it almost certainly will be. The short answer is that the VCO hunts until it finds a frequency and phase to which it can lock.
Some understanding of the capture process, as it is called, may fortunately be acquired without mathematics if the behaviour of the circuit is examined at certain points in the loop and certain assumptions are made.
To assist in the explanation, assume first that the connection between the LPF output and the VCO input is broken. The VCO, deprived of a control voltage, will take up its free-running frequency which may be assumed to be lower than the input frequency. It has already been assumed, when discussing the locked-

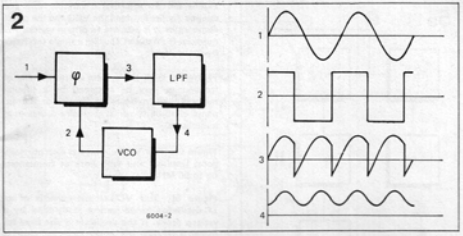
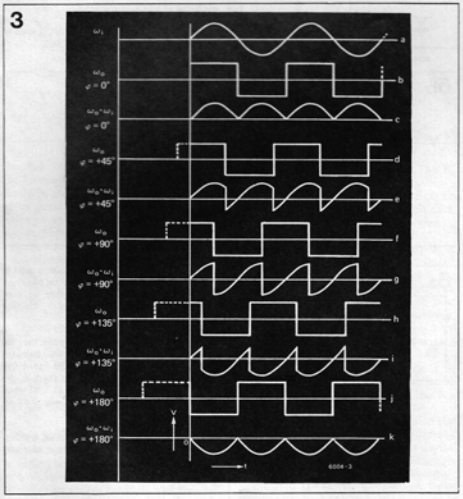


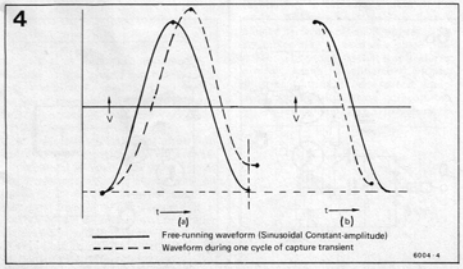
Figure 1. A control system consists of an information source Ax, a comparator circuit C, a processing circuit B and a controllable quantity Ay.

Figure 2. The elements of a PLL are: the phase comparator ϕ, the low-pass filter LPF, and the controllable oscillator VCO.

Figure 3. Showing how the output of the phase comparator varies with the phase difference between the input signal and the VCO.

Figure 4. Diagram to illustrate how the difference frequency waveform changes during one cycle of the capture transient.





condition, that the VCO frequency increases when the VCO control voltage goes positive and decreases when it goes negative. It may also be assumed that the LPF completely removes frequencies equal to the sum of the input and VCO frequencies, that it passes D.C. with no attenuation and that it passes the difference frequency of the VCO and input signal with some attenuation, which decreases as the difference frequency decreases (i.e. as the VCO frequency approaches the input frequency).

While the VCO is running free because of the supposed broken connection a difference-frequency oscillation of constant amplitude appears at the LPF output. When the connection is re-made what next happens must be examined carefully. As pull-in has not yet taken place a difference frequency still exists and an oscillatory voltage is fed to the VCO control input.

Consider now one positive swing of the VCO control voltage from trough to crest (figure 4). The VCO control voltage is going positive, therefore the VCO frequency is increasing and the difference frequency is decreasing. Because of the decreasing difference frequency the attenuation of the difference frequency signal in the LPF will be progressively reduced and the overall swing of the VCO control voltage will have greater amplitude than with the VCO free-running. Figure 4a compares the positive-going swings under controlled and free-running conditions, starting from the same trough potential and time. The crest of the controlled swing is more positive and it occurs later because the difference frequency is decreasing.

Figure 4b shows what happens during a negative (crest-to-trough) swing. Here the VCO control voltage is going negative and the VCO frequency is decreasing, so the difference frequency is increasing. Attenuation in the LPF is thus progressively increasing; overall amplitude is less than when free-running and the trough occurs sooner.

Figure 4b is added onto 4a to show what will happen during one complete trough-

to-trough cycle of the difference signal. The positive-going half cycle has a more positive peak than the free-running difference signal. This 'handicaps' the negative-going half signal and its reduced amplitude also helps to make the trough more positive than it would be in the free-running condition.
Later cycles of the capture-transient, as it is called, cannot be compared with the free-running waveform, but they follow the same general pattern. Positive-going swings have increased amplitude while negative-going swings have reduced amplitude. This results in both crests and troughs becoming progressively more positive whilst the time interval between them becomes longer. This means that the VCO frequency will also increase until a point is reached where one of these swings of the control voltage sweeps the VCO frequency through the input frequency. More swings may occur until the VCO has found the correct phase relationship before lock-in actually occurs.

Applications of Phase Locked Loops

A PLL provides two information outputs. The VCO frequency, which is related to the input frequency, and the VCO control voltage whose value depends on the phase difference between the input signal and the VCO output.
If the desired information contained in the input signal is in the form of a frequency change (i.e. frequency modulation) then the PLL may be used as an FM detector. Its advantages over ratio detectors and coincidence detectors are: less distortion, better suppression of interference and the absence of LC circuits. PLL's are also useful in frequency synthesis as figure 5 shows. In the example given in figure 5a the condition for lock-in is that $f_c/nv = f_r$ and with a channel spacing of Δf we have $\Delta f = f_r$. The frequencies delivered by the VCO are thus multiples of the reference frequency and it follows that the VCO frequency is itself determined by the division ratio n_v. In many practical cases a variable-ratio divider will not be able to accept a high VCO frequency directly, so the VCO frequency is fed first to a stable fixed-ratio divider and from this to a stable adjustable divider. With this procedure it is possible to divide down from a relatively high carrier frequency to a low channel-spacing frequency. This is useful in, for example, aircraft VHF equipment.
In figure 5b an arrangement for frequency synthesis is shown in which delta pulses (needle pulses) recurring at the reference frequency from a crystal oscillator are fed into the phase comparator together with the VCO signal. As delta pulses contain the odd and even harmonics of the fundamental frequency the PLL can lock onto any harmonic.

Construction of a PLL

a. The VCO

Requirements for the VCO depend, in the first instance, on the application of

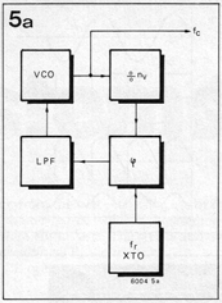


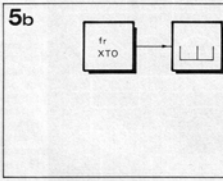
Figure 5a. By inserting a variable-ratio frequency divider between the VCO and the phase comparator it is possible to obtain various frequencies from the VCO using a single reference frequency f_r.

Figure 5b. With this system a large number of frequencies may be obtained by a simpler method than in figure 5a, though at the expense of stability which generally decreases as n increases.

Figure 6a. This VCO circuit has exceptionally good linearity and will work at frequencies up to 50 MHz.

Figure 6b. This VCO circuit consists of an LC oscillator tuned and/or controlled by a varicap diode. If the oscillator is also used for tuning a receiver (i.e. as the local oscillator) it is known as a tuneable voltage-controlled oscillator (TVCO).

Figure 7. Simplified circuit of a VCO used in PLL IC's such as the Signetics NE565.



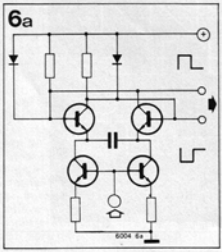
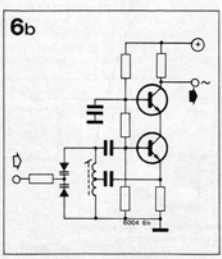
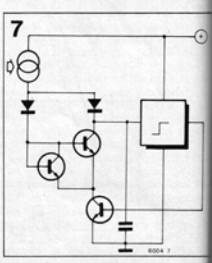


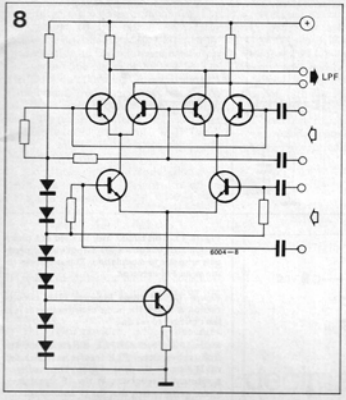
Figure 8. The symmetrical multiplier is used in almost all PLL IC's and can also be obtained as an IC in its own right. It may be constructed successfully from discrete components also.

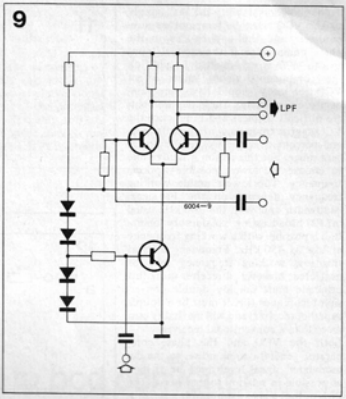
Figure 9. An asymmetric multiplier may be used, provided that the low-pass filter can provide sufficient suppression of the input frequencies. This type of circuit is used in the input section of an OTA and a PLL of good performance can, in fact, be built with an OTA type CA3080.

Figure 10. If RF transformers are used, a chea multiplier may be built using four identical diodes.









the PLL. When it is to be used as an FM detector the linearity (Frequency change v. control voltage change) should be as good as possible, while for frequency synthesis this is unimportant but high stability is essential.

Voltage-controlled multivibrators or varicap-tuned LC oscillators, like those shown in figures 6a and 6b respectively, generally have to be made up from discrete components, while integrated PLL circuits, such as the Signetics 565 shown in figure 7, rely on the triggering principle.

Where a PLL is to be operated with a fluctuating supply voltage the VCO frequency should be independent of voltage, or alternatively a stabilised supply may be used.

b. Phase Comparator

The output from the phase comparator or multiplier must be dependent solely on the product of the signals fed into it. This requirement is basically met by any non-linear component, subject to the proviso that the input signals also appear in the output. It is important to ensure that these signals have no detrimental effect on the performance of the system.

An even more important requirement is that the output should not contain any D.C. components resulting from rectification of the input signals, as this can cause 'mistracking' and may even cause the PLL to go out of lock.

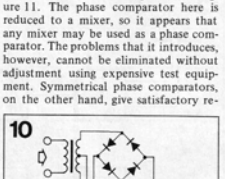
If a balanced multiplier as shown in figure 8 is used impairments such as these can easily be avoided. The input signals are suppressed by the circuit and no rectification occurs. If suppression of the input signals is not required it is possible to use an asymmetric multiplier such as the example in figure 9. A circuit of this kind is included in the input of an operational transconductance amplifier (OTA) such as the CA 3080. This IC performs well in PLL circuits.

It will be understood that rectification of the input signals can occur in this case, but nonetheless a satisfactory degree of AM suppression may be achieved.

The best performance in this respect is achieved when the VCO output is fed into the asymmetric input and the input signal into the symmetrical input. The amplitudes of the signals should not exceed 0.5 V and 0.05 V respectively. The degree of AM suppression that may be obtained is almost as high as with a symmetrical multiplier.

If R.F. transformers are available it is possible to use a diode ring modulator as a multiplier as in figure 10, but this is a rather old-fashioned method.

The simplest, but unfortunately also the worst, solution for a phase comparator consists of a single semiconductor device that is fed with a VCO signal large enough to switch it on and off continuously. Because of the inevitable feedback from the circuit to the VCO a buffer stage is essential, as in the arrangement of figure 11. The phase comparator here is reduced to a mixer, so it appears that any mixer may be used as a phase comparator. The problems that it introduces, however, cannot be eliminated without adjustment using expensive test equipment. Symmetrical phase comparators, on the other hand, give satisfactory results with very little outlay on test equipment.



c. The low-pass filter

The low-pass filter (LPF) is the circuit that determines the bandwidth of a PLL. Simple RC filters, a few examples of which are given in figure 12, usually suffice. Examples b, c and d are suitable for symmetrical phase comparators, while a is applicable to asymmetric arrangements. As a general rule resistor R is already a component in the phase comparator.

Although the calculation of component values for the low-pass filter is easily accomplished when using IC PLL's by referring to the manufacturer's data, sophisticated test equipment is needed to evaluate the performance of a PLL at frequencies in excess of 10 MHz. Filter d is the most suitable for home-built equipment.

The cut-off frequency of the RC combination formed by C_2 and the output resistance of the phase comparator is determined by the lowest frequency to be detected (20 Hz in Hi-Fi FM). The cut-off frequency of the second RC section, formed by P (at its maximum value) and C_1 both connected in parallel with the output resistance, is determined by the maximum PLL input frequency deviation. Any desired bandwidth, up to a maximum determined by the loop gain and the input signal amplitude, may now be set with P.

Problems experienced with PLL's

Theoretically a PLL detector exhibits great advantages over other FM detectors, but in practice these are difficult to realise fully. There are two basic critical factors:

1. VCO frequency stability
2. Signal/noise ratio

To obtain good stability the D.C. supply to the VCO must be temperature-compensated, and this applies also to the phase comparator if the control input to the VCO is asymmetric. In addition the components whose values affect VCO frequency should have zero temperature coefficients. These requirements are difficult to meet and in practice the VCO centre frequency often drifts several percent over the working temperature range. For this reason it is advisable to choose the lowest possible working frequency. The lowest usable working frequency depends on the FM signal bandwidth and with the 200 kHz usual in FM broadcasting satisfactory operation is possible with a working frequency as low as 450 kHz. Frequency drift at this low working frequency may be neglected; however, a receiver using this principle must employ double conversion techniques (i.e. it must be a double superhet receiver) and will inevitably cost more than a conventional receiver.

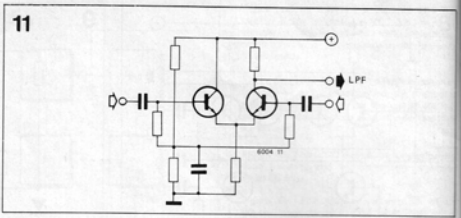
Both the VCO and the phase comparator generate some noise, so the demodulated signal level must be as high as possible in relation to that noise. The PLL output-signal amplitude is proportional to the quotient of the deviation f and the working frequency, which in a receiver is of course the intermediate frequency f_{IF}. With an intermediate frequency of 10.7 MHz and a deviation of 75 kHz this quotient is about 0.007, while with an IF of 450 kHz it is 0.17 so that the lower frequency improves the signal-to-noise-ratio by about 28 dB.

A PLL constructed from discrete components, working at 450 kHz and using the phase comparator of figure 8 and the VCO of figure 6a, can achieve a signal-to-noise-ratio of 60 dB on a stereophonic broadcast.

Feedback PLL

As outlined above, the main problem when using a conventional PLL as an FM detector arises from the standardisation on 10.7 MHz as an IF frequency. This means that practically all commercially available FM front-ends have an IF output at this frequency. In addition, special provision has to be made for the derivation of an automatic frequency correction (AFC) control voltage from the PLL. However, by removing some of the components from the AFC loop in a conventional tuner the local oscillator can be used as a VCO. The linearity of such a VCO can be quite good since the 75 kHz deviation is small in relation to the working frequency (around 100 MHz). The reference frequency for the phase comparator can be supplied by a stable oscillator in which the frequency-determining element is a quartz crystal or a ceramic filter, so that VCO phase jitter noise, which is relatively strong at 10.7 MHz, is avoided.

Figure 13 is a block diagram of a feedback PLL. The aerial signal is mixed with the output from the tuneable voltage-controlled oscillator (TVCO) to give a 10.7 MHz signal that is fed through



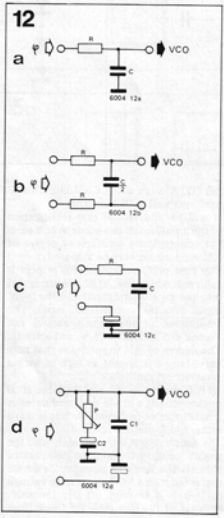
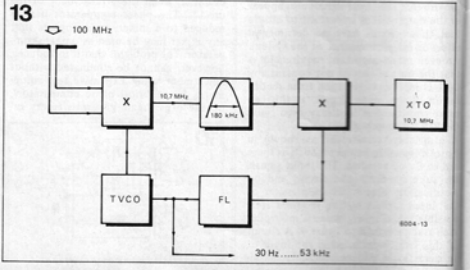


Figure 11. This circuit may be used as a phase comparator, but unwanted demodulation products arise due to modulation. This precludes its use as an FM detector.

Figure 12. Of these low-pass filter circuits version d is best for home construction as it is least critical to set up.

Figure 13. Feedback PLL differs essentially from conventional PLL insofar as it includes the IF filter in the control loop. This results in a substantial reduction in the IF signal deviation, to the extent that the IF bandwidth can be low enough for m to be unity or less. This makes alignment of the bandpass filter and component values in the low-pass filter exceedingly critical and for these reasons it is better to choose a larger bandwidth. There are a number of feedback PLL systems in which the principal aim is to maintain the modulation index as consistently as possible at unity. The complexity of such systems, however, as well as the difficulty of aligning them, limits their use to radio amateurs with sufficient theoretical knowledge and to space-travel communication.



an IF filter to the phase comparator. The other input to the phase comparator receives a high-stability 10.7 MHz reference signal from the reference oscillator, thus, when the signal is locked in, the TVCO follows the aerial signal deviation. This means that the deviation of the 10.7 MHz signal is considerably reduced, hence the name 'Feedback PLL'. Because of this reduced deviation the IF bandwidth is much smaller than in a conventional receiver.

In the article entitled 'Modulation Systems' the minimum bandwidth of an FM signal is given as:

$$b_{min.} = 2(m + 1)f_{LFmax}$$

and this relationship is valid when $m \gg 1$. In a feedback PLL, however, the IF-signal modulation index is considerably less than 1 which accounts for the reduced bandwidth. The significant advantage of a feedback PLL system lies in the IF bandwidth, which becomes independent of deviation and in fact depends only on the highest modulation frequency. This gives improved signal-to-noise ratio and lower distortion compared to a conventional receiver, although the degree of improvement depends on the original modulation index of the aerial signal.

For mono FM transmissions, with a maximum modulation frequency of 15 kHz and a modulation index of 5, the IF bandwidth in a conventional receiver must be 180 kHz, whilst the bandwidth in a feedback PLL receiver is only 30 kHz. The ratio is considerably less unfavourable for stereo transmissions however, as the highest modulation frequency of 53 kHz means that the feedback PLL IF must have a bandwidth of 106 kHz. The principle of feedback PLL was known before the introduction of stereo FM broadcasting but unfortunately this did nothing to prevent the introduction of multiplex stereo systems and so any improvements that might have been made in stereo reception were thrown away.

It is still true to say, however, that a feedback PLL receiver similar to figure 13 gives a considerable saving in cost compared to a conventional receiver with comparable performance. Feedback PLL systems are of particular interest to radio amateurs, because significant improvements in signal-to-noise ratio may be realised if a low maximum modulation frequency is specified. However, as far as the author is aware, little work has been carried out in this field. This is surprising as the principles involved have been known for many years and the VHF and UHF amateur bands offer unlimited possibilities for experimentation.

Summary

PLL is particularly suitable for frequency synthesis and for demodulation of FM signals. When used as an FM detector the relative deviation of the input signal should be as high as possible. This involves the use of multiple frequency conversion which is too expensive for the consumer market and too complicated for many home constructors.

Feedback PLL's may be used at high frequencies and offer the advantages of reduced IF bandwidth and lower distortion with the absence of conventional AFC. Full exploitation of the potential of feedback PLL's is probably too expensive for consumer applications. Nevertheless, simplified feedback PLL circuits are feasible and are indeed cheaper than conventional receivers. They should, therefore, be of interest in consumer electronics.

VHF and UHF radio amateurs are particularly well placed to take advantage of feedback PLL techniques, as their own experience makes them familiar with the RF work involved.

A simple feedback PLL FM receiver will be described in a future issue of Elektor.

J. Wittje

decimal to bcd converter

This converter can be used as a manual encoder which will convert decimal coded signals into BCD codes and drive digital circuits. Furthermore, the converter can be used as a teaching aid for explaining the BCD code.

One IC and six germanium diodes are sufficient for converting a decimal number into a BCD number. A switch for zero is not provided because the converter automatically indicates zero when all switches are open. The reverse resistance of the diodes must be as high as possible (if necessary, check with an ohmmeter) and the gate inputs can be provided with a pull-up resistor connected to the positive supply voltage.

If the circuit is to be used to explain the BCD code, the BCD-output conditions can be indicated by means of LED's. The circuit for the required buffer stage is shown in figure 2.

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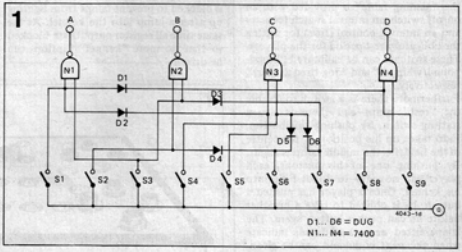

Table

D	C	B	A	Decimal
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

2