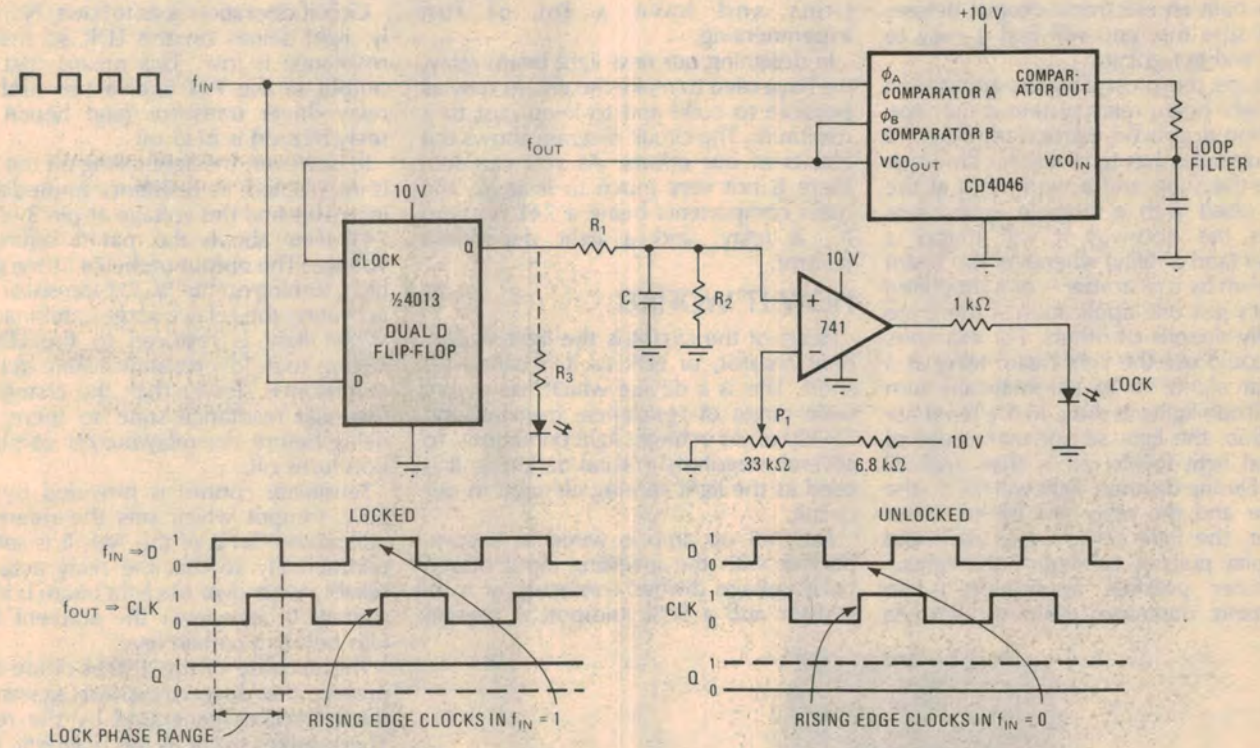
PLL lock indicator detects latching simply



Much less complex than some of the previously described lock indicators for phase locked loops, with no need to derive and utilise a multiple of the input frequency for phase comparison purposes, this circuit is easier to set up and use. It sacrifices nothing in the way of accuracy and offers other advantages, such as the ability to lock onto harmonics of the input signal.

The locking technique is illustrated for the CMOS CD4046 PLL, whose output leads the input by 90° when the lock state is achieved. The loop's capture ratio is such that lock can be maintained for a square wave input signal no greater than +90° and no less than −90° out of phase with respect to f_{out}. The 4013 D flipflop detects phase differences by clocking the state of f_{in} at f_{out}'s rising edge. Assuming the PLL and its associated loop filter are working properly, a steady Q = 1 at the output of the flipflop indicates the PLL is in or will shortly be in the lock state. The non-inverting input of the 741 comparator will then rise to 10V through the integrator R1R2C, and its resulting high going output will light the light-emitting diode.

If the PLL no longer locks on frequency, the phase of f_{in} with respect to f_{out} will be random. The output of the flipflop will thus be a train of variable width pulses. The comparator input thus drops to approximately 5V and because potentiometer P1 sets the inverting input at approximately 7V, A1 moves low, extinguishing the LED.

The lock detector will lock onto higher harmonics of f_{in}. With a 50/50 mark-to-space square wave signal, locking has been observed to the fifth harmonic.

If a less precise indication is tolerable, lock detection can be achieved with even fewer parts by placing a LED at the output of the flipflop and eliminating the comparator circuitry. Resistor R3 should be selected to hold the LED dim for the out-of-lock condition.

(By Steve Kirby, in "Electronics", April 10, 1980.)