THE DIGITAL ELECTRONICS COURSE

GETTING FAMILIAR WITH A/D CONVERTERS

Read about phase-locked loops and learn how to take advantage of these powerful but easy-to-use devices in your own circuits.

BY ROBERT A. YOUNG

The phase-locked loop (PLL) is a linear circuit that is often used in conjunction with digital circuits in consumer electronics—for instance, in tone decoders, FSK (frequency-shifted keying), FM demodulators, frequency-synthesizer applications, and tuner systems. It is primarily used to perform demodulation—where it is used to follow phase or frequency—and for synchronization—where it used to track a carrier or a synchronizing signal that may vary with time.

Inside the PLL. A functional block diagram of the typical PLL circuit is shown in Fig. 1. As shown, a PLL is made up of three sections: a phase comparator (also called phase detector), a low-pass filter, and a voltage-controlled oscillator (or VCO, as it is commonly called). The VCO is an oscillator whose free-running frequency is determined by an external resistor and capacitor (denoted R_e and C_e, respectively) that form an RC network. The output of the PLL is taken at the output of the VCO. The VCO is assumed to have a free-running frequency and a frequency shift that is proportional to the input control voltage.

Our gratitude is extended to the EIA/CEG for the creation of this course, especially to the consultants who brought it to fruition: Dr. William Mast, Appalachian State University; Mr. Joseph Sloop, Surry Community College; Dr. Elmer Poe, Eastern Kentucky University.

The Digital Microprocessor Course is reprinted here with the permission of the Electronic Industries Association/Consumer Electronic Group (EIA/CEG). The complete parts kit is available from EIA/CEG. For further information, contact EIA/CEG Product Services Department, 1722 Eye Street, NW, Suite 200, Washington, DC 20006; or call 202/457-4986.

The input to the PLL (e_i) is a sinewave of arbitrary frequency, while the VCO output (e_o) is a sinewave of the same frequency, but of arbitrary phase. If:

$$e_i = \sqrt{2E_i}\sin(\omega_o t + \theta_1(t))$$

and

$$e_o = \sqrt{2E_o}\cos(\omega_o t + \theta_2(t))$$

then the output of the phase detector is:

$$e_d = e_i \times e_o$$

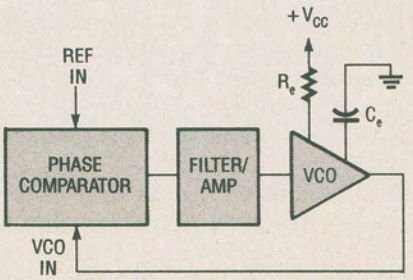

Fig. 1. The typical PLL circuit is made up of three sections: a phase comparator (also called phase detector), a low-pass filter, and a voltage-controlled oscillator (VCO).

The low-pass filter removes the AC components of the detector output, and the DC term is seen as a function of the difference in phase angle between the VCO output and the input signal.

A better understanding of the PLL may be obtained by considering that initially the frequency of the input signal and the VCO output are very close in frequency, but not identical. Under those conditions, the output of the detector is equal to the frequency difference of the VCO output and the input signal.

If no input signal were applied, the VCO would oscillate at a center frequency—usually selected to be within the desired output frequency range—which is set by the external RC network. The VCO's output frequency is referenced to the phase comparator. The phase comparator accepts two inputs; one from an input reference and the other a sampling of the VCO output. The phase comparator detects phase differences between the input reference signal and the VCO output. Since the phase difference is a function of the frequency difference, the comparator might be said to detect frequency differences.

The comparator converts the difference between the input reference signal and the VCO output into an output signal that is applied to the low-pass filter. The low-pass filter (or integrator) converts the signal received

from the comparator into a DC voltage by averaging the output of the phase comparator. That DC voltage is then fed to the VCO's control input.

Let's suppose that the loop feeding the VCO is closed with no input reference signal applied to the phase comparator. Under that condition, the VCO oscillates at its center frequency, drifting at every opportunity. But when a stable frequency is applied to the phase comparator's reference input, assuming that the input frequency is within the PLL's capture range, or is a harmonic thereof, a voltage will be developed at the output of the low-pass filter. That voltage, when applied to the VCO, causes the VCO to lock onto the incoming frequency.

With the loop in lock, the difference-frequency output of the phase detector is a voltage that is a function of the phase difference. If the input frequency is equal to the VCO's free-running frequency, the control voltage into the VCO must be zero.

PARTS LIST FOR THE PLL EXERCISE

U1—555 oscillator/timer, integrated circuit
U2—7476 dual J-K flip-flop, integrated circuit
U3—565 phase-locked loop, integrated circuit
C1–C3—0.1-μF, ceramic-disc capacitor
C4, C5—0.01-μF, ceramic-disc capacitor
R1, R2—100,000-ohm potentiometer
R3–R5–1000-ohm, ¼-watt, 5% resistor
Breadboard materials, dual 5-volt power source, wire, etc.

Let's now assume that the input (reference) frequency increases, causing an instantaneous phase difference between the VCO output and the input (reference) frequency. That would

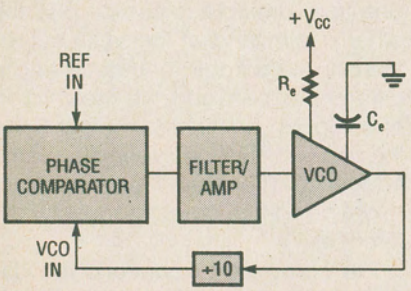

Fig. 2. By feeding the VCO's output to a divide-by-ten counter/divider prior to the PLL's phase comparator (as shown here) a PLL can be used as a frequency synthesizer.

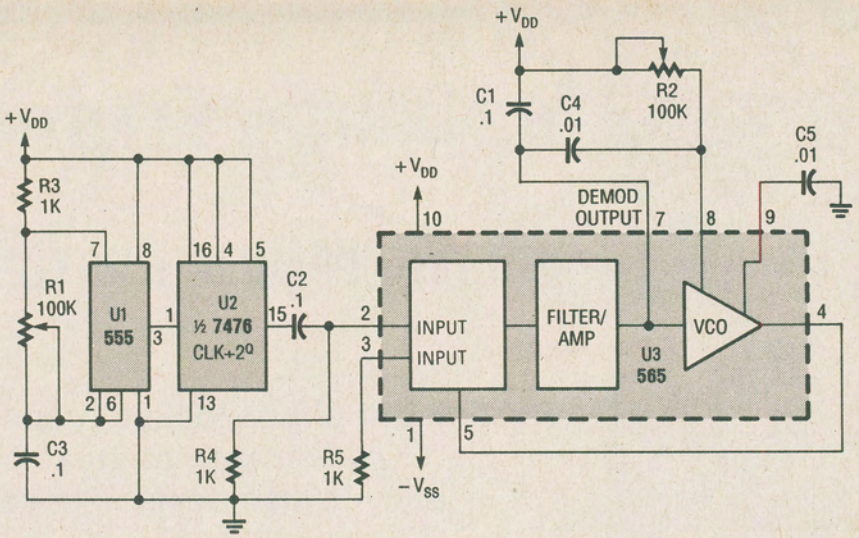

Fig. 3. A 555 oscillator/timer configured for astable operation supplies a reference signal, which is fed through a flip-flop that's used to divide the signal by a factor of two before it is applied to the PLL. Varying the output frequency of the oscillator will cause a corresponding change in the oscillating frequency of the PLL's VCO.

cause an increase in the voltage developed in the low-pass filter. When that voltage is fed to the VCO's control input, the VCO's output frequency would increase until it equals the input frequency. A decrease in frequency would have the opposite effect.

The range of frequencies that the PLL can lock onto is called the capture range; the range of frequencies over which the VCO output will follow the input reference is called the lock range.

Frequency Synthesis. Figure 2 shows a block diagram of a PLL-based frequency synthesizer. Note that the VCO's output is fed to a divide-by-ten counter/divider prior to application to the phase comparator. Under that condition, the phase comparator always sees a 10-to-1 phase relationship between the input reference and the VCO output and therefore forces the VCO to produce an output signal that's ten times the input reference signal.

If a divide-by-eight counter/divider is substituted for the divide-by-ten unit, the VCO's output would go to 8 times the input reference. Programmable counter/dividers used in consumer products use this scheme to generate a wide range of frequencies.

PLL Exercise. In this exercise, the 565 phase-locked loop is powered from a split 5-volt (±5-volt) supply, which can be formed by connecting two 5-volt supplies. The reference input to the circuit is supplied by a 555 oscillator/timer (U1) configured for astable operation (see Fig. 3). The output of the astable multivibrator is then fed through a flip-flop (half of a 7476 dual J-K flip-flop), which divides the frequency of the signal applied to it by two. The output of the flip-flop (U2) is AC-coupled to the input of the PLL (U3). Resistors R4 and R5 are used to bias the inputs to U3's internal comparator to accept the astable signal generated by U1.

For this exercise you'll need a dual-trace oscilloscope to view the input (reference) signal and to set the input to U3's internal VCO to 1 kHz. If only a single-trace oscilloscope available, it will be necessary to switch the scope probes from location to location to view the various signals.

Assuming that you are using a dual-trace scope, connect one channel input between the output of U2 and capacitor C2. Connect the other scope channel to the output of U3's VCO at pin 4, and sync the scope on that input signal. The VCO should be running at the reference frequency. Slowly adjust the frequency of the oscillator (U1) either up or down by varying the resistance of potentiometer R1 and observe the output of the VCO. Note that the VCO will free run for a while, and then lock onto the new input frequency.

Now, cascade the two flip-flops of U2—producing a divide-by-four circuit—while keeping the rest of the circuit intact. Feed the oscillator output to the input to PLL. Observe the output of the VCO. Next, disconnect one of the cascaded flip-flops from its present position, and place it in the PLL's feedback loop, between pins 4 and 5 of U3. What effect does that have? ■